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An on-chip TVS design to meet system level ESD protection for RS485 transceiver

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ABSTRACT

RS485 interface is widely used in the area of industrial control and remote meter reading, which is often subjected to serious electrostatic damage. A new On-Chip TVS (OCT) structure without extra process modification and a novel electrostatic discharge method for RS485 transceiver IC have been proposed. It is composed of a series of Zener diodes and fabricated in 5V/18V/24V 0.5μm CDMOS technology. A 100ns pulse width of the Transmission Line Pulsing (TLP) test is performed for this proposed OCT. The driver circuit itself can work as an ESD device as well. The OCT trigger voltage is compatible with the signal level of RS485 standard. The OCT device protection level of human-body-model (HBM) is up to 16.34kV. RS485 transceiver integrated with OCT has also been tested in order to verify its reliability. The results indicate that it can pass the IEC61000-4-2 contact ±10kV stress and IEC 61000−4−4 Electrical Fast Transient (EFT) ±2.2kV without any hard damages and latch-up issues. The RS485 transceiver integrated with the OCT allows error-free data rate transfer up to 500 kbps. The chip occupies a silicon area of $2.4 \times 1.17 mm^2$.

Keywords: On-Chip TVS (OCT); Transmission line pulsing (TLP); RS485 zener diode.

INTRODUCTION

Remote read and control become a vital technology in the Internet of Things application. [1] introduces a monitoring system via RS485 serial communication protocol. [2] designs an Automatic Nucleic Acid Detection System though RS485 bus. The low-voltage meter reading system is based on RS485 interface [3]. RS485 network is the critical communication method in power system management. [4] presents the parallel operation control of a modular AC to DC converter via RS485 serial communication bus, and RS485 can leave addressing to a higher level of software [5]. RS485 interface is proved to be an indispensable remote transmission interface of an intelligent electrical network. RS485 is communication used widely in the electricity information collection system [6]. A ModBus interface, which runs on the RS485 configuration, was used to establish the interface with the SCADA system through the MATLAB application [7]. The intelligent meter reading technology becomes more and more popular in meter application, and RS485 network is the key transmission interface of a smart grid [8]. Unfortunately, intelligent electrical meters are often located outdoors, which transmit signals via outdoor cables. Lightning surge,

static electricity, and other destructive transient interferences can be easily coupled with the intelligent electrical meter communication interface through the outdoor cable [9], which will damage the instrument. When the communication interface chip could not able to provide sufficient protection capability under those circumstances mentioned above, the Transient Voltage Suppressor (TVS) arrays on board are the best choice for protection. TVS device provides a highly efficient surge current resistance method at the PCB level. With proper design, the TVS device can play a role of transient surge protection device as well as ESD protection device. Transient Voltage Suppressors (TVS) are nonlinear device and can clamp the ESD voltage to safe level and divert the ESD current to ground [10]. TVS are effective and have low cost than isolation program [11]. [12] shows an ultralow capacitance value and makes it well suited for high-speed system applications. [13] presents that the introduced TVS diode can increase failure of the low-noise amplifier. [14] discloses an integrated circuit wherein a transient voltage suppressing (TVS) circuit for suppressing a transient voltage. An interconnection improved complementary SCR is first introduced [15]. The TVS diodes are better placed close to the chip under stress. For example, the TVS device is copackaged with the IC in some circumstance. [16] proposed a co-design with TVS and CAN bus transceiver in CAN bus applications. Generally, the TVS is always placed at the PCB interface and maybe far away to the chip for certain considerations. However, significant surge current and ESD current may couple to the wire between the TVS and the vulnerable chip. However, significant surge current and ESD current may couple to the wire between the TVS and the vulnerable chip. In some cases, there was no space to place TVS due to limited PCB area. In other circumstances, TVS diodes are not used because of cost issues. What is more, the off-chip TVS may not fully cover the signal range of the circuit. TVS device embedded in the RS485 transceiver IC can help solve these problems and minimize the PCB size.

This paper proposed a new TVS device structure and a novel electrostatic discharge method. The TVS, which is integrated into the RS485 transceiver IC without extra process mask and modification, discharge the static electricity together with the RS485 transceiver IC output driver circuit. The driver circuit occupies a large part of the chip area, through a reasonable design of the trigger voltage; the driver not only provides the circuit function, but also has the ability to discharge large ESD currents. Parasitic capacitance is the key parameter of an ESD device. [17] proposed a new ESD protection design for highspeed I/O applications in nanoscale CMOS process. By properly setting the on chip TVS(OCT) device, the impact of board parasitic can be reduced and meet the design specifications of chip simultaneously. The OCT and the output driver circuit not only cooperate well to discharge the static electricity but also keep well commutation functional under the common-mode input range over -7V to 12V [18]. The date rate of this transceiver is up to 500kbps, and it can be applied to the severe noise distributed system.

STRUCTURE OF THE CHIP

Fig 1 shows the application scheme of the RS485 transceiver chip. There are three parts in the system: RS485 transceiver chip, off-chip TVS device, and RS485 bus. A and B are the bus communication ports. Because the signal range of A and B ports is -7 ~ 12V, a bidirectional TVS array should be applied to the system. The off-chip TVS device is connected between terminals A/B and GND. It is better to place the off-chip TVS close to the chip. Always, the TVS is kept away from the chip for the practical layout floor plan of PCB and other layout instructions, which increase the parasitic parameter. When the interrupt impulse irrupts on the PCB wire between the off-chip TVS and the vulnerable chip, large PCB area and parasitic effects lead to a long response time, and the chip may be damaged before the off-chip TVS turn on.

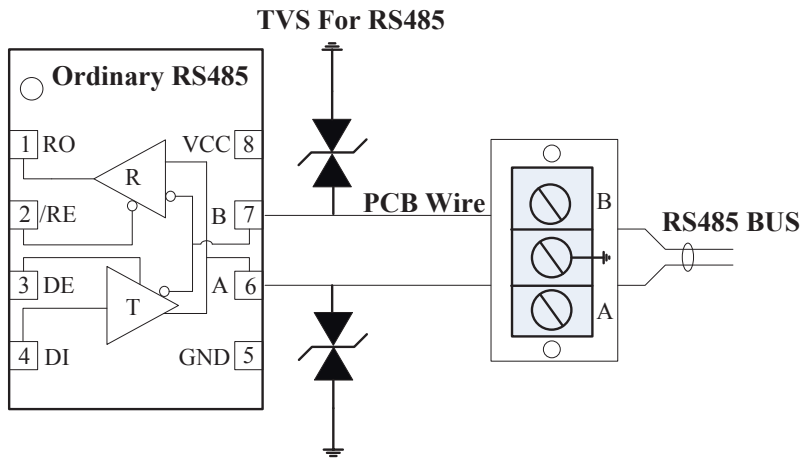

Figure 1. The application scheme of the RS485 chip with off-chip TVS.

Fig. 2 illustrates the structure of the RS485 chip with OCT. The chip consists of three parts, receiver, driver and OCT. The chip is based on half-duplex transmission mode, ports A and B act as bidirectional terminals: the receiver's inputs and the transmitter's outputs. OCT devices are coupled between A/B and GND. The A/B inputs of the receiver are configured with a 100K Ω resistor in series, respectively. The ESD current injected into the receiver is very weak. So, we focused on the protective capability of the driver. Terminal /RE and DE are the enabling ports of receiver and transmitter, respectively. Terminal RO is the receiver's output port, and terminal DI is the transmitter's input port. Compared with the RS485 chip without OCT, it has the following advantages. First, there is no need to worry about the distance between the off-chip TVS and the RS485 chip. Second, it has a stronger ESD protection capability. Thirdly, the off-chip TVS may be eliminated in many RS485 application areas, as shown in Fig 2; not only the PCB area is minimized, but also the cost of off-chip TVS is cut off. The RS485 chip with the OCT is more suitable for ESD interrupt environments.

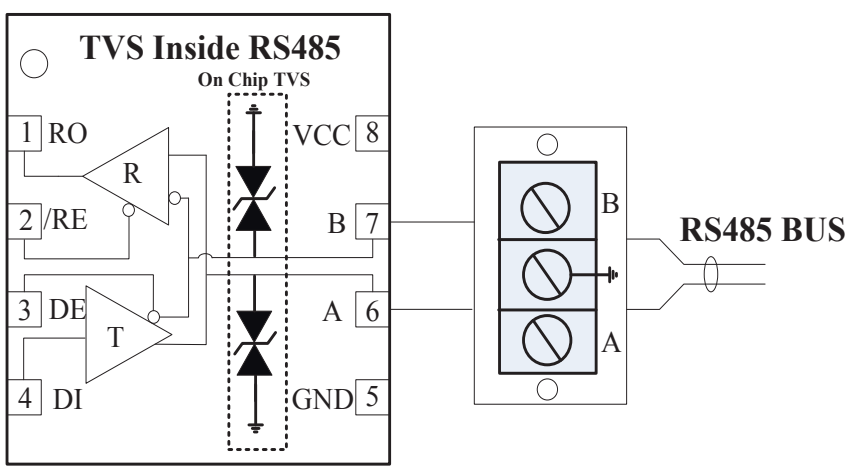

Figure 2. The structure of the RS485 chip with OCT.

OCT DESIGN

Design of the TVS Device's Window

For a RS485 chip, TVS protects the data transmission interface pins A and B. Their signal voltage ranges form -7V to 12V, so a dual-direction TVS device is required for A/B ports. The ESD design window of a nonsnapback diode is shown in Fig 3. VTV is the trigger voltage, which is set at about 1.2 times of 12V. VCMAX is the TVS's maximum clamping voltage, while the clamping current reached its peak value Ipp.

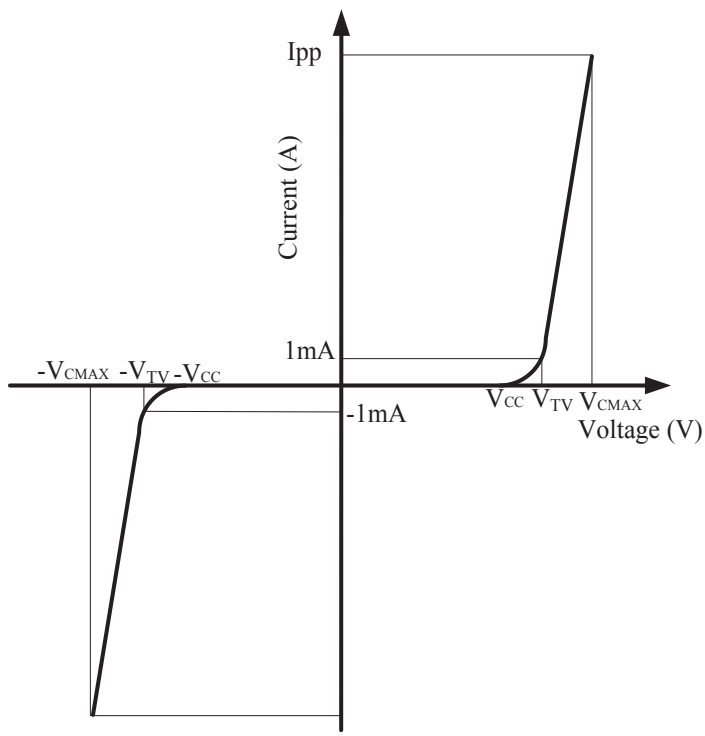

Figure 3. The ESD design window of the TVS device.

It is much tough to design a silicon-based on-chip TVS than that of an off-chip TVS. For one thing, the process of RS485 transceiver IC may lack the appropriate process layer or process modification method for OCT [19]. For another thing, the ESD ability of the RS485 output driver should be taken into consideration at the same time. What is more, the layout and the position of the OCT must be placed appropriately; when an ESD event occurs, it cannot affect the normal signal of the RS485 bus. The connection of the TVS device and the output driver is shown in Fig 4. MOSFETs M0 to M5 in the shadow area constitute one of the RS485 IC output drivers, such as the driver of port A. The MOSFETs are LDMOS structure [20]. This design proposed a novel electrical-static discharge method, and the OCT and the RS485 output driver cooperate well to protect the whole chip. The new design forms two protective barriers: one is the on-chip TVS devices, which are coupled between A/B and GND, and the other is the output driver, part of the RS485 transceiver IC, acting as ESD device simultaneously

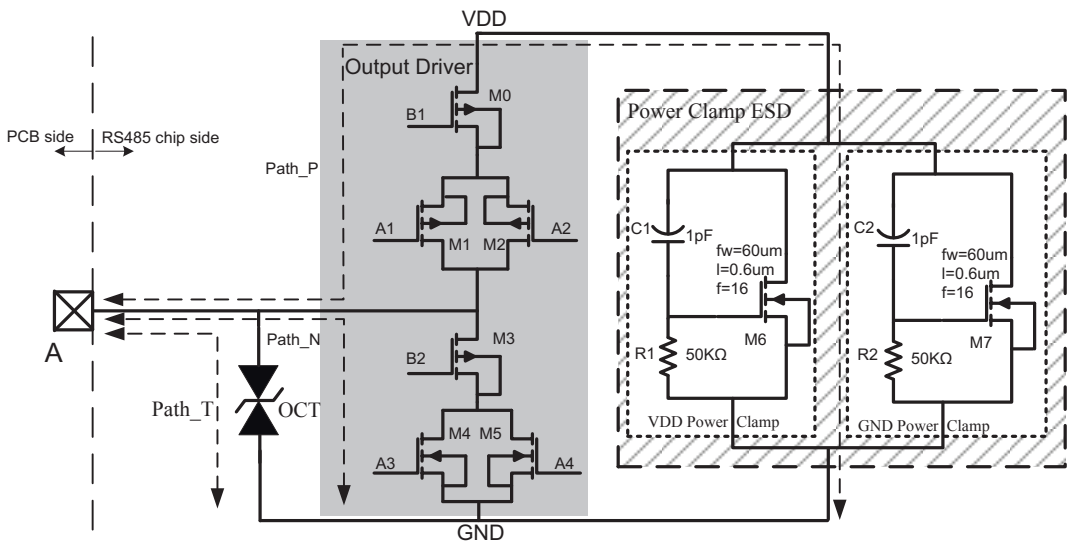

Figure 4. The protection scheme of the OCT design.

Through a rational design, the output driver circuit and OCT device can fit well to deal with the two barriers mentioned above. When the transient overvoltage strikes port A, the OCT turns on and discharges large current at first. If the transient overvoltage is large enough, the output driver, acting as an ESD device, turns on later to discharge the current together with the OCT. The current discharge path is illustrated in Fig 4. When a large enough transient overvoltage strikes, the discharge paths is first Path_T, then Path_N, and finally Path_P. The second breakdown voltage of the OCT for the forward direction should be higher than the trigger voltage of the Path_N and Path_P.

As the signal ranges of A/B cover from -7V to 12V, the 18V LDMOS are chosen to make up the output driver from the standard 5V/18V/24V 0.5μm CDMOS process. In order to save the chip area, LDMOS adopts asymmetric structure. The source to drain trigger voltage of the LDNMOS and the LDPMOS is measured to be 45.3V and 36.9V, respectively, and the trigger voltage of the power clamp ESD is 12.6V. Then, we can calculate the positive trigger voltage of the Path_N and Path_P is 45.3V and 49.5V, respectively. According to the specification, the VTV of the OCT should be about 14.4V. For the positive direction, VCMAX of the OCT should be designed higher than 45.3V at least. And for the negative direction, should be higher than 36.9V. Take the positive direction as an example. When a ESD pulse stress is at the A port, the Path_T turns on and discharges the ESD current first; when the pulse is large enough that the voltage of Port A rise up to 45.3V, the Path_N turns on and discharges the ESD current along with Path_T to protect the whole chip. So, the OCT device and the driver circuit cooperate well to protect the RS485 chip.

Equivalent Circuit Diagram of the TVS Device

As mentioned above, it is troublesome to design an OCT device, and it is more challenging to design an OCT device, which is fully compatible to that of the RS485 transceiver IC without extra process modifications [19]. Compared to some related designs, salicide blocking and ESD implantation modifications have been added into the processes to increase the robustness [21]. This proposed OCT is fabricated without extra process modification, which saves the fabrication cost and shortens the production cycle.

The existing standard process limits the choice of OCT architecture. In this paper, the zener diodes, whose forward voltage is 0.8V, and breakdown voltage is 6.3V, are used to construct the TVS device. Since 6.3V is below 12V, it is necessary to raise the trigger voltage by connecting the zener diodes in series. The equivalent circuit diagram of TVS device is shown in Fig 5.

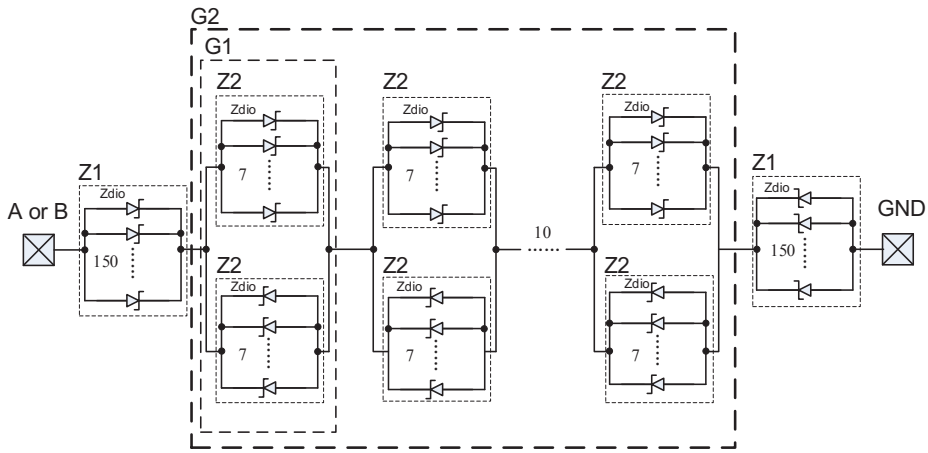

Figure 5. The equivalent circuit diagram of the TVS device.

The ESD pulse strikes from two directions; therefore, in order to ensure the reliability, the TVS device is designed symmetrical regardless of whichever direction the ESD strikes. It can be seen from Fig 5 that Z1 is made up of 150 paralleled zener diodes Zdio with the N+ base size of 10μm×10μm. Z2 consists of 7 paralleled Zdio. Z2 is coupled in an end to end configuration to compose group G1. Ten G1 groups are coupled in series to make up group G2. The TVS consists of a forward Z1, a G2 and a reverse Z1 connected in series configuration. Terminal A/B is coupled through TVS to terminal GND. Take the positive direction as an example; the TVS's breakdown voltage VTV is the Z1's reverse breakdown voltage plus 10 forward turn-on voltage and Z1's forward turn-on voltage, that is, about 15.1V.

Evaluation for the OCT

The OCT has been fabricated in the 0.5μm BCD process. Fig 6 illustrates the die photo of TVS device.

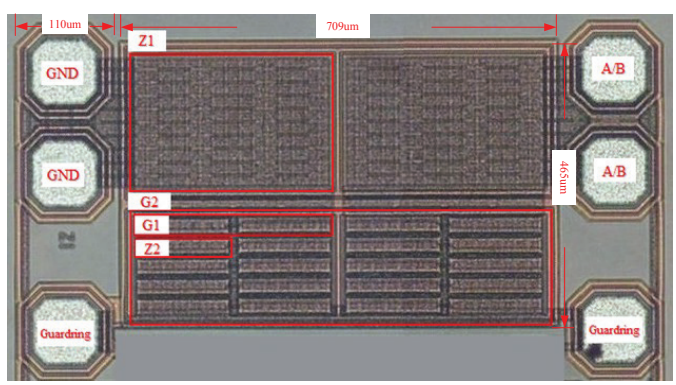

Figure 6. The die photo of TVS device.

As the Fig 6 depicts, the layout is symmetric and occupies an area of 709×465μm^2. The two zener diodes Z1 are located at the upside of the photo, and the zener diodes group G2 is located at the underside of the photo. The two pads A/B are anode side, and the two GND pads are cathode side. It is obvious that the layout is very symmetrical and is suitable for the signal range of the chip.

The OCT has been evaluated by TLP system of a 100ns pulse width. Fig 7 is the TLP I-V curve of the OCT device. For positive pulse, the OCT has been measured to 10.89A without any leakage current greater than 10^{-5}A. Its positive trigger voltage is 13.33V, which is above 12V and close to 14.4V, and it is greater than the maximum signal level and can be safely applied to the bus terminal of RS485. For reverse pulse, the OCT has been measured to -12.78A without any leakage current greater than 10^{-5}A. Its reverse trigger voltage is -13.10V, and its absolute value is greater than the maximum signal level and can be safely applied to the bus terminal of RS485. Its forward maximum clamping voltage is 47.39V, which is higher than 45.3V, and reverse maximum clamping voltage is -45.8V, and the absolute value is higher than 36.9V. It can be seen from figure 7 that the OCT device's IV curve is basically symmetric. The OCT works closely with the output drive to protect the RS485 transceiver.

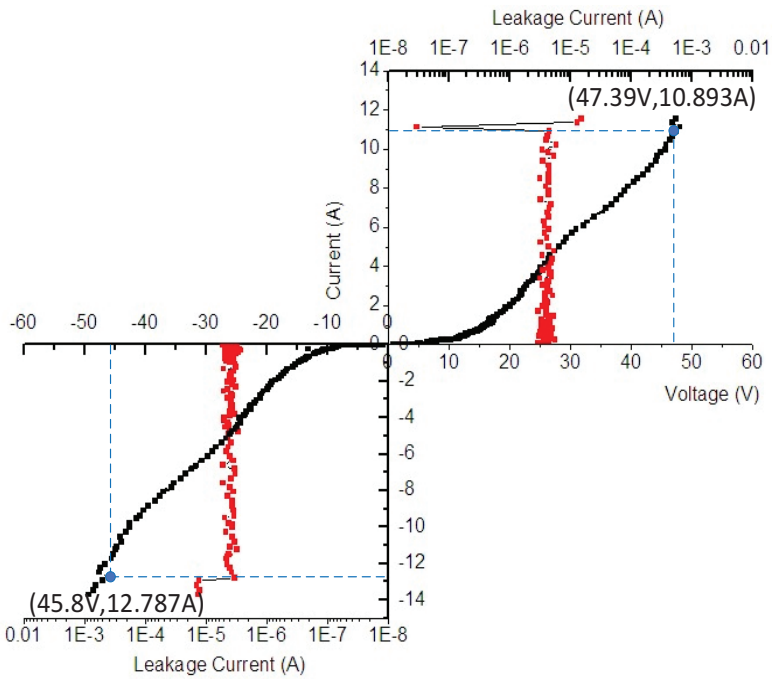

Fig 7. The TVS device's TLP test I-V curve.

The TLP test results of the TVS device are listed in table 1. The bias voltage is 13.2V when the leakage current is measured. Although the layout has perfect symmetry, the OCT's reverse trigger voltage is not exactly the same as the positive trigger voltage. The positive trigger voltage is 13.33V, and the reverse trigger voltage is 13.10V, which is due to the following reasons. The first reason is the discontinuity of semiconductor material and the inconsistency of the fabrication process. The second reason is the asymmetry of the TLP test instrument and a certain degree of measurement error. As the working voltage of A/B is -7V~12V, the asymmetry will not affect the normal work of the RS485 chip. Once the voltage of A/B ports transcends the trigger voltage, the OCT device will turn on and discharge transient overvoltage energy. The device protection level of human-body-model (HBM) is 16.34kV for the forward direction and -19.18kV for the reverse direction.

Table 1. The ratio of the wavelength (L) to the different riser's diameter (D).

Test items	Results (forward direction)	Results (reverse direction)
Trigger voltage (V)	13.33	13.10
Maximum clamping voltage (V)	47.39	45.80
Maximum clamping current (A)	10.893	12.787
Equivalent HBM voltage (kV)	16.34	19.18

SILICON CHIP AND TEST RESUILTS

The Silicon Chip

The chip is fabricated in a 0.5μm CDMOS process and the power supply voltage is 5V. It occupies an area of $2400\times1165\mu m^2$ including the OCT and pads. A chip micrograph is shown in Fig. 8. The layout of the OCT is at the periphery of the chip. The layout of the RS485 transceiver IC, including the driver circuit, is in the middle of the chip. The OCT should be well positioned, too. Since the transient voltage is injected to pins A and B, the OCT should be placed closed to ports A and B to reduce the length distance of current path. The locations of B PADs are away from the GND PAD as compared to the location of A PADs for floor plan and package consideration. In order to minimize the location effect, we increased the width of the main metal trace of the GND to 66.5 um, and two metal layers are used along the path except the place where there is a jump. Besides, this will reduce the current crowding effect to enhance the efficiency of the ESD current discharging. Also, in order to enhance the uniformity of the fingers, a double PAD structure is adopted, and the two pads are both used for bonding in the chip packaging, which can enhance the ESD capability and further minimize the location effect. Octagonal shape pads are used, and the area of the PAD is larger than that of the ordinary PAD.

System Verification for RS485

Figs 9–11 show the IEC61000-4-2 contact and IEC61000-4-4 EFT test scheme. There are two electrical meters equipped with the DUT RS485 transceiver chip, an electrostatic discharge generator and an electrical fast transient generator in the scheme. The A and B ports of the RS485 chip are connected to the outer terminals of the DUT meter case to perform the tests

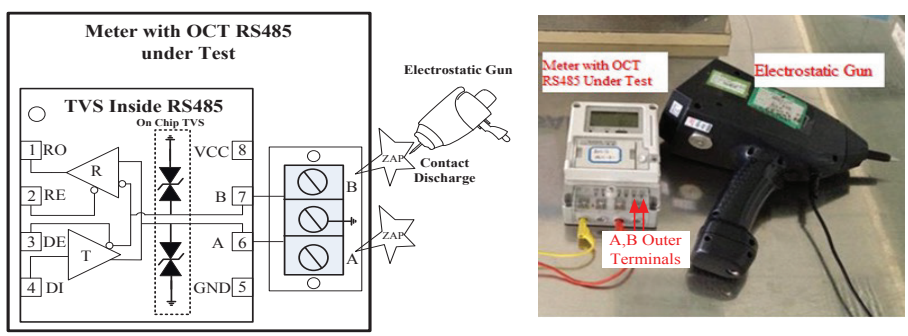

Figure 9. The IEC61000-4-2 contact test system.

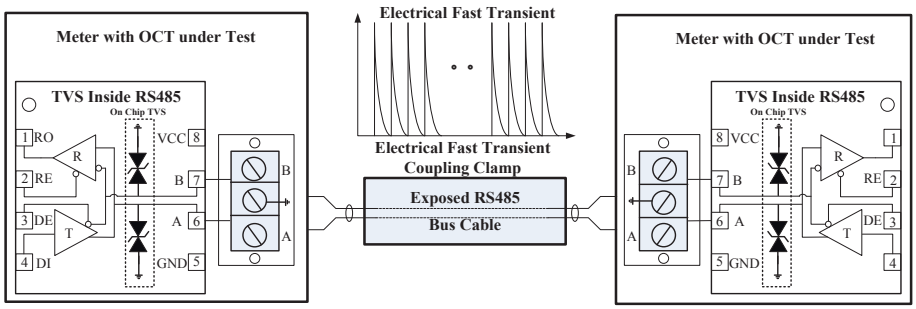

Figure 10. The IEC61000-4-4 EFT test system sketch map.

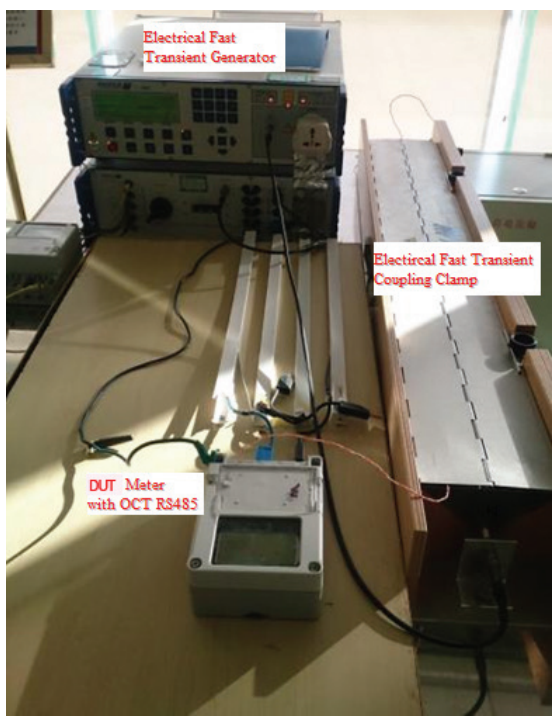

Figure 11. The photo of IEC61000-4-4 EFT test system.

Ports DE and RE of one chip are set high state to ensure only the transmitter works, and ports DE and RE of the other chip are set low state to ensure only the receiver works. The electrostatic discharge gun will zap the ports A and B of RS485 chip to evaluate the capability of the OCT. The A and B ports of the two DUT (device under test) chips are connected by the transmission cable separately. After the chips were attacked by IEC61000-4-2±10kV contact discharge, an IEC61000-4-4±2.2kV, 100KHZ EFT is coupling to the transmission cable.

The chip in one electricity meter transmits the real-time date at rate of 500kbps, which will be received by the chip in the other electricity meter. During the experiments, there is a little bit error; however, it can be back to normal when the ESD and EFT pulses disappeared.

After the above two experiments, the waveforms of the DUT chips are observed by an Oscilloscope. Through comparing the input and output signals of the chips, the communication state of the chips can be checked. Fig 12 shows the waveform of the input and output signal of the two chips. The bottom one is the input signal of the master chip, and the upper one is the output signal of slave chip.

From the results, it can be seen that the output signal of the slave chip is almost the same as the input signal of the master chip except some time delays. To sum up, the RS485 transceiver with OCT has been verified to be no hard damage and latch up issue to pass IEC61000-4-2±10kV contact discharge and IEC61000-4-4±2.2kV, 100KHZ EFT test.

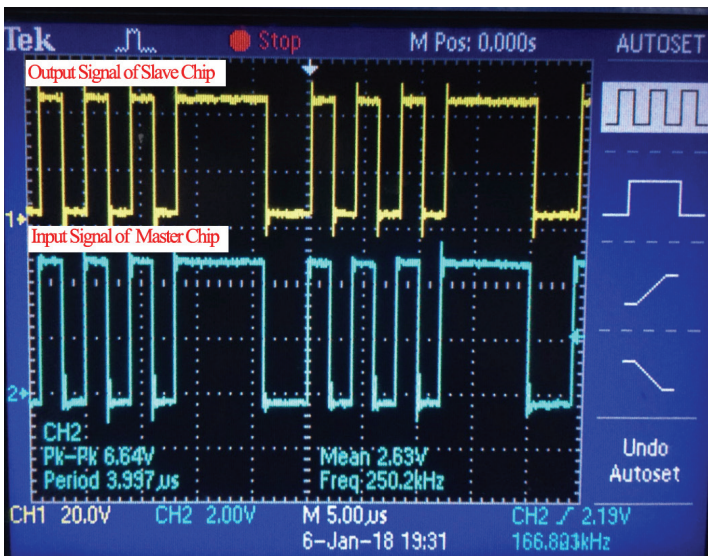

Figure 12. Waveforms of the input of master chip and the output of slave chip.

CONCLUSION

The RS485 transceiver chip with OCT has been introduced in this paper. It is evaluated with a 100ns pulse width TLP system. The positive trigger voltage and the reverse trigger voltage of the OCT are 13.33V and 13.10V, respectively. The trigger voltage is compatible with the signal level of the RS485 standard. The maximum positive and negative clamping currents are 10.893A and 12.787A, respectively. And the positive and negative HBM of Chip are 16.34kV and 19.18kV in 2.4×1.17mm2 layout area. The transceiver IC integrated with the OCT has been verified to be a workable solution, and its date rate is up to 500kbps. The chip on the smart meter has been evaluated to pass the IEC61000-4-2 contact ±10kV stress and IEC 61000−4−4 EFT ±2.2kV without any hard damages and latch-up issue.

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