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A new generalized cross-connected switched capacitor multilevel inverter topology with high output voltage gain for single phase solar PV unit

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ABSTRACT

Switched capacitor multilevel inverters are gaining much attention these days due to their merits like voltage boosting and voltage balancing characteristics. A Cross Connected Switched Capacitor Multilevel Inverter (C^2SC-MLI) topology is proposed in this work. It can synthesize thirteen levels in the terminal voltage waveform and with a voltage boost ratio of 1:3. The topology is extendable by adding additional "n" modules in series. The number of levels (N_{Level}) and the voltage gain can be increased up to 4i+9 and 1:(i+2) respectively by connecting 'i' such 'n' modules. The topology also has inherent voltage balancing ability. To prove the advantage of proposed topology it is compared with recent switched capacitor multilevel inverter topologies and conventional multilevel inverter topologies in terms of number of power electronic components required, cost and voltage gain. The performance of proposed topology is validated using simulation in MATLAB and with an experimental prototype rated 0.1 kW fed by a solar PV emulator under steady state and dynamic loading conditions.

Keywords: Multilevel inverter; Voltage boosting; Switched capacitor; Voltage balancing.

INTRODUCTION

With the continuous rise in penetration of renewable energy sources and modern technologies like smart electric vehicles, the role of power converters has become vital (Sudheer & Venkata 2017; Dalcal, A., & Akbaba, M. 2018). The conventional two-level converters suffer from setbacks like poor power quality and high voltage stress (Guo et al., 2016; Kalyan & Srinivasa, 2017). The multilevel inverters are gaining wider attention due to their advantages like improved power quality and reduced voltage stress (Franquelo et al, 2008; Hirofumi 2017). The multilevel inverters synthesize high voltage staircase form by accumulating several low voltage dc sources controlled by switches connected to those sources. The rating of these switches is based on the rating of the voltage source to which it is

connected (Gupta et al, 2015; Prem & Sivaraman 2017). Therefore, a high voltage output can be achieved using low voltage components, thus reducing the voltage stress across the switches. Higher the number of steps in the staircase waveform, higher will be the power quality (Thiyagarajan & Somasundaram, 2019). Starting from Neutral Point Clamped Multilevel Inverter (NPC-MLI) proposed by (Nabae, Takahashi & Akagi, 1981), the other two conventional multilevel inverter topologies developed are Flying Capacitor Multilevel Inverter (FC-MLI) and Cascaded H-Bridge Multilevel Inverter (CHB-MLI) topologies (Baker, 1981; Meynard & Foch, 1992). Diodes are used to clamp the voltage in NPC-MLI and capacitors replaced the diodes in FC-MLI. The rising number of diodes with the increase in number of steps in the staircase waveform is the setback of NPC-MLI and the voltage balancing issue is the lacuna of FC-MLI (Junfeng, Cheng & Ye, 2014). The CHB-MLI with its modularity and less control complexity gained wider attention in the application of renewable energy generation. But it requires multiple independent voltage sources. The addition of every independent voltage source has to be supported with four switches to control it (Prem et al 2019; Sandeep et al 2019). This drastically increased the size and cost of the circuit (Kangarlu & Ebrahim, 2013). Further the above three topologies cannot boost the voltage fed at their input, which is one of the primary requirements in renewable power conversion (Rahim et al, 2011), further the voltage balancing requirement reduces the reliability of the circuit due to the deployment of higher number of passive components. So, the recent research is focused on reducing the number of power components in H-Bridge based topologies and to incorporate an inherent voltage boosting and self-balancing ability in it. Hybrid Multilevel Inverters formed by combining H-Bridge and NPC-MLI or H-Bridge and FC-MLI are developed to address the issue of component reduction (Silva & Espionza 2010; Alishah et al 2015; Liu et al 2008) by using floating capacitors in the place of independent dc sources. The voltage tracking of these floating capacitors requires complex circuitry and high frequency switching scheme to ensure voltage balance between the capacitors. This increase cost of the circuit (Junfeng et al 2019, Sandeep et al. 2019). In the Hybrid multilevel inverter topology proposed in (Liu et al, 2008), the number of switching components increase drastically at higher number of levels. Switched Capacitor Multilevel Inverters have capacitors connected in series/parallel combination to the voltage source to synthesize multiple levels in the output voltage and a H-Bridge cell before the load for polarity reversal (Mak & Ioinovici 1998). A multilevel inverter using the above concept is presented in (Hinago & Koizumi, 2012), but the number of IGBTs employed is high. The topology proposed in (Ye et al, 2014) lacks the ability to accommodate reactive loads. The voltage gain of the high frequency Switched Capacitor Multilevel inverter suggested in (Zeng et al, 2017) is its setback even though it is capable of synthesizing multiple voltage levels with lee components. The switched capacitor topologies suggested in (Junfeng et al 2017; Barzegarkhoo et al,2018) can provide only nine levels with 200% voltage boost but cannot be extended beyond nine levels. Further in the topology suggested in (Barzegarkhoo et al,2018), The blocking voltage across the polarity changing switches is double that of input voltage which make its deployment questionable for high voltage requirements. The single stage switched capacitor module suggested by (Sze, 2018) reduces the standing voltage across the H-Bridge switches but it can provide only a fixed voltage boost irrespective increased number of modules and requires higher number of switches while cascading. A single-phase single source seven level inverter topology presented in (Sze 2018a), it offers a voltage boost of 300 % but the author has not dealt with topology expansion. In the switched capacitor topology discussed in (Khoun, Abapour & Zare, 2019), for the synthesis of every two levels a basic unit has to be added continuously which results in bulky circuit thus increasing the cost. In this paper a switched capacitor multilevel inverter topology formed by hybriding the concept of conventional SC-MLI and Hybrid MLI topologies is proposed. The salient features of the topology are as follows

- The topology can synthesize a staircase wave form with thirteen levels (Six positive, Six negative and a zero level), with 14 switches
- It can offer a voltage boost of 1:3 and it increases by two for the addition of every ‘n’ module in series.
- The capacitors used in the topology are self-balancing in nature and hence the necessity of voltage balancing circuit is nullified.

CONSTRUCTION AND SWITCHING STATES OF C²SC-MLI

A basic module with a source and two capacitors is connected to an 'n' module with a capacitor to form the proposed MLI topology as shown in Fig.1. The 'n' module shown here is a H-Bridge with a switched capacitor and an IGBT connecting the H-Bridge to the Basic module. With the basic module fixed, any number of such 'n' modules can be connected in series based on the desired number of levels to be synthesized in the terminal voltage waveform. To demonstrate the concept and application of the C²SC-MLI a 13-level prototype has been developed as shown in the Fig.1. A solar PV unit, battery, fuel cell or a rectifier connected to the terminals of a wind generating unit can act as a source feeding the basic module shown in Fig.1. Other than the source, the basic module has two clamping capacitors C_1 and C_2 connected to it to synthesize levels in the voltage waveform and to deliver voltage boost along with the capacitor C_3 connected in the 'n' module.

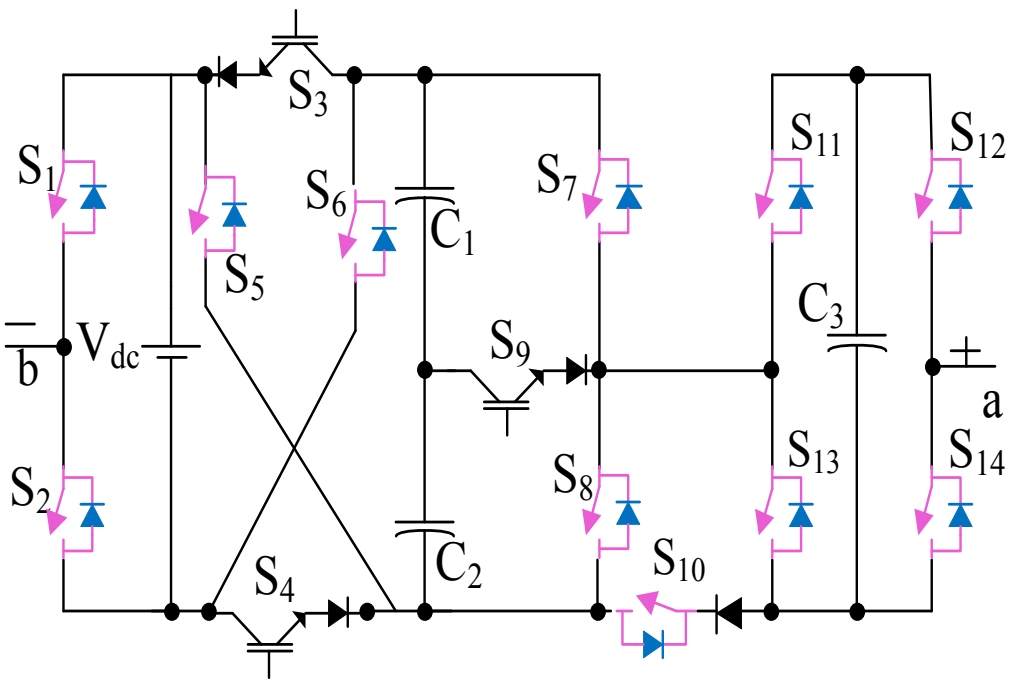


Figure 1. 13 level prototype of C²SC –MLI

Apart from the capacitors, there are nine IGBTs in the basic module and five IGBTs in the 'n' module. The working of the prototype can be understood using the switching states depicted in Table 1 and the conduction path diagrams shown in Fig.2. In Table 1 the first column 'L' indicates the level number. That is the output voltage is zero during level 0. At level 1 the terminal voltage is $+0.5V_{dc}$, it is $+V_{dc}$ at level 2 and increment by $+0.5V_{dc}$ until $+3V_{dc}$ at Level 6. Similarly, from Level 7 to Level 12 it increments by 0.5 from $-0.5V_{dc}$ at Level 7 to $-3V_{dc}$ at level 12. Here 'V_{dc}' is the magnitude of voltage delivered by the independent dc voltage source in the basic module shown in Fig.1. The conduction path for synthesizing the levels 0, $\pm V_{dc}$, $\pm 2V_{dc}$ are shown in the Fig.2.

Table 1. Switching States of C^2SC-MLI for synthesizing 13 levels

L	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}
0	0	1	1	1	0	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	0	0	0	1	0	1	1	0	0
2	0	1	1	1	0	0	1	0	0	0	1	1	0	0
3	0	1	0	0	1	0	0	0	1	0	1	1	0	0
4	0	1	0	0	1	0	1	0	0	0	1	1	0	0
5	0	1	0	0	1	0	0	0	1	0	0	1	1	0
6	0	1	0	0	1	0	1	0	0	0	0	1	1	0
7	1	0	1	1	0	0	0	0	1	0	0	0	1	1
8	1	0	1	1	0	0	0	1	0	0	0	0	1	1
9	1	0	0	0	0	1	0	0	1	0	0	0	1	1
10	1	0	0	0	0	1	0	1	0	0	0	0	1	1
11	1	0	0	0	0	1	0	0	1	0	1	0	0	1
12	1	0	0	0	0	1	0	1	0	0	1	0	0	1

These five levels are explained in particular because the capacitors C_1 to C_3 gets charged simultaneously while the inverter is delivering required voltage at the terminals.

0 V_{dc} : The zero state in the inverter aids the circuit to circulate the inductor current, thus preventing voltage spikes when inductive loads are used. The conduction paths in the circuit during this state of operation shown in Fig.2a. Here, the inductive current gets circulated with in the path "*a-Load-b-S_2- S_4- S_{10}- S_{14}"*. Further, the capacitors C_1 and C_2 gets charged through the path *"Source--S_3- C_1-C_2 S_4"*. Similarly, the capacitor C_3 gets charged through *"Source-S_3-S_7-S_{11}-C_3-S_{10}-S_4"*.

$\pm V_{dc}/2$: This is the first step in the positive/negative cycle in the staircase voltage waveform. The source voltage V_{dc} is clamped across the capacitors C_1 and C_2 as $0.5V_{dc}$ each. The load gets a voltage of $+V_{dc}/2$ through *"b-S_2-S_4-C_2-S_9- S_{11} -S_{12}-a-Load-b"* as shown in the Fig.2b. Corresponding negative voltage step $-V_{dc}/2$ can be obtained in a similar way through the path "*b-S_1-S_3-C_1-S_9- S_{13} -S_{14}-a-Load-b"*as shown in Fig.2c. While synthesizing above positive and negative voltage steps, the capacitors C_1 and C_2 gets charged through the path *"Source--S_3- C_1-C_2 S_4"*.

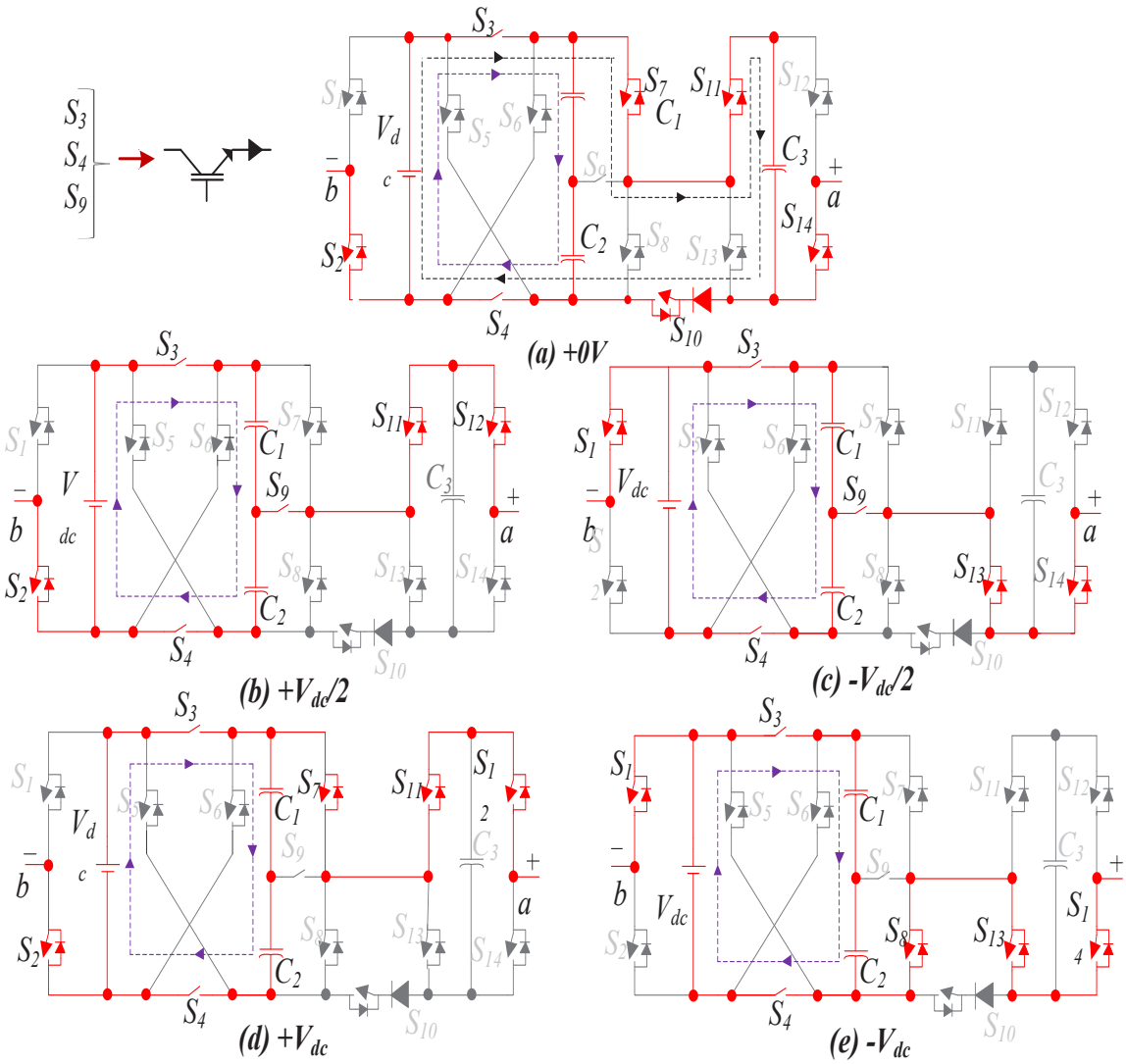


Figure 2. Operation of C^2SC –MLI

$\pm V_{dc}$: This is the second step in the positive/negative cycle in the staircase voltage waveform. The source voltage V_{dc} is clamped across the capacitors C_1 and C_2 as $0.5V_{dc}$ each. The load gets a voltage of $+V_{dc}$ through *"b-S_2-source-S_3-S_7- S_{11} -S_{12}-a-Load-b"* as shown in the Fig.2d. Corresponding negative voltage step $-V_{dc}$ can be obtained in a similar way through the path "*b-S_1-source-S_4-S_8-S_{13}-S_{14}-a-Load-b"* as shown in Fig.2e. While synthesizing above positive and negative voltage steps, the capacitors C_1 and C_2 gets charged through the path *"Source-S_3- C_1-C_2 S_4"*.

PWM SCHEME

The switches in the HSC-MLI should be controlled using a suitable Pulse Width Modulation (PWM) scheme. There are PWM schemes like Phase shifted PWM, Level shifted PWM, Phase Opposition Disposition PWM, Selective Harmonic Elimination (SHE), Space Vector PWM etc., (Hinago & Koizumi, 2012). A level shifted PWM is employed in this topology to perform simulation and experimental analysis. The control scheme is shown in the

Fig.3. There are twelve carriers for twelve level excluding zero state. Six positive carrier signals C_{P1}-C_{P6} and Six negative carrier signals C_{N1}-C_{N6}. The reference wave is a sine wave whose peak magnitude should be set such that it is equal to the number of steps in one quarter cycle of an expected stair case output in the inverter terminal.

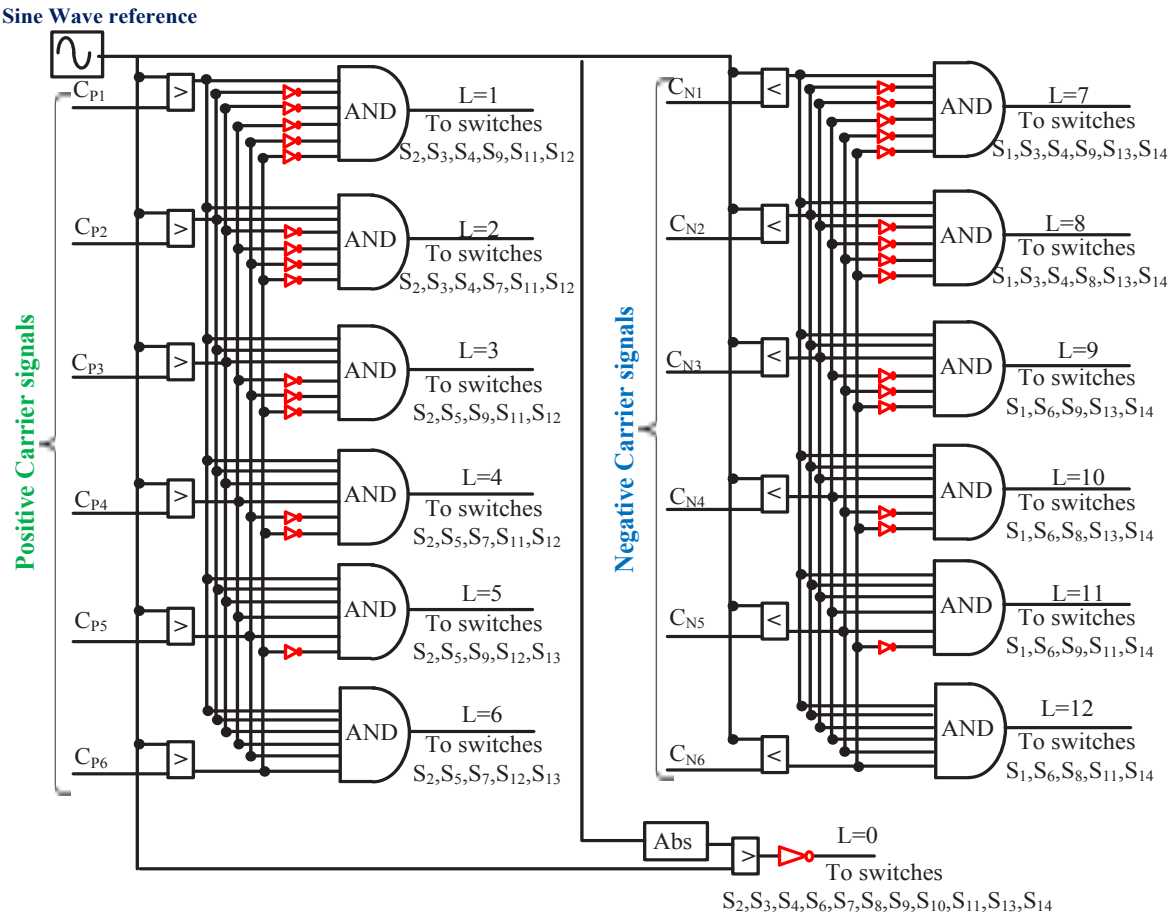


Figure 3. Schematic of the PWM control scheme

For thirteen level inverter, the number of steps in a quarter cycle will be six and hence the sine wave magnitude is 6V in positive half cycle and -6V in negative half cycle with the frequency equal to the frequency of terminal voltage. In this case it is 50 Hz.The circuit can be used for both fundamental frequency and high frequency switching. For high frequency switching the carrier C_{P1} should be chosen as a triangular wave (0,1,0) with a switching frequency 5kHZ and C_{P2} has to be shifted by one level (1,2,1) with the same switching frequency and so on. As for as the negative carriers are concerned C_{N1} = (0, -1,0), C_{N2} = (-1, -2, -1). To synthesize zero level, the absolute value of the reference to be compared with the minimum carrier and complimented. The gating signal to be given for the switch S_1 should be the output of an OR logic whose inputs are L=7, L=8…..L=12.

SELF-VOLTAGE BALANCING AT CAPACITORS

The equivalent circuit of C^2SC-MLI is shown in the Fig.4. In the Figure the resistance R_{ON} is the internal resistance of the switch, r_i is the internal resistance of the capacitors and R_D is the resistance of diode.

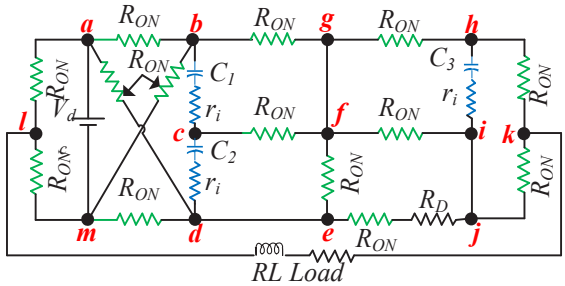


Figure 4. Schematic of the PWM control scheme

The voltage across a capacitor is said to be balanced if the average voltage across the capacitor over a cycle is zero (Alishah et al.2014). The self-voltage balancing ability of the C²SC-MLI is established by determining whether the voltage across the capacitors over a cycle is zero. With the assumption that the switches are ideal, From the switching state shown in Table 1 and Fig.2 it can be observed that C_3 is charged during the zero state and discharging during Level 5, Level 6, Level 11 and Level 12. The voltage at level 5 is $+2.5V_{dc}$ and the current through C_3 can be determined by applying Kirchoff's Voltage law in the loop "adcfihklma" of the equivalent circuit shown in Fig.4 as follows,

$$i_{c3}^{+}(at\ L=5) = -\left(\frac{V_{dc} + {V_{dc}}/{2} + V_{dc}}{Z}\right) \tag{1}$$

the current through the capacitor C_3 while synthesizing level 6 ($+3V_{dc}$) can be calculated by applying KVL to the loop "adcbgfihklma" of the equivalent circuit as follows

$$i_{c3}^{+}(at\ L=6) = -\left(\frac{V_{dc} + {V_{dc}}/{2} + {V_{dc}}/{2} + V_{dc}}{Z}\right) \tag{2}$$

By adding equations (1) and (2), the total current flowing through C_3 during positive half cycle will be

$$i_{c3}^{+}(net) = i_{c3}^{+}(at\ L=5) + i_{c3}^{+}(at\ L=6) = -\left(\frac{11{V_{dc}}/{2}}{2Z}\right) \tag{3}$$

Similarly, the current through C_3 during negative half cycle can be calculated by summing up the current through the capacitor during L=11 and L=12 by applying KVL across the loops "mdcfihklam" and "mbcdejihklam" respectively in the equivalent circuit shown in the Fig.4. The net current during negative half cycle thus found is

$$i_{c3}^{-}(net) = i_{c3}^{-}(at\ L=11) + i_{c3}^{-}(at\ L=12) = \left(\frac{11{V_{dc}}/{2}}{2Z}\right) \tag{4}$$

Therefore, the average current through the capacitor over cycle obtained by summing up equations (3) and (4) is zero. This validates the voltage balance across C_3. In the same way the net voltage across capacitors C_1 and C_2 can be proved as zero. Thus, the self-voltage balancing capability of C²SC-MLI is validated.

EXTENDED STRUCTURE OF C²SC-MLI

The C²SC-MLI can be extended to deliver more voltage levels by connecting additional 'n' modules in series as shown in the Fig.5. The voltage of the capacitors C_{n1}, C_{n2},……. C_{ni} connected in the first to i^{th} 'n' module is maintained as $+V_{dc}$. So that the maximum voltage across the switches in the 'n' module never exceeds the source voltage, thus limiting the switching stress.

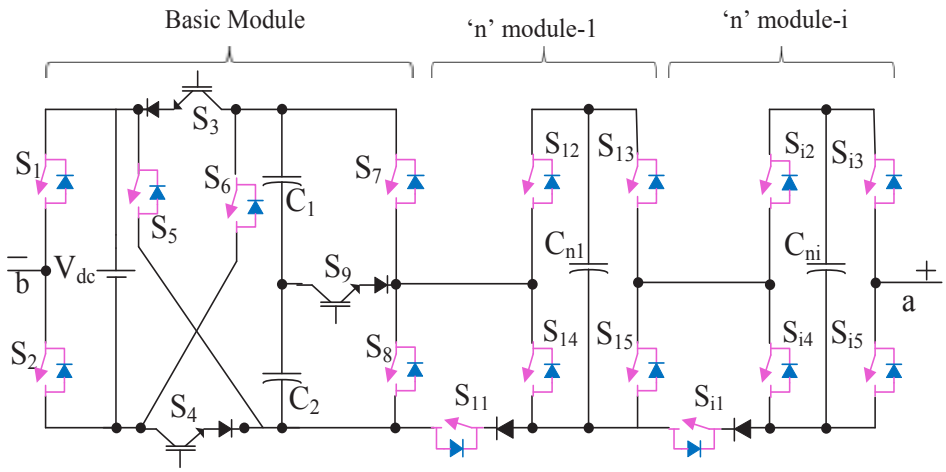


Figure 5. Extended Structure of C2SC-MLI

If 'i' is the number of 'n' modules connected in series with the basic module, The number of output voltage levels in the staircase waveform can be computed as in equation (5)

$$N_{level} = 4i + 9 \tag{5}$$

For synthesizing N_{Level} the number of IGBTs (N_{IGBT}) will be

$$N_{IGBT} = 5i + 9 \tag{6}$$

For controlling the above IGBTs, each IGBT require a driver circuit and hence

$$N_{driver} = N_{IGBT} \tag{7}$$

Apart from the IGBTs and drivers, the number of capacitors and diode required can be estimated using the equations (8) and (9)

$$N_C = i + 2 \tag{8}$$

$$N_D = k \tag{9}$$

On addition of a single 'n' module, the topology can deliver a voltage boost of 1:3, After the first module, the addition of further 'n' module will increase the boost gain by a factor of V_{dc}. Therefore, the voltage boost obtained using extended structure with 'i' such modules connected in series will be

$$V_{Boost} = i + 2 \tag{10}$$

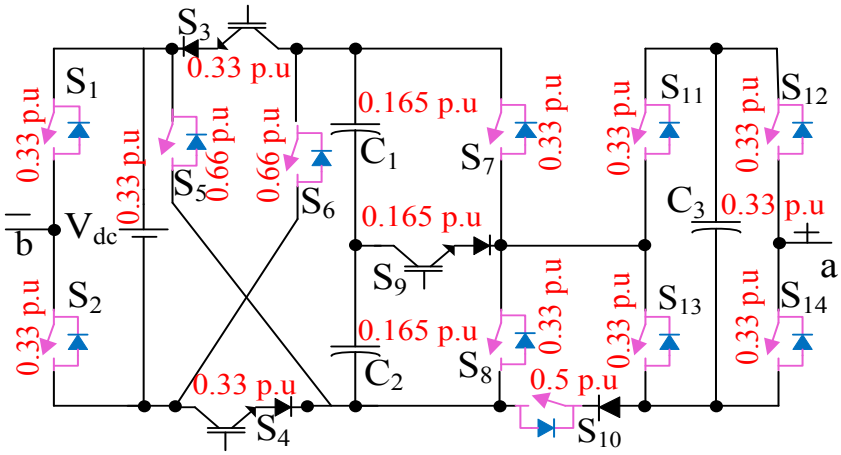


Figure 6. Standing voltage across the switches

A 13-level prototype delivers a voltage whose peak is three times that of the input dc voltage source. If the peak output voltage is taken as base value, the per unit value of input dc voltage is the ratio of input voltage to peak value of output i.e., 0.33 p.u. The voltage across the capacitors C_1, C_2 are 50% of the voltage across the input dc source which is 0.165 p.u. The voltage across the capacitor C_3 is equal to dc source voltage. Similarly, the voltage across the switches connected between the capacitors and sources can be estimated based on the conduction path they are involved. The per unit blocking voltage across each switch is shown in the Fig.6. From the figure the Total Blocking Voltage across the topology for thirteen level output is 5 p.u (if the peak voltage of output 60V is taken as base). For an extended topology with 'I' modules connected in series, the total blocking voltage can be estimated using the equation (11)

$$TBV = 3.18 + 1.82i\ p.u \tag{10}$$

The maximum blocking voltage of 0.66 p.u appears across the switches S_5 and S_6, therefore the ratio of maximum blocking voltage to peak voltage 1.pu is only 0.66 p.u which indicates the reduced stress across the switches. Using the equations (5-9), The number of IGBTs, capacitors and diodes for the given number of levels are computed and compared against the similar topologies and portrayed in Table 2. From the table it can be observed that the C^2SC-MLI requires few components when compared to other topologies considered for comparison. Further, all the above topologies can yield a maximum of 200% voltage boost, but the C^2SC-MLI can offer a voltage boost of 1:3 with a low maximum blocking voltage to peak voltage ratio of 0.66.

Table 2. Comparison of C^2SC-MLI with other topologies for synthesizing 13 Levels

Topology	Sources	IGBTs	Capacitors	Diodes	Drivers	Voltage boost
Sze 2018	2	24	4	-	20	1:2
Junfeng et al 2014	3	18	3	3	18	1:2
Alisha et al 2016	2	14	4	4	14	1:2
CHB	6	24	-	-	24	No Voltage boost
NPC-MLI	1	24	12	12	24	No Voltage boost
FC-MLI	1	24	27	-	24	No Voltage boost
Proposed	1	14	3	1	3	1:3

ESTIMATION OF EFFICIENCY

The efficiency of an inverter topology can be found by determining the ratio of output power to input power. Here output power can be calculated by measuring the terminal voltage and load current and the input power is the sum of output power and losses (Babaei, Alilu, & Laali, 2014). In a switched capacitor multilevel inverter, the net losses are the sum of conduction losses, switching losses, capacitor ripple losses and losses across the diode. These losses can be estimated as follows

Conduction Losses

The loss that incurred due to the current through the internal resistance of the IGBTs is called conduction loss. Using the first half cycle shown in the Fig.7 and switching sequence given in Table 1, based on the conduction period, voltage level and load current, the switches can be grouped as shown in Table3 for synthesizing levels other than zero states. The loss equation per switch in each switch group can be estimated based on the conduction current and conduction period as given in Table 3.

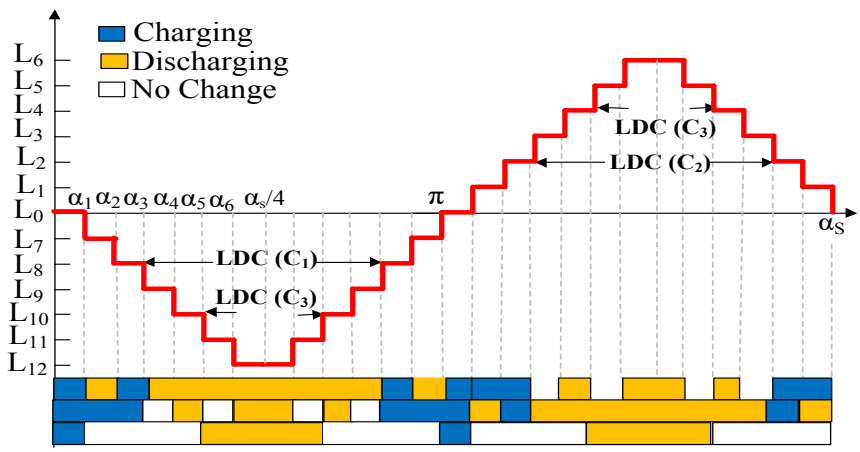


Figure 7. Capacitor charging and discharging cycle of capacitors

Table 3. Conduction losses estimation for different switch groups

Group number	Switches involved	Loss equation for individual switch P_i (i=group number)	Net losses in the switch group
1	S_1, S_2, S_{12}, S_{14}	$P_1 = \frac{1}{\pi}\int_{\alpha_1}^{\alpha_7} R_{ON} I_L^2 dt$	$4 \times P_1$
2	S_3, S_4	$P_2 = \frac{2}{\pi}\int_{\alpha_1}^{\alpha_2} R_{ON} I_L^2 dt$	$2 \times P_2$
3	S_7, S_8	$P_3 = \frac{2}{\pi}\left[\int_{\alpha_1}^{\alpha_3} R_{ON} I_L^2 dt + \int_{\alpha_4}^{\alpha_5} R_{ON} I_L^2 dt + \int_{\alpha_6}^{\alpha_7} R_{ON} I_L^2 dt\right]$	$2 \times P_3$

4	S_5, S_6	$P_4 = \frac{1}{\pi}\int_{\alpha_3}^{\alpha_7} R_{ON} I_L^2 dt$	$2 \times P_4$
5	S_9	$P_5 = \frac{2}{\pi}\left[\int_{\alpha_1}^{\alpha_2} R_{ON} I_L^2 dt + \int_{\alpha_3}^{\alpha_4} R_{ON} I_L^2 dt + \int_{\alpha_5}^{\alpha_6} R_{ON} I_L^2 dt\right]$	P_5
6	S_{11}	$P_6 = \frac{2}{\pi}\left[\int_{\alpha_1}^{\alpha_5} R_{ON} I_L^2 dt + \int_{\alpha_6}^{\alpha_7} R_{ON} I_L^2 dt\right]$	P_6

During the zeros state the switches S_2, S_3, S_4, S_7, S_{10}, S_{11} and S_{14} will be conducting and the net loss incurred during the zero state can be calculated using the equation (11)

$$P_0 = 2 \times \left[\int_0^{\alpha_1} (2R_{ON} + 2r_i) I_{C_{1/2}}^2 dt + \int_0^{\alpha_1} (4R_{ON} + r_i) I_{C_3}^2 dt + \int_0^{\alpha_1} R_{ON} I_L^2 dt\right] \quad (11)$$

The total average conduction loss incurred can be computed using the Table 5 and equation (12) as

$$P_{con-avg} = P_0 + 4 \times P_1 + 2 \times P_2 + 2 \times P_3 + 2 \times P_4 + P_5 + P_5 \quad (12)$$

Switching Loss

Based on the switching characteristics of a practical switch explained by (Rashid, 2017), The energy dissipated in a switch when it gets ON can be expressed as

$$E_{ON} = \frac{V_{ON} I_C}{6} t_{on} \quad (13)$$

Here V_{ON} is the voltage drop across the switch when it is ON, this will happen due to the internal resistance of the switch. I_{ON} is the current flowing through the switch when it is conducting, this will vary based on the level in which the switch is turned ON. T_{on} is the time taken for the IGBT to turn ON. Similarly, from the linearized switching model, the energy dissipated in a switch when it is turned OFF can be determined using the equation (14) below

$$E_{OFF} = \frac{V_{OFF} I_C}{6} t_{off} \quad (14)$$

Here Voff is the standing voltage across the switch when it is not conducting, this will be based on the source to which it is connected and toff is the time taken for the switch to turn off. The total switching loss per switching instant is the sum of equations (13) and (14). The average switching loss can be determined using the equation (15), here f is the frequency and 'n' is the number of switching instants per cycle.

$$P_{SL} = n \times 2f(E_{on} + E_{OFF}) \quad (15)$$

$$P_{SL-Total} = \sum_{i=1}^{14} P_{SL-i} \tag{16}$$

Capacitor Ripple Loss

The ripple voltage comes in to consideration when there is a difference between the the desired voltage at the capacitor and the actual voltage at that instant. It will be caused when the capacitor transits from discharging to charging state or vice versa (Barzegarkhoo et al, 2018). If i_{ck} is the current through the capacitor 'k' and C_k is the capacitance offered by the capacitor 'k', then the voltage ripple can be estimated as

$$\Delta V_{ck} = \frac{1}{2\pi f C_k} \int_{\alpha_m}^{\alpha_n} i_{ck}(t)dt \tag{17}$$

The total ripple loss is the sum of the losses incurred across the capactitors C_1 to C_3 and it can be expressed as

$$P_{R-L} = \frac{1}{2\pi} \sum_{k=1}^{3} C_k \, {\Delta V_{ck}}^2 \tag{18}$$

The total losses and efficiency are obtained by, equation (20), (Babaei, Alilu, & Laali, 2014),

$$P_{Loss} = P_{SL-total} + P_{Con-total} + P_{R-L} + P_{diode} \tag{19}$$

$$\eta = \frac{P_{out}}{P_{in} + P_{Loss}} \tag{20}$$

SIMULATION OF C²SC-MLI

A thirteen-level prototype of C²SC-MLI is simulated with Solar PV module fed dc-dc converter as an input voltage source delivering 20V. The capacitors clamped to the solar PV panel are rated as 10 V/4700 micro farad each.

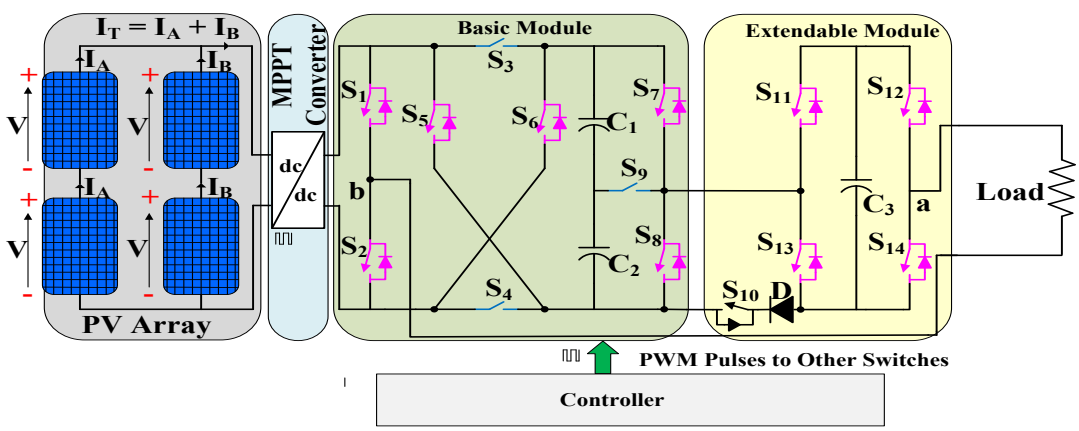


Figure 8. Standing voltage across the switches

The voltage across capacitor C_3 in the 'n' module is fixed as 20V with a capacitance of 4700 microfarad. An RL load with a Resistance of 50 ohm and an inductance of 50 mH is connected across the load terminals. The schematic of the simulation setup is shown in The Fig.8. The controller shown in the Figure 8 is Level shifted PWM based controller.

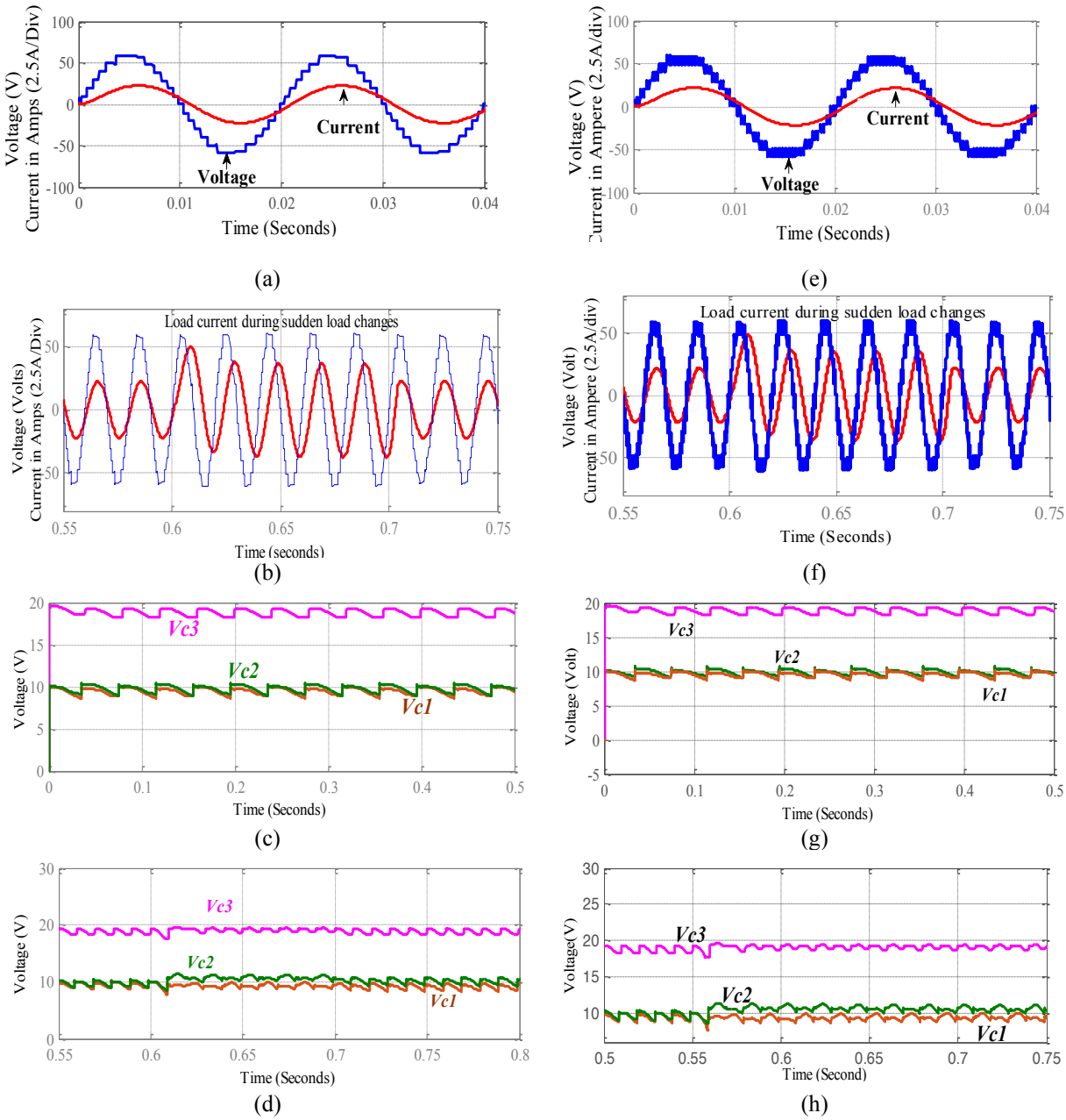


Figure 9. (a) Load Voltage and Current at normal operation (b) Capacitor voltages during normal operation (c) Load voltage and current during load changes (d) Capacitor voltage changes

In fundamental frequency switching scheme the frequency of reference sine wave is chosen as 50 Hz and the level shifted carriers are chosen as constant values 0.4,1.4,2.4 etc up to 5.4 for positive levels and -0.4,1.4,2.4 etc up to 5.4 for negative levels as suggested in (Sandeep et al, 2019) is used as shown in the Fig.3 to generate the gating pulses for the IGBTs. For an input voltage of 20V, the peak voltage obtained in the terminal is 60V. With that peak voltage applied across the load, the peak current observed is 1.192 A, as shown in Fig.9a. The capacitor voltages are observed as C_1=C_2=10V and for capacitor C_3 it is 20 V as shown in Fig.9c. For a sudden change in load applied in the circuit the load current and capacitor voltages settle down within a cycle and with less overshoot, as shown in Fig.9b and Fig.9d thus ensuring the reliability of the circuit components. In particular the capacitor voltage settles down and balanced with in a cycle following the damped-out load changes as shown in Fig.9d.

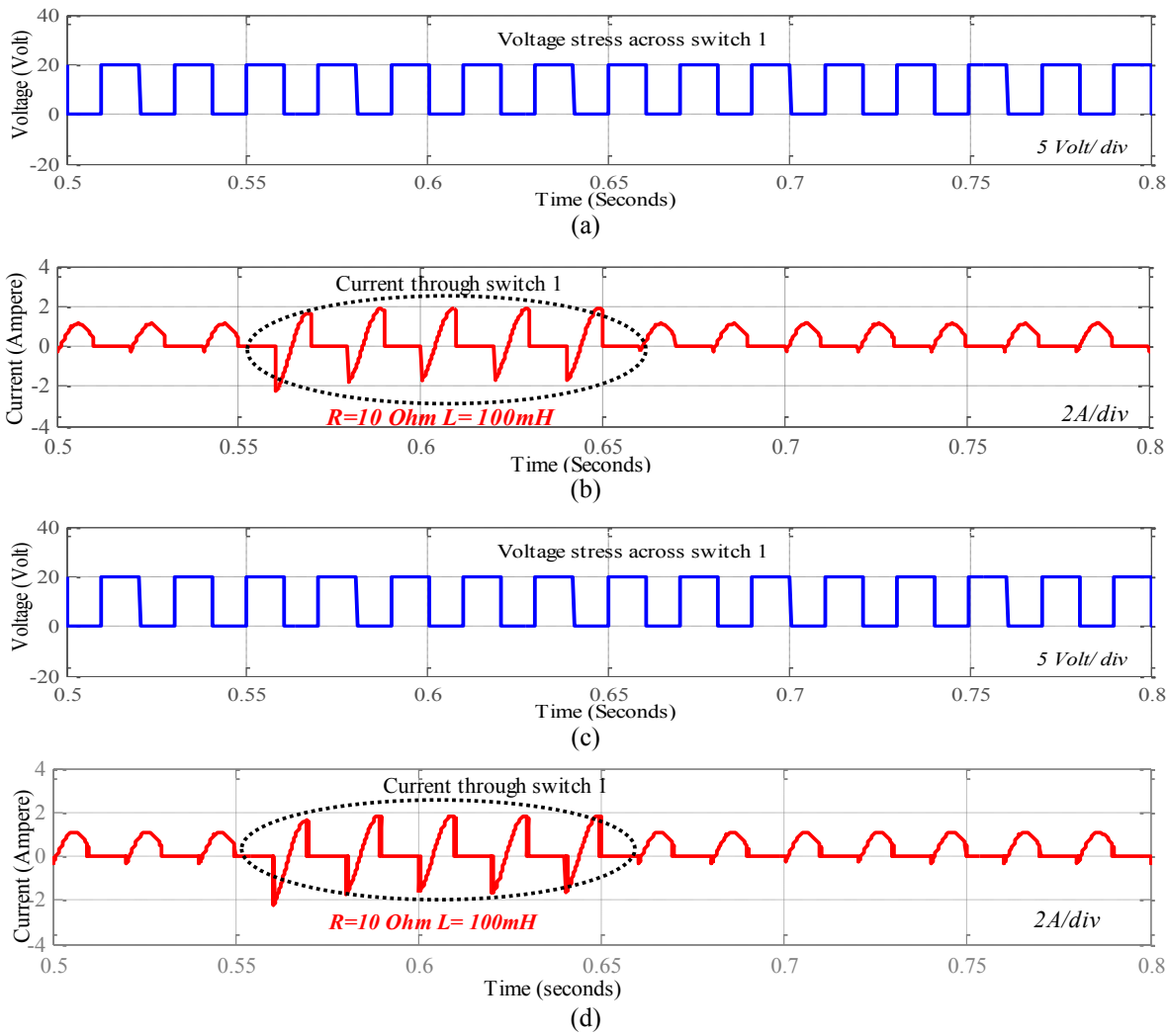


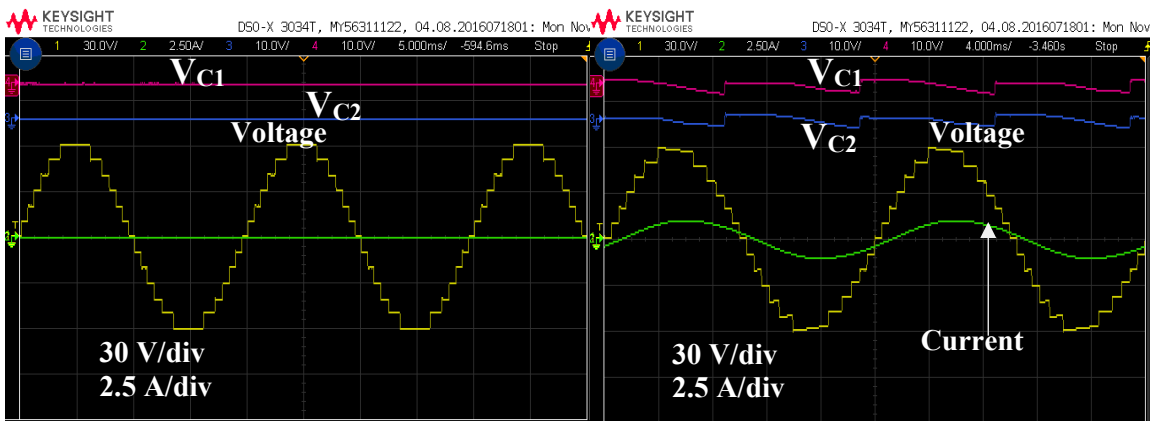
Figure 10. (a) Switch voltage and Switch current in fundamental frequency switching
b) Switch voltage and Switch current in high frequency switching

For high frequency switching scheme with the reference sinewave of 50 Hz remaining the same, The carriers are chosen as triangular waves with magnitudes (0,1,0)V, (1,2,1)V, (2,3,2)V etc up to (5,6,5)V with a switching frequency of 5kHZ and for negative cycle the carriers are 0,-1,0)V, (-1,-2,-1)V, (-2,-3,-2)V etc up to (-5,-6,-5)V with the same switching frequency. The Load voltage and load current waveforms when high frequency switching is

employed is shown in the Fig.9e-9h. The voltage across the switch S_1 and the corresponding switch current are observed to analyse the behavior of switches under varying switching frequency and sudden load changes and the observations are presented in Fig.10. From the Fig.9 and Fig.10, it can be found that, C^2SC-MLI exhibits the similar charecteristics in high frequency and fundamental frequency switching control. The voltage across the switches remains the same inspite of change in system load and the the current transition occurs smoothly during load changes. Thus, the adaptability of the switches to fundamental and high frequency switching schemes and to sudden load changes makes the circuit reliable under wider operating span.

EXPERIMENTAL RESULTS

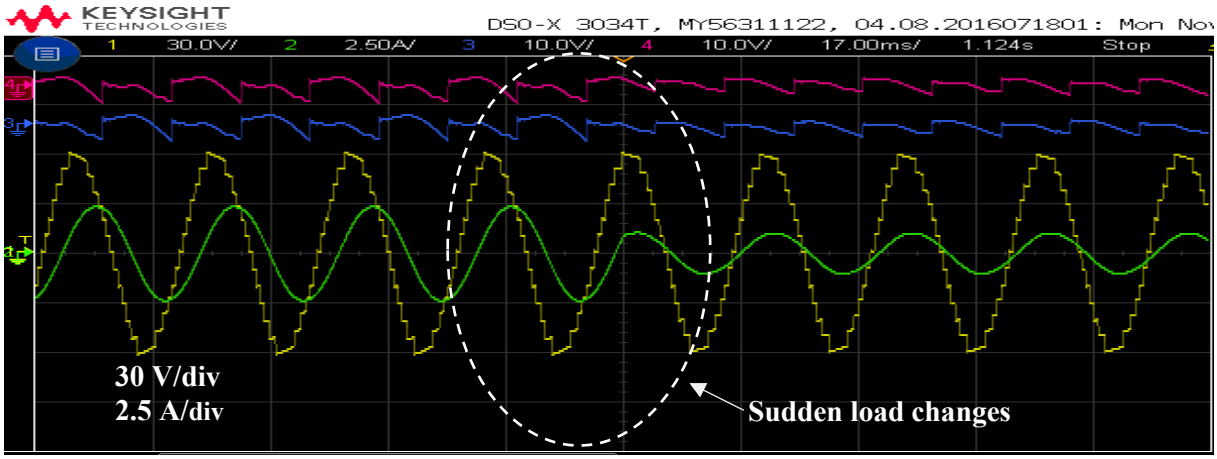
An experimental prototype of C^2SC-MLI rated 0.1 kW is fabricated with IHW15N120E1 switches. The solar PV unit shown in Fig.8 is realized using an ecosense made solar PV emulator with an inherent dc-dc converter. The ecosense solar PV emulator is made to emulate the characteristics of M/s.SunPower made solar PV panels with a rating of 40V, 5A, 161W_p in series parallel combinations. The switching algorithm is embedded in an FPGA spartan 6 processor which fed the Driver IR2110 circuit. The SI4700M16 capacitors rated 16V/4700µF are used for C_1 and C_2, and SI4700M25 capacitor rated 25V/4700µF is used for C_3.



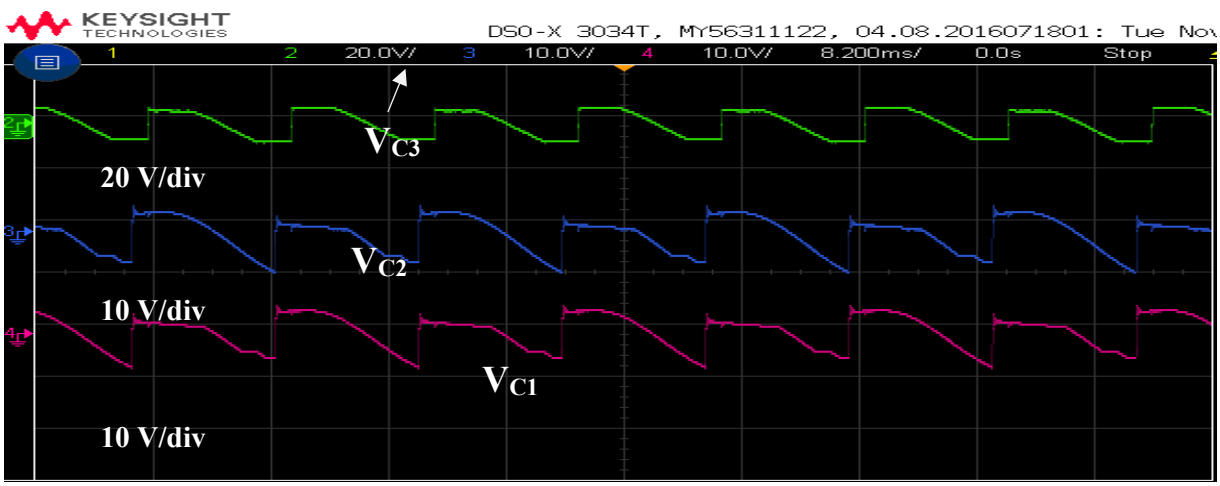
(a) (b)

Figure 11. (a) No load voltage and current (b) Voltage and current at R=50 ohm and L=50 mH

The solar PV emulator delivers an input voltage of 20V. The no load voltage is shown in Fig.10a. The capacitor voltage under no load is zero as shown in the Fig.10a. The voltage delivered by the emulator divides as 10V across each clamping capacitor C_1 and C_2 when loaded as shown in Fig.10b. For an input of 20V, a peak terminal voltage of 60V can be obtained which when fed to a load with R=50Ω and L=50mH, a peak current of is 1.2 A observed as shown in Fig.10b. From the Fig.12a it can be observed that when the load is changed from R=10Ω and L=100mH to R=50Ω and L=50 mH, the load current changes from 2.5A to 1.2 A within a cycle. Further, the disturbed capacitor voltages settle down to new steady state with balanced voltage with in a cycle.



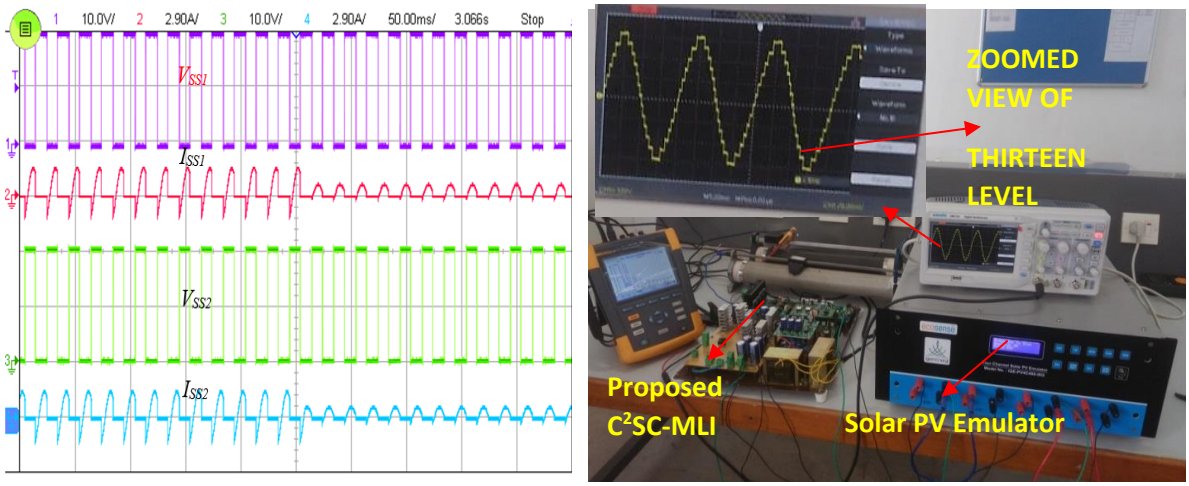
(a)



(b)

Figure 12. (a) Voltage and current during sudden load changes (b) Capacitor voltages

The voltage of capacitors C_1 and C_2 balances at 10 V and that of capacitor C_3 at 20 V as shown in Fig.12b. In simulated capacitor voltage waveform, the capacitor is charged instantaneously as its internal resistance is neglected. In experimental setup, the practical capacitors will have a finite internal resistance resulting in lagging rise time as depicted in Fig.12b. In the experimental capacitor voltage waveform, the dynamic characteristics of the C^2SC-MLI is analyzed under changing load conditions. as shown in Fig.12a. This smooth transition in load current and capacitor voltages ensures that the switches and capacitors are reliable.



(a) (b)

Figure 13. (a) Voltage and current stress in switches 1 and 2 changes (b) experimental setup

The efficiency of the topology can be calculated using the equations given in Table 3 and equation (20). The switching loss per switch in the switch group number 1 is calculated as follows, The internal resistance of every switch is R_{ON}=0.1 Ω as given in the datasheet of IHW15N120E1, The load current is 1.2A, and the conduction period of α_1 to α_7 which is $6\alpha_s/28$, the conduction loss is 0.027425W, which when multiplied by four, the loss incurred in switch group 1 is 0.1097W. Similarly, the conduction of other switch groups and zero state are calculated and the total conduction loss is 0.462W. The blocking voltage of the switch S_1 is 20 V as shown in the Fig.13a, the on-state voltage drop for an internal resistance of 0.1 Ω and a conduction current 1.17A is 0.117V, it has 2 switching instants (conducts during entire negative cycle), The turn on and turn off time of IGBT taken from data sheet is 50µs, with this data, the switching loss can be calculated using equation (15) as 0.003W. Thus, the total switching loss across all the switches is estimated as 0.98 W. The total capacitor ripple loss is 1.28W estimated using equation (20). The loss across the diode is neglected as it is very minimal and conducts only during the zero state. Summing up all the losses will yield net loss as 2.692W. Therefore, the efficiency of the topology is 96.6%. The experimental setup is shown in the Fig.13b. The cost of the topology is compared with the similar topologies available in the recent literature and the results are given in the Table 4. given below.

Table 4. Cost Comparison

Device	Model	Unit cost	Sze 2018	Junfeng etal,2014	Alishah et al, 2016	CHB MLI	NPC MLI	FC MLI	Proposed
IGBTs	IHW15N120E1	2.73	65.52	49.14	38.22	65.52	65.52	65.52	38.22
Diodes	1N3208	3.63	14.52	10.89	14.52	0	43.56	98.01	10.89
Gate Driver	IR2110	1.80	36	5.4	7.2	0	21.6	0	1.8
Capacitors	SI4700M16	7.99	31.96	143.82	111.86	191.76	191.76	191.76	23.97
Total Cost			$148	$209.25	$171.8	$257.28	$322.4	$355.29	$74.88

CONCLUSION

A novel switched capacitor inverter topology named C 2 SC-MLI is proposed and experimentally verified for synthesizing 13 levels. It's confirming that the proposed topology uses lower power components count and subjected to low voltage stress on individual switches, i.e. the ratio of peak output voltage and maximum blocking voltage on switches is only 0.66 which is comparatively lower than the other SCMLI topologies presented in literatures. Further, in the proposed topology it has been proved that the switching and conduction losses are low owing to less components and in addition to this, the voltage rating and capacitance of floating capacitors are low which further increases the efficiency and reliability of the proposed inverter. The extension of proposed topology is recommended which is more suitable for higher number of voltage level and it suitable for medium and high voltage applications like PV power plant and HVDC etc.

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