Subthreshold modeling of dual-halo dual-dielectric triple-material surrounding-gate (DH-DD-TM-SG) MOSFET for improved leakages

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ABSTRACT

This paper presents a model of Subthreshold current and Subthreshold swing model for Dual-Halo Dual-Dielectric Triple-Material Cylindrical Gate All Around/Surrounding Gate (DH-DD-TM-CGAA/SG) MOSFET for improved leakages. The virtual cathode method is used to derive the current in the subthreshold regime. The model presented in this paper also incorporates the effect on subthreshold characteristics of the device with variation in radius of silicon pillar and gate oxide thickness. The channel leakage current is a key metric to evaluate the capability of the device. The effectiveness of DH-DD-TM-CGAA MOSFET was observed by comparing it with the conventional triple metal structures. Furthermore, the consequence of variation in technology parameter is also studied. The outcomes of the proposed model depict the cutback in subthreshold channel leakage current as compared to existing triple metal structures. The analytical results show the excellent agreement with the simulated results.

Keywords: halo implant; dual-dielectric; short channel effects (SCE's); subthreshold current and swing; triple-metal surrounding gate (TM-SG) MOSFET.

INTRODUCTION

In the development of nanopower devices the scaling of classical MOSFET has been the most prominent challenge for device engineers in recent years (Colinge, 2004). But the further downscaling of the MOSFET is not possible due to short channel effects (SCEs). The constraint imposed by SCEs is avoided by modifying the device structure. The dual gate (DG), triple gate (TG), and cylindrical gate all around (CGAA) MOSFETs (Sharma et al., 2016) are the futuristic structures. The CGAA MOSFET offers a higher current drive capability, high packaging density, and low leakage current as compared to classical MOSFET. This is mainly due to superior control by gate over the channel (Verma et al., 2015). Hence, after incorporating the advantage of CGAA MOSFET with triple material and dual dielectric further enhances the performance of the device. The dual dielectric structure minimizes the gate leakage and improves the carrier transportation efficiency in the channel. Wang et al. (2012) proposed a TM-SG MOSFET. The TM-SG MOSFET offers good scalability and reduction in SCEs. The superposition method was used to develop the model, which involves complex mathematical calculations to find out the threshold voltage and surface potential. Vaddi et al. (2011) described a model for a generic DG MOSFET with gate to source underlap. The model is useful only for underlap MOSFETs and used for reduction in subthreshold leakage current. Liu & Hsieh (2000) proposed a model

for the subthreshold behavior of a MOSFET. The model assumes that the threshold voltage above the gate to source voltage V_{ds} is small. This assumption is not applicable to triple material structures. The model for fully depleted double gate MOSFET was developed by Xi Liu et al. (2010). The model uses the variable separation technique that involves complex mathematical calculations. Gautam et al. (2012) presented a model for CGAA MOSFET using the impact of localized charges. This is a charge dependent model, which is an indirect way of finding the subthreshold current. Tiwari et al. (2012) proposed the subthreshold characteristics of TM-DG MOSFET by using virtual cathode concept. A similar approach was adopted by Dhanaselvam & Balamurugan (2013) to identify the subthreshold characteristics of TM-SG MOSFET. The subthreshold characteristics of DH-DD-TM-CGAA MOSFET have not been reported in the literature. The virtual cathode technique by considering the drift and diffusion components of current densities is used to find the subthreshold characteristics of the device. The performance of the device is investigated with different device parameters and the characteristics are analyzed and compared with other existing devices.

DEVICE STRUCTURE

A 3D view of cylindrical DH-DD-TM-SG MOSFET is shown in Figure 1.The schematic view of DH-DD-TM-CGAA MOSFET structure is depicted in Figure 2. It is conspicuous that the gate terminal contains three metals M_1, M_2, and M_3. The device consists of gate stack having work function ϕ_{M1} (Au) = 4.8 eV, ϕ_{M2} (Mo) = 4.6 eV, and ϕ_{M3} (Ti) = 4.4 eV, respectively. The triple metal has been constructed by employing Molybdenum (Mo) acting as gate material as its work function can be changed by varying N_2 implant (Lin et al., 2002). The thicknesses of the inner and outer oxide layers are t_{Sio2}=1nm and t_{HfO2}=4nm, respectively. The lengths of channel region L_1 and L_5 are halo-doped with N_{dh} while the remaining parts are doped with N_{ak}, assuming that N_{dh} concentration is more than N_{ak} concentration (Balamurugan et al., 2008). Table 1 describes the device parameters for simulation and Table 2 summarizes the model used to carry out the simulation.

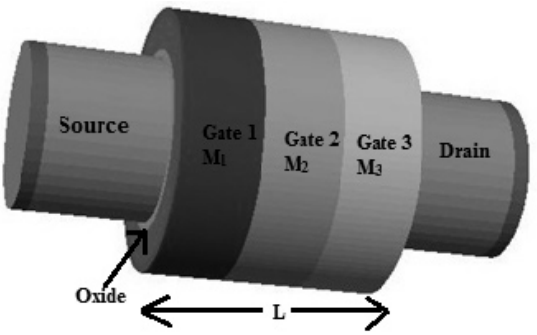

Figure 1. 3D View of cylindrical DH-DD-TM-SG MOSFET.

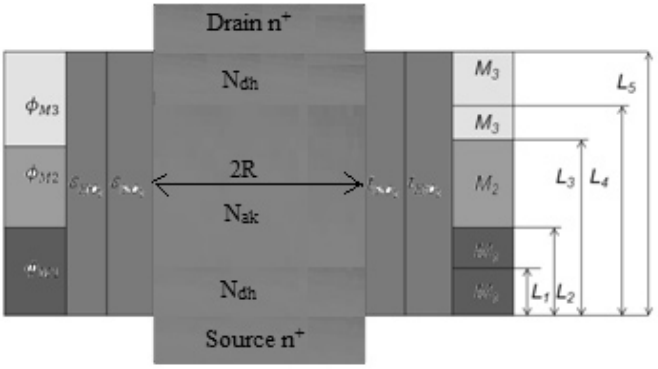

Figure 2. Schematic View of cylindrical DH-DD-TM-SG MOSFET.

Table 1. Summary of device parameters for DH-DD-TM-SG and TM-SG.

Parameters	**DH-DD-TM-SG MOSFET**	**TM-SG MOSFET**
Channel Length (nm)	30	30
S/D Doping (/m^3)	$1x10^{26}$	$1x10^{26}$
Channel Doping (/m^3)	$1x10^{23}$	$1x10^{23}$
Channel Halo Doping (/m^3)	$1x10^{24}$	-
Silicon Oxide Thickness (nm)	1.78	1.78
Silicon Thickness (nm)	10	10
Source/Drain Length (nm)	15	15
Permittivity of SiO_2	3.9	3.9
Permittivity of HfO_2	20	-

Table 2. Summary of the physical models employed to carry out the simulation for DH-DD-TM-SG and TM-SG.

Physical Model	**Description**
Mobility model	Lombardi CVT model is good for non-planar device and FLDMOB model has been used to consider the velocity saturation effect
Recombination model	Shockley-Read-Hall (SRH) model is used to integrate carrier lifetimes
Impact ionization and tunnelling model	Not used for current simulation
Energy transport model	Drift diffusion model is considered for carrier transport mechanism
Statistics	Boltzmann transport model considers the carrier statistics and highly suitable for semiconductor devices
Numerical method	Newton method is used to solve the all system of unknown together

ANALYTICAL MODEL

Subthreshold Current

In ideal circumstances a device should be turned off when the gate overdrive voltage is below the device threshold voltage. But practically a small amount of current flow is well known as the subthreshold conduction current. Therefore, it is essential to consider the subthreshold behavior of a MOSFET. The proposed model depends on the virtual cathode concept. Initially, the current flows from source to drain in the z-direction. Therefore the total current density (drift and diffusion) is given by Dhanaselvam et al. (2008):

$$J_T(r,z) = -q\mu \mathrm{c(r,z)} \frac{d\phi_k(\mathrm{r},z)}{dz} \qquad (1)$$

where c(r, z) represents the carrier concentration and is given as

$$c(r,z) = c_i e^{\frac{q\phi_k(r,z)}{K_B T}} \quad k=1, 2, 3, 4 \& 5 \tag{2}$$

By integrating the $J_T(r, z)$ from 0 to R, i.e., the diameter of the silicon, given by $R=t_{si}/2$, the subthreshold current is given by

$$I_{ds,sub}(z) = \pi t_{si} \int_0^{\frac{t_{si}}{2}} J_T(r,z)dr \tag{3}$$

At position $z=z_{kmin}$, the subthreshold current occurs and it is given as

$$I_{ds,sub} = \left[\frac{\pi \mu t_{si} \frac{K_B T}{q} \left(1 - e^{\frac{-qV_{ds}}{K_B T}}\right)}{\int_0^L Q_K^{-1}(z)dz} \right] \tag{4}$$

$$I_{ds,sub} = \left[\frac{\pi \mu t_{si} \frac{K_B T}{q} \left(1 - e^{\frac{-qV_{ds}}{K_B T}}\right)}{\int_0^{L_1} Q_1^{-1}(z)dz + \int_{L_1}^{L_2} Q_2^{-1}(z)dz + \int_{L_2}^{L_3} Q_3^{-1}(z)dz + \int_{L_3}^{L_4} Q_4^{-1}(z)dz + \int_{L_4}^{L_5} Q_5^{-1}(z)dz} \right] \tag{5}$$

where

$$Q_K(z) = 2\int_0^{\frac{t_{si}}{2}} \left(q \frac{c_i^2}{N_{ak}} e^{\frac{\phi_k(r,z_{k\min})}{V_T}} \right) dr \tag{6}$$

The trapezoidal rule is used to express the indefinite integrals; $Q_K(z)$ is approximated as

$$Q_K \approx \frac{t_{si}}{2p} q \frac{c_i^2}{N_{ak}} \left(e^{\frac{\phi_k(r,z_{k\min})}{V_T}} + 2\sum_{m=1}^{p-1} e^{\frac{\phi_k(\frac{t_{si}}{2p}m,z_{k\min})}{V_T}} + e^{\frac{\phi_k(0,z_{k\min})}{V_T}} \right) \tag{7}$$

for k=1, 2, 3, 4, & 5 and $1 \le p \le \infty$.

Put the equation in subthreshold current expression:

$$I_{ds,sub} = \frac{\pi \mu t^2{}_{si} c_i^2 K_B T \left(1 - e^{\frac{-V_{ds}}{V_T}}\right)}{\left[\frac{L_1}{M_1} + \frac{L_2}{M_2} + \frac{L_3}{M_3} + \frac{L_4}{M_4} + \frac{L_5}{M_5}\right] 2pN_{ak}} \tag{8}$$

$$M_1 = e^{\frac{\phi_1(r,z_{k\min})}{V_T}} + 2\sum_{m=1}^{p-1} e^{\frac{\phi_1(\frac{t_{si}}{2p}m,z_{k\min})}{V_T}} + e^{\frac{\phi_1(0,z_{k\min})}{V_T}} \tag{9}$$

Due to the symmetrical structure of DH-DD-TM-SG MOSFET, the above equation can be approximated as

$$M_k \approx e^{\frac{\phi_k(r,z_{k\min})}{V_T}} + e^{\frac{\phi_k(0,z_{k\min})}{V_T}} \tag{10}$$

$$M_k \approx 2e^{\frac{\phi_{k\min}}{V_T}} \tag{11}$$

$$I_{ds,sub} = \frac{\pi\mu t^2{}_{si} c_i^2 K_B T\left(1-e^{\frac{-V_{ds}}{V_T}}\right)}{\left[\frac{L_1}{e^{\frac{\phi_{1\min}}{V_T}}} + \frac{L_2}{e^{\frac{\phi_{2\min}}{V_T}}} + \frac{L_3}{e^{\frac{\phi_{3\min}}{V_T}}} + \frac{L_4}{e^{\frac{\phi_{4\min}}{V_T}}} + \frac{L_5}{e^{\frac{\phi_{5\min}}{V_T}}}\right] N_{ak}} \tag{12}$$

So, $\phi_{5\min} > \phi_{4\min} > \phi_{3\min} > \phi_{2\min} > \phi_{1\min}$; therefore the above expression can be reduced to

$$I_{ds,sub} \approx \frac{\pi\mu t^2{}_{si} c_i^2 K_B T\left(1-e^{\frac{-V_{ds}}{V_T}}\right) e^{\frac{\phi_{1\min}}{V_T}}}{L_1 N_{ak}} \tag{13}$$

where $V_T = \frac{K_B T}{q}$

Subthreshold Swing

Subthreshold Swing (SS) is a key metric for a MOSFET. The gate-source voltage needed to drop down the subthreshold current by a factor of ten is known as subthreshold swing and is given by (Gupta et al., 2018a;2018b).

The Subthreshold Slope (SS) is written as

$$SS_{dh} = 2.303\frac{K_B T}{q}\frac{1}{\frac{d\phi_{1\min}}{dv_{gs}}} \tag{14}$$

$$\phi_{1\min} = 2\sqrt{\alpha_1\beta_1} - \frac{\chi_1}{\kappa^2} \tag{15}$$

where the Boltzmann's constant $k_B = 1.38x10^{-23} J/K$, T=300K, the intrinsic carrier concentration $c_i = 1.45x10^{10} cm^{-3}$, and electron mobility $\mu = 1076 cm^2/Vs$. The value of α_1, β_1, χ_1, κ^2 and $\phi_{1\min}$ is reported in the literature (Gupta et al., 2018c).

RESULTS & DISSCUSSION

The subthreshold current and swing of DH-DD-TM-CGAA MOSFETs are determined with respect to various device parameters. The control gate having more work function is contiguous with source. The moderate work function contained by the first screen gate and the work function contained by the second screen gate is the least, which is adjacent to drain. The subthreshold leakage current is plotted for varying gate to source bias for DH-DD-TM-CGAA and TM-SG MOSFET. Figure 3 shows the deviation of $I_{ds,sub}$ at numerous values of the device length. From equation (13), the exponential dependence of $\phi_{1\min}$ on V_{gs}, produces the variation in subthreshold drain current. The smallest value of leakage current has been observed for longer channel length as compared to shorter one (Dhanaselvam et

al.,2013). This is mainly due to rise in minimum surface potential with smaller channel length due to existence of SCEs. There is significant increase in subthreshold current for smaller channel length because of exponential relationship between subthreshold current and minimum surface potential. The DH-DD-TM-SG shows $I_{ds,sub}$ of 1.88E-06 A at channel length of 30 nm, whereas TM-SG depicts 1.48E-05 A. It is manifested that $I_{ds,sub}$ is less for the DH-DD-TM-CGAA device as compared to TM-SG MOSFET due to high-K gate stack, which increases the short channel immunity in the device.

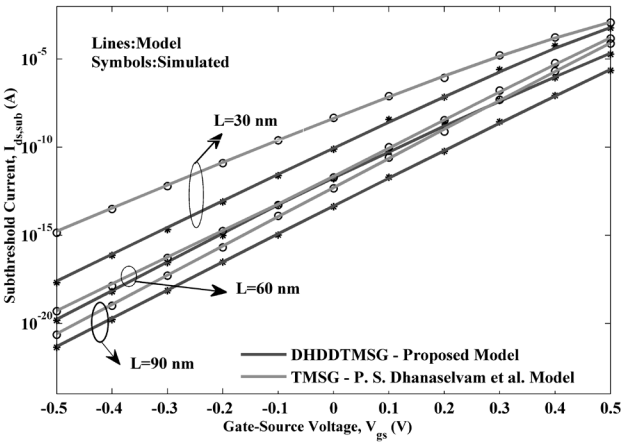

Figure 3. Variation in $I_{ds,sub}$ with V_{gs} for distinct channel length.

Figure 4 depicts subthreshold current against the gate voltage at different drain to source bias for DH-DD-TM-SG and TM-SG devices.

The subthreshold current varies linearly with the gate to source bias. But exponential rise is observed in subthreshold current with enhancement in drain to source bias. It is due to the drain induced barrier lowering. The increase in drain-source voltage moves up the position of minimum surface potential, which again raises the subthreshold current exponentially. So this exponential relationship becomes important for the shorter channel length devices.

The leakage current is neglected for longer channel length devices but their effect at smaller channel length cannot be ignored. Higher leakage current results in higher power consumption. So it must be considered at smaller lengths because it can result in low power consumption. The DH-DD-TM-SG shows $I_{ds,sub}$ of 2.59 nA at drain bias of 0.1 V, whereas TM-SG depicts 71.2 nA. The analytical results are well matched with simulated results.

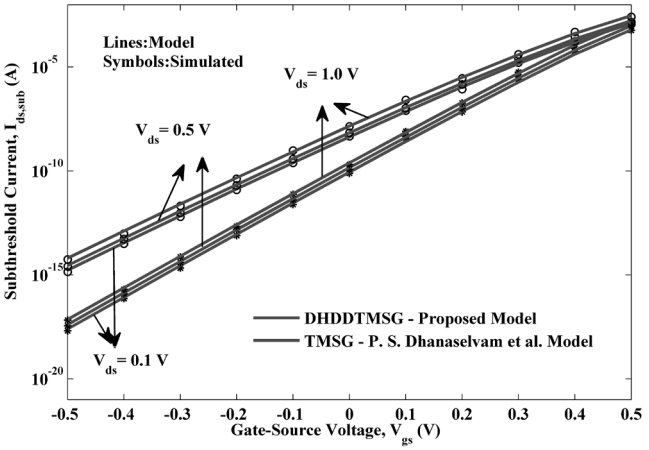

Figure 4. Variation in $I_{ds,sub}$ with V_{gs} at various drain bias.

Figure 5 depicts the subthreshold current against the gate voltage at different device length ratios for DH-DD-TM-SG and TM-SG devices. It is clearly observed that a smaller value of subthreshold current is obtained when the control gate length L_1 is increased. The characteristics resemble those of the long channel length devices. So the gate length ratio 3:2:1 has a small value of leakage current in comparison to the other channel length ratio. The minimum surface potential increases at lower ratio of L_1:L_2:L_3, which produces more subthreshold current as evident from Figure 5. The DH-DD-TM-CGAA has smaller value of leakage current as compared to TM-SG due to the device structure. The theoretical results are similar to the simulated results obtained by using TCAD Silvaco.

Figure 6 plots the subthreshold current against the gate voltage at different oxide thickness for DH-DD-TM-SG and TM-SG devices. It is observed that the increase in oxide thickness results in a more leakage current. This is because the thicker oxide causes reduction of control of gate terminal over the channel.

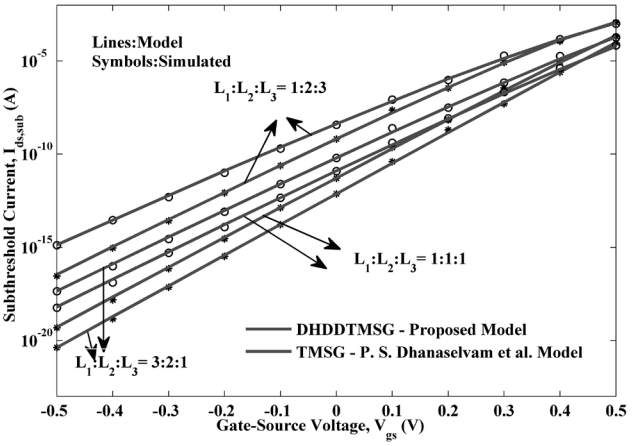

Figure 5. Variation in $I_{ds,sub}$ with V_{gs} at different device length ratio.

The thinner gate oxide reduces the subthreshold current when we move from 3nm to 1nm. This is due to enhanced electrostatic control of gate and lessened SCEs at thinner oxide. It is also compared with the TM-SG devices, which have poor switching performance as compared to DH-DD-TM-CGAA MOSFETs.

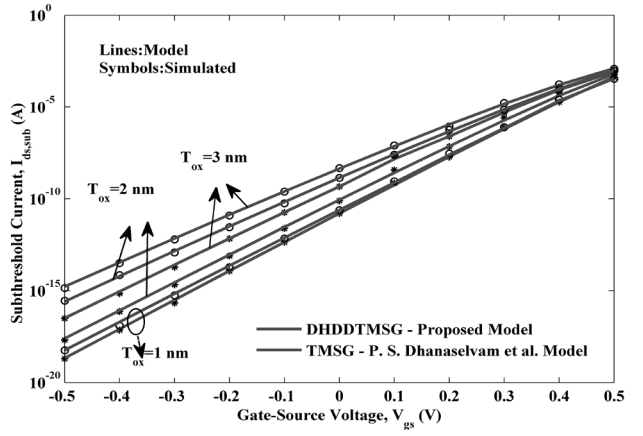

Figure 6. Variation in $I_{ds,sub}$ with V_{gs} at distinct oxide thickness.

Figure 7 shows the plot of subthreshold leakage current for various values of cylinder diameter/silicon thicknesses. The thickness of the silicon film is varied from 10nm to 30nm. It is observed that there is an increase in subthreshold leakage current with increase in silicon film thickness due to the poor channel electrostatics behavior (Chiang, 2009).

As it is obvious from subthreshold current expression of equation (13) that the subthreshold current varies with the square of silicon film thickness, this increases the leakage current. The large value of silicon thickness provides appropriate amount of driving current, which enhances the device speed. But this reduces the propagation delay and hence enhances the switching performance of the device. The trade-off among device speed and subthreshold current should be taken into consideration when designed in practical applications. The result obtained for the proposed device DH-DD-TM-CGAA is also compared with that of TM-SG MOSFETs.

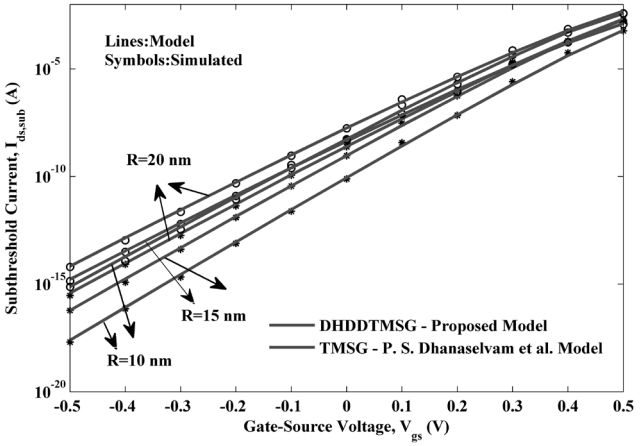

Figure 7. Variation in $I_{ds,sub}$ with V_{gs} at various radiuses of silicon pillar.

Figure 8 depicts the deviation of subthreshold current for diverse values of channel doping concentration. As shown in Figure 8 $I_{ds,sub}$ has changed from order of 10^{-20} A (at $N_a=10^{24}$ m^{-3}) to 10^{-15} A (at $N_a=10^{22}$ m^{-3}). This increase in $I_{ds,sub}$ with change in doping concentration is due to velocity saturation of electrons at high doping conditions. The velocity saturation causes drain current to become constant at high drain bias. The theoretical results are similar to the simulated results obtained by using TCAD Silvaco.

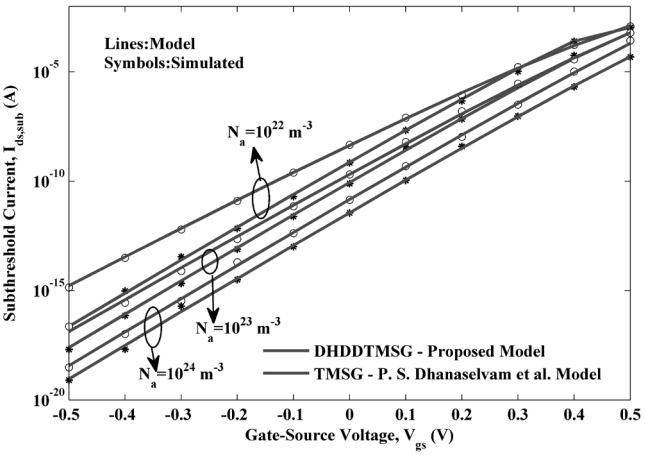

Figure 8. Variation in $I_{ds,sub}$ with V_{gs} at varying doping concentration.

SS is the capacity of the device to go from OFF to ON state. It should ideally be close to 60 mV/decade. Figure 9 depicts the subthreshold swing at different channel lengths. It is figured out that the SS is reduced for the proposed device as compared to TM-SG MOSFETs (Dhanaselvam & Balamurugan, 2013). This is mainly due to reduction in subthreshold leakage current in the proposed device as compared to others owing to the reduction of SCEs.

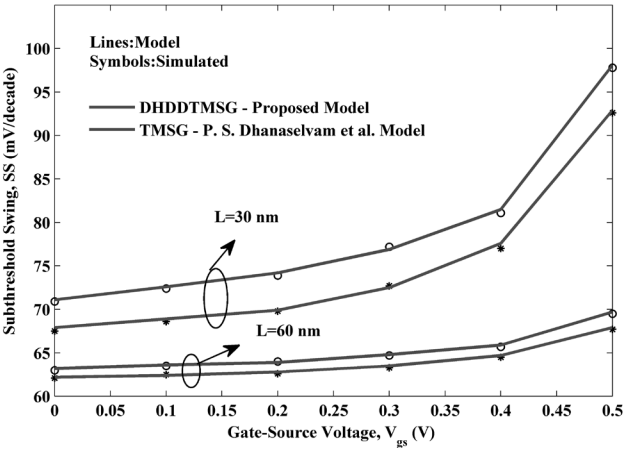

Figure 9. Variation in SS at different channel length for DH-DD-TM-SG and TM-SG MOSFETs.

The subthreshold swing is plotted for different drain-source bias in Figure 10. DH-DD-TM-SG MOSFET shows SS close to 60mV/decade. It is due to the halo implants and the dual dielectric of the channel. The improvement in SS due to the change in drain-source bias indicates that drain induced barrier lowering is less dependent on V_{ds}. The subthreshold behavior of the MOSFET can be studied by using the analysis of V_{ds} over the SS.

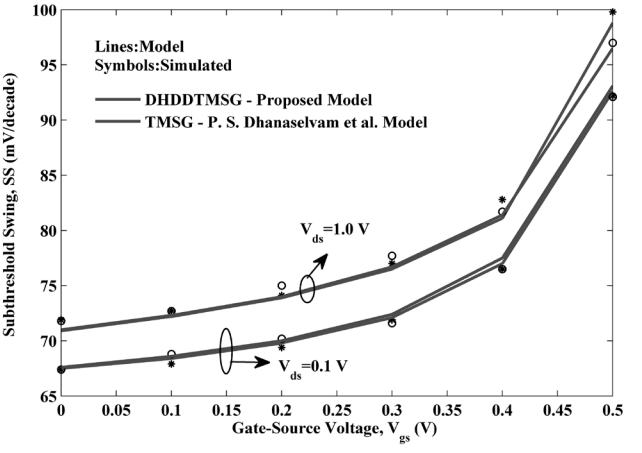

Figure 10. SS with varying drain-source potential.

Figure 11 depicts the variation of SS at different device length ratios. It is evident from the figure that the dependency of subthreshold swing on the V_{gs} is increased by increasing the gate to length ratio. The channel length ratio illustrates the amount of each gate material present in the device. The channel length ratio 3:2:1 has less subthreshold swing as compared to their counterparts 1:2:3 and 1:1:1. The SS appreciably decreases at lower ratio of L_1:L_2:L_3. The control on the channel decreases by the gate for a smaller value of control to screen gate ratio, which boosts up the SS as evident from Figure 11. The theoretical result is well calibrated with the simulated results.

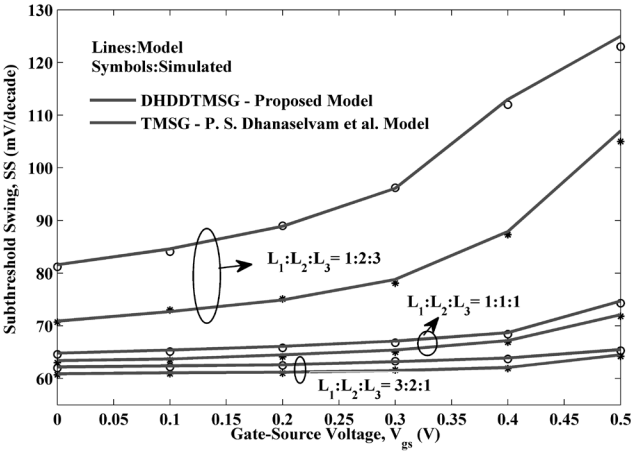

Figure 11. Variation in SS at different device length ratios with varying V_{gs}.

Figure 12 illustrates the subthreshold swing with various gate oxide thicknesses. The subthreshold swing increases with increase in oxide thickness. Higher subthreshold swing is obtained at thicker gate oxide due to poor gate control. The thinner gate oxide approaches to the long channel characteristics at lower channel lengths are visible in Figure 12. The thinner gate oxide provides better control of channel by the gate due to penetration of vertical field into channel and hence it reduces the SS. For operating a device in subthreshold region the SS should be kept to minimum value for better performance. This can be achieved by thin silicon film, which plays a vital role in the design of device for subthreshold region.

Figure 13 shows the plot of SS at various values of cylinder diameter/silicon thicknesses. For larger value of silicon film thickness, lack of control of gate terminal over the channel leads to enhancement in SCEs, which further enhances the SS. The proposed DH-DD-TM-SG MOSFET shows lesser value of subthreshold swing at different values of silicon film thickness as compared to TM-SG device.

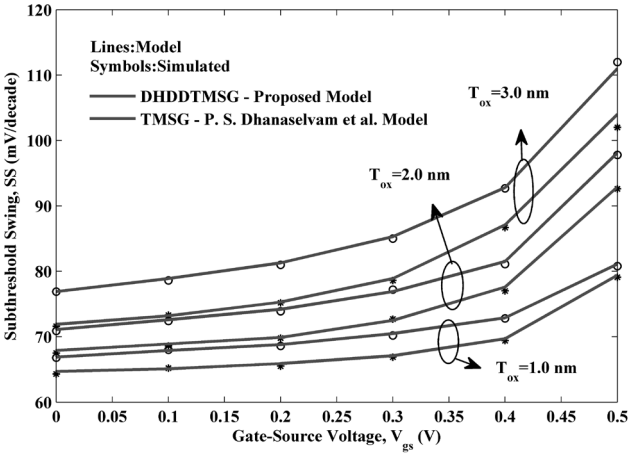

Figure 12. Variation in SS at numerous values of gate oxide thickness.

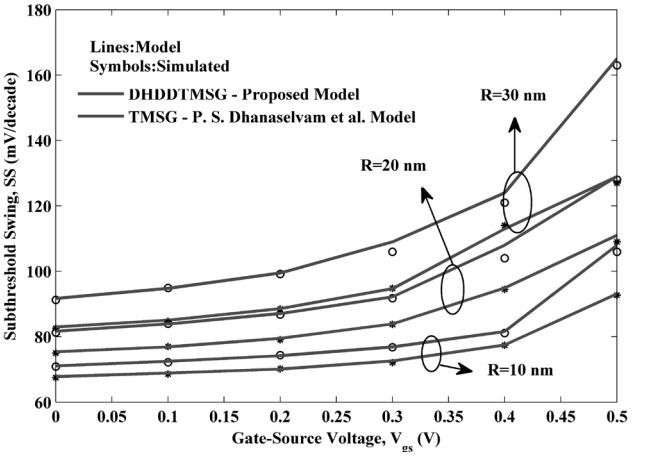

Figure 13. SS at various radii of silicon pillar for DH-DD-TM-SG and TM-SG.

Figure 14 depicts the deviation of SS at different values of channel doping concentration. The higher value of SS is observed for lesser value of doping concentration. The doping concentration causes minor changes in the $I_{ds,sub}$, but SS varies inversely with the channel doping concentration. The theoretical result well agreed with the simulated results.

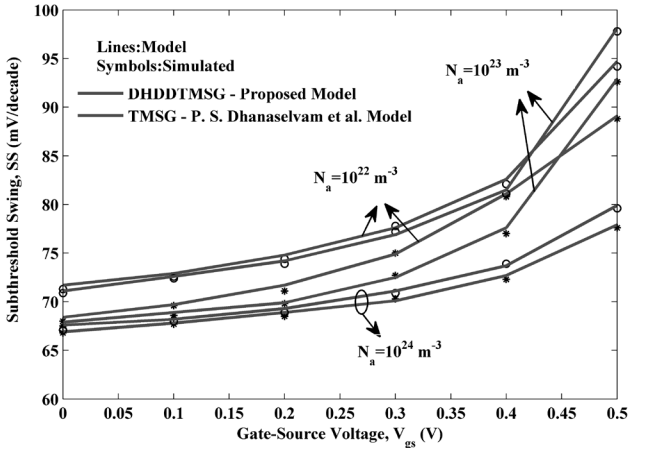

Figure 14. SS variation with varying values of channel doping concentration.

CONCLUSION

Analytical models of subthreshold current and subthreshold swing for dual-halo dual-dielectric triple-material cylindrical gate all around/surrounding gate (DH-DD-TM-CGAA/SG) MOSFETs have been developed. The virtual cathode method is used to derive the current in the subthreshold regime. The channel leakage current is a key metric to evaluate the performance of the device. The effect on subthreshold characteristics of the device with variation in silicon film thickness, doping concentration, channel length ratio, drain bias, and gate oxide thickness is also presented. It can be concluded that when the length of the control gate increases as compared to two screen gates, then the device has excellent performance in subthreshold regime. It can also be concluded that, at smaller values of oxide and silicon film thicknesses, the device shows good switching performance. DH-DD-TM-SG MOSFET shows SS close to 60 mV/decade. It is due to the halo implants and the dual dielectric of the channel. The DH-DD-TM-SG shows $I_{ds,sub}$ of 1.88E-06 A at channel length of 30 nm, whereas TM-SG depicts 1.48E-05 A. DH-DD-TM-SG shows 5.72% improvement in SS as compared to TM-SG MOSFET at L = 30 nm.

The outcomes of the present model depict the reduction in subthreshold channel leakage current and SS as compared to existing triple metal structures using TCAD Silvaco. So the proposed model provides guidance for making of future VLSI circuits with DH-DD-TM-CGAA MOSFETs.

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NOMENCLATURE

Symbols	Description
q	Electronic charge (C)
$\phi_k(r,z)$	Surface potential (V)
t_{si}	Silicon film thickness (nm)
N_{ak}	Acceptor ion concentration (atoms/m^3)
N_{dh}	Doping ion concentration (atoms/m^3)
z_{kmin}	Position of minimum surface potential (nm)
V_{ds}	Drain-source bias (V)
V_T	Thermal voltage (25.9 mV)
ϕ_{1min}	Minimum surface potential under metal M_1 (V)
L_1,L_2,L_3	Channel length at different metal gates (nm)