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# دراسة لمورفولوجيا السطح والتوصيف الضوئي لسطح رقائق السيلكون البللوري والمتعدد البللورات الذي تم تخشينه في محاليل قلوية مخففة

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# الخلاصة

يتناول هذا البحث دراسة لعملية تخشين سطح رقائق السيلكون البللوري والمتعدد البللورات من خلال تكوين تشكيلات هرمية بالنحت الكيميائي في محلول مخفف من هيدروكسيد البوتاسيوم وذلك من خلال تحديد درجة الحرارة المثلى للمحلول مما يؤدى إلى أقل إنعكاس ضوئي ممكن من على سطح السيلكون. ويتم في هذه الدراسة قياس الإنعكاس الضوئي بعد التخشين بإستخدام جهاز قياس الطيف الضوئي في شريط الطول الموجي الضوئي بعد التخشين من خلال المعاينة المجهرية للسطح بإستخدام مجهر القوة الذرية ومجهر المسح الإلكتروني. وقد وجد أن المجهرية للسطح بإستخدام مجهر القوة الذرية ومجهر المسح الإلكتروني. وقد وجد أن درجة حرارة المحلول المثلى لعملية التخشين والتي تؤدي إلى أقل إنعكاس ضوئي من السطح تتراوح بين 80 و85م للسيلكون البللوري مما يؤدي إلى إنعكاس ضوئي منتظم يقدر بحوالي 8.%، بعد وضع طبقة غير عاكسة على السطح بينما وجد أن درجة الحرارة المثلى تقع بين 85 و95م للسيلكون المتعدد البللورات مما يؤدي إلى إنعكاس ضوئي يقدر بحوالي 8.% بعد وضع الطبقة الغير عاكسة على السطح بينما وجد أن درجة الحرارة المثلى تقع بين 85 و95م للسيلكون المتعدد البللورات مما يؤدي إلى إنعكاس ضوئي يقدر بحوالى 8.% بعد وضع الطبقة الغير عاكسة على السطح بينما وجد أن درجة الحرارة المثالى تقع بين 85 و95م للسيلكون المتعدد البللورات مما يؤدي إلى إنعكاس ضوئي يقدر بحوالى 8.% بعد وضع الطبقة الغير عاكسة .

# Study of surface morphology and optical characterization of crystalline and multi-crystalline silicon surface textured in highly diluted alkaline solutions

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#### ABSTRACT

In this work, alkaline texturing of (100) crystalline Si and multicrystalline Si wafers in diluted KOH solution leading to pyramidal structures is studied as a function of the etching temperature. The surface morphology is investigated using Atomic Force Microscopy and Scanning Electron Microscopy and the surface reflectance is measured by spectrophotometry in the wavelength range 200-1200 nm. It is found that etching in diluted 1% KOH solution leads to incomplete surface texturing when the etching temperature is equal to 70°C. The optimum etching temperature is found to be in the range 80-85°C which results in a minimum surface reflectance for crystalline silicon covered with an antireflection coating of 0.8%, with a uniform distribution over a wider wavelength range for samples that received a saw damage removal in 30% KOH solution prior to texturing. On the other hand, the optimum etching temperature shifts to the higher range 85-95°C for multicrystalline silicon surface with a minimum reflectance of 4.6% with ARC.

Keywords: Surface texturing; alkaline texturing; silicon solar cell; front surface reflectance; anti-reflection coating.

#### INTRODUCTION

Surface texturing is a beneficial and essential step in the fabrication process of monocrystalline silicon (c-Si) and multicrystalline silicon (mc-Si) solar cells (Campbell & Green 1987; Sopori 1988; Hylton et al., 1996). It leads to an increased front surface area and hence to larger amount of light coupled into the cell. Equivalently, the presence of surface texture such as pyramidal structures and V grooves at the silicon surface allows the reflected light to have a second bounce onto the surface (Hylton et al., 2004) which increases the amount of light coupled into the cell and leads to a reduction in the fraction of reflected light from 35%-40% at the polished c-Si surface to theoretically 10-11% after the second bounce at the textured surface. However, the degradation of the open circuit voltage of the cell, due to extra recombination at the

larger front surface area is undermined by the gain obtained in the cell photocurrent, and therefore can be tolerated, especially if the front surface is properly passivated.

It is well known that the pre-processing surface treatment of silicon solar cells involves two etching steps carried out in alkaline etching solutions. Alkaline etching is anisotropic since it etches crystallographic planes in silicon with different rates and etches the (100) planes much faster than the (111) and (110) planes. This difference has been attributed to the different Si bond density, to the large differences in etching activation energies, to the etching retardation or halting caused by thin silicon oxide/ dioxide SiO instantaneously grown on some planes and not on others after immersion the silicon into the etchant which retards or stops the nucleation of pyramids, and to the competition between the forward and reverse etch reactions especially when the etching is done at low KOH concentrations (Seidel et al., 1990; Price et al., 1973; Palik et al., 1985; Palik et al., 1983; Glembocki et al., 1991; Raley et al., 1984; Kendall 1979; Kendall & de Guel 1985; Tan et al., 1996).

The first etching step is usually carried out with a high etch rate at 70°C in an alkaline solution, with a KOH concentration in the order of 30% per weight which removes approximately 5-10 µm from the as-cut wafer, releasing the surface from the damaged layer that degrades the carrier lifetime. The etch rate in this solution is relatively high (1-2 µm/min) (Singh et al., 2001) and the process leads to plane etching that does not lead to the formation of pyramidal hillocks, but results in a semipolished surface with enhanced roughness. The second etching step is necessary for the formation of randomly distributed or patterned pyramidal hillocks and V-grooved structures, which would reduce front surface reflectance and enhances coupling the light into the cell. This step is carried out by anisotropic wet chemical etching in alkaline organic solutions (Finne & Klein, 1967) such as Tetra-methyl ammonium hydroxide (TMAH) (Kim et al., 2013), ethylenediamine and hydrazine, or also in inorganic alkaline ternary aqueous mixture of water, isopropyl alcohol (IPA) and a low or intermediate KOH or NaOH concentrations (1-10%) in the temperature range 75°C-85°C (Seidel et al., 1990, Tan et al., 1996; King & Buck, 1991), during which pyramidal structures with a standard base angle of 54.74° are usually formed. The latter process is the most commonly used texturing process, as it is cost effective, safe, controllable and reproducible.

As far as non-textured mc-Si surface is concerned, the surface initially reflects less light than a polished c-Si surface due to the tilt angles between adjacent differently oriented crystallographic planes, that redirect the light to some extent, to effectively redirect the light for a second incidence (Hylton et al., 2004). Due to this wide variation of plane orientations, alkaline surface etching is not efficient in texturing a mc-Si surface, as it is in c-Si. Hence, the reduction in surface reflectance from a mc-Si surface textured in an alkaline solution is expected to be smaller than that observed from a (100) c-Si surface. Therefore, other surface texturing procedures should be recommended for effectively texturing mc-Si, such as isotropic acid etching (Li et al., 2012), plasma etching (Dekkers et al., 2000) and reactive ion etching (Dekkers et al., 2000) as well as physical texturing using laser (Zielke et al., 2012) and mechanical grooving (Dobrzanski & Drygala 2008).

The purpose of the present study is to investigate a highly controlled etching procedure of (100) c-Si and mc-Si wafers, in highly diluted alkaline solution with a 1% per weight KOH concentration at different temperatures. The purpose is to create a well controlled high density of pyramidal hillocks, that leads to low surface reflectance with the minimum amount of chemicals to be disposed, which is an important element, given the tremendous increase in the production volume of silicon solar cells.

The surface morphology of the textured surfaces is characterized by means of Atomic Force Microscopy (AFM) and Scanning Electron Microscopy (SEM), and the surface reflectance is measured and interpreted in view of the observed morphology. The impact of adding a thermally grown thick silicon dioxide (SiO<sub>2</sub>) antireflection coating (ARC) on top of the textured surface, on the surface reflectance is also assessed.

#### EXPERIMENTAL DETAILS

### **Texturing Chemical Procedure**

Experiments are carried out on Czochralski c-Si quarter 4 inch wafers (n-type and p-type) and on large grain mc-Si with grain size as large as a few hundreds of µm's, all with 1-10 Ω.cm resistivity. Prior to texturing, surface cleaning is carried out on some samples in a piranha solution made of boiling H<sub>2</sub>SO<sub>4</sub>/H<sub>2</sub>O<sub>2</sub> (4:1) at 95°C for 10 minutes and other samples were subjected to saw damage removal in a 30% KOH solution at 70°C for 10 minutes. At such KOH concentration, the surface etches very fast without any hillock formation, but leads to a surface rougher than the polished silicon surface, as depicted in the AFM images displayed in Figure 1(a) and Figure 1(b). These images describe the surface roughness of both groups, defined as the root mean square height of the surface as obtained from the AFM Pico image software. The surface roughness amounts to 0.558 nm for c-Si cleaned in piranha solution and to 0.876 nm for c-Si etched in 30% KOH solution.

The samples are then cleaned, following a standard RCA cleaning procedure (Kern 1993) followed by a 2% HF dip to remove the very thin native oxide layer grown during the chemical cleaning procedure. Finally the samples are rinsed in DI water and dried using a nitrogen jet to be ready for texturing. The texturing was carried out with no stirring under a laminar flow for 20 minutes during which the solution temperature was monitored and kept constant. The alkaline etching solution consists of KOH with a concentration of 1% wt (5 mg): Isopropyl Alcohol (IPA) 6% wt (30 ml):  $12~M\Omega$  De-ionized (DI) water (465 ml). Isopropyl alcohol is added to reduce the etch rate to the required levels without participating in the chemical reaction. Its main role is to improve uniformity of the pyramidal hillocks by acting as a wetting agent that adjusts the relative water concentration in the KOH solution, without severely affecting the pH value (Price 1973). It also helps removing hydrogen sticking on the silicon surface, which can be residual of the HF dip or cleaning process and which retards pyramid nucleation at selective sites. The temperature of the solution is used as a process parameter that varies in the range 70-95 °C.

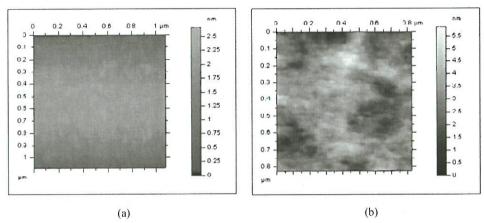


Fig. 1. AFM image showing surface roughness of c-Si surface: (a) after cleaning in piranha solution, (b) after etching in 30% KOH solution.

# Characterization of the morphology of textured surfaces

The surface morphology was investigated by means of an Agilent 5420 Atomic Force Microscope (AFM) in tapping mode. AFM images were processed using Pico image software and scanning has been done in two window sizes: 25  $\mu$ m and 10  $\mu$ m. In tapping AFM mode, both topography and amplitude images are captured side by side. The amplitude images map the slopes of the changes in the topography of the surface, which relate to the amount of deflection of the tip, as it encounter any change in the topography (up or down). Therefore amplitude images display these changes as clear voltage signals which highlights feature edges much sharper than the topography image. The surface morphology and topography are also looked at by means of Scanning Electron Microscopy (SEM).

# Monocrystalline silicon

After 20 minutes etching at 70°C, random hillocks pyramidal in shape with four lateral {111} planes resting on the (100) oriented plane begin to form as depicted in the AFM image of Figure 2(a) and in the SEM microphotograph of Figure 2(b). By looking

closely at the images, it is possible to say that the base of the hillocks is nearly but not perfectly square, which has been observed by Tan et al. (1996) and attributed to a slight deviation of the side planes from the {111} orientations. These hillocks are distributed sparsely, which is indicative of random inhomogeneous nucleation, in the early stages of the reaction, at preferential sites arising from crystallographic defects or wetting. The AFM scanning window image and the SEM microphotograph displayed in Figure 2(a) and Figure 2(b) indicate partial covering of the surface area, with well developed pyramids. It has been reported earlier, that etching at high KOH concentrations reaches its maximum rate at round 72°C (Singh et al., 2001), and that etching at 60°C for 10 minutes in 2% KOH resulted in a dense distribution of smaller size pyramids (0.8 μm) (Sethi et al., 2012). Also, hillock density is reported to increase at lower KOH concentration, but at high etch temperature (Tan et al., 1996). Therefore, the lower hillock density observed here with the 1% KOH etch at 70°C may suggest that either: i) the 70°C etch temperature is too low to allow hillocks to nucleate in the 1% KOH concentration even with the presence of alcohol, setting a threshold temperature for nucleation at such low concentration, or ii) hindrance of etching due to residuals of native oxide or hydrogen bubbles at the surface (Tan et al., 1996).

The base width of the pyramids is approximately equal to 3.2 µm and the height of the pyramids is estimated from surface roughness measurements to be in the  $2.5 \mu m$ range, which leads to hillock side angles close to the theoretically expected value of 54.74°. From the size of well developed hillocks, the etch rate is estimated to about 0.125 µm/min. A similar texture shape is observed for the surface of wafers with saw damage removed in a 30% KOH solution as depicted in Figure 3. The size of the pyramids in this case is almost equal to the previous case with no saw damage removal, but with a much smaller density.

Etching at T = 80°C leads to a much dense distribution of larger hillocks in which smaller hillocks are embedded with a surface coverage of practically 100%, as depicted in Figure 4, for wafers that did not receive a saw damage removal in 30% KOH solution. The largest pyramid has a base width of 4.2 µm and a height of 3 μm, which again confirms the expected theoretical side angles. In addition, with an average base size of 4 µm, the estimated hillock density is 6 x 106 /cm2 which agrees well with the trend reported for the hillock density versus percentage (%) KOH concentration for etching at 80°C (Tan et al., 1996) and with the average size reported with texturing for the same duration in a low KOH concentration (0.5-3%) at higher temperature (Wijekoon et al., 2011).

The etch rate at 80°C in the 1% KOH solution used here is estimated to approximately 0.15 µm/min which agrees with previous results (Alvi et al., 2008) and which, by fitting the experimental results could be expressed by the Arrhenius expression



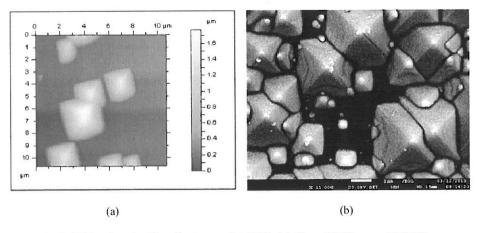


Fig. 2. (100) oriented c-Si surface textured at 70°C: (a) 10 µm AFM image, (b) SEM microphotograph with 11K magnification

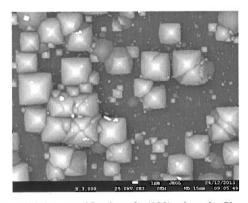


Fig. 3. SEM micrograph with 3K magnification of a (100) oriented c-Si surface textured at 70°C for wafers with saw damage removed in 30% KOH solution.

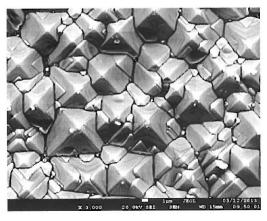


Fig. 4. SEM image of a (100) oriented c-Si surface textured at 80°C (No saw damage removal).

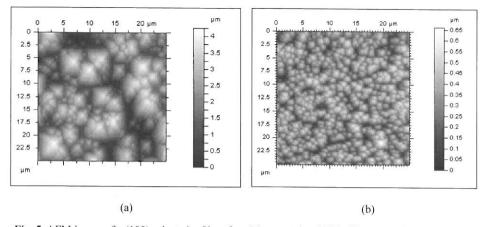


Fig. 5. AFM image of a (100) oriented c-Si surface (a) textured at 80°C with no saw damage removal (b) textured at 80°C for wafers with saw damage removal in 30% KOH etch.

Where the 0.6 eV activation energy lies within the 0.53-0.6 eV range previously reported for KOH etching mixtures (Seidel et al., 1990; Fan et al., 1988; Zhou et al., 2008), and is far from the 1.2 eV Si deposition activation energy which consolidates the hillock formation by etching, rather than by deposition. These values and results, however, should be taken very cautiously, since much smaller pyramid and much dense pyramid distribution are obtained in wafers, which have received a saw damage removal in 30% KOH solution prior to texturing in 1% KOH at 80°C as depicted in Figure 5, which shows that in this case the pyramids seem to maintain their small size in the 2-3 µm range, but are densely nucleated and cover all the surface area.

#### Multicrystalline silicon (mc-Si)

Large grain multicrystalline silicon (mc-Si) is still used to produce commercial silicon solar cells, despite the dominance of single crystal silicon cells imposed by the extraordinary increase in silicon cell production volume. Multicrystalline silicon varies significantly in grain size and quality from supplier to supplier, depending on the method followed in its fabrication and casting. The surface of a non-textured mc-Si wafer includes grains with a single crystallographic orientation, which have sizes up to or larger than 10 µm. Grains of different crystallographic orientations are separated by grain boundaries. Such a non-textured surface, shown in the amplitude AFM image of Figure 6, is relatively rough with a topography that leads to reduced reflection, compared to polished single crystalline silicon, but still not rough enough to exclude texturing. After etching for 20 minutes in a 1% KOH solution at 85°C some grains show successful high density pyramidal hillock formation, as confirmed in the AFM amplitude image of Figure 7 (a), which is indicative of a (100) orientated grain.

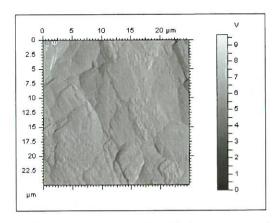


Fig. 6. AFM amplitude image (25 µm scan size) of a bare non-textured mc-Si surface.

The size of the pyramidal hillocks is close to what is obtained in (100) c-Si wafers after texturing at 80°C. On the other hand, adjacent grains which are not (100) oriented did not show hillocks as depicted in Figure 7(b), which after texturing, still show practically the same configuration before texturing as displayed in Figure 6. These results are confirmed in the SEM microphotograph as displayed in Figure 8, showing the border between two adjacent grains. After texturing in KOH solution, one of the grains contains very clear pyramidal hillocks, while the other still shows the initial rough topography of the mc-Si surface.

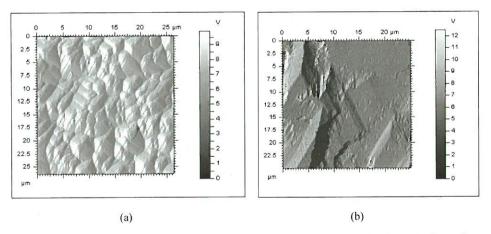


Fig. 7. AFM amplitude image (25 μm scan size) of a mc-Si surface textured at 85 °C (a) focused on a textured grain (b) focused on a non-textured grain

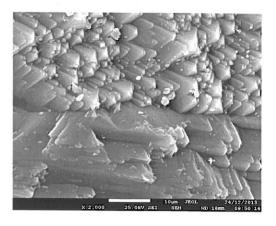


Fig. 8. SEM image with 2K magnification of multi- c-Si after texturing in 1% KOH solution at 85°C focused on a transition area between two adjacent grains; one of them is (100) oriented and the other has a different orientation

#### Optical characterization

An optical characterization study related to the measurement of surface reflection of different c-Si and mc-Si, textured and non-textured, with and without saw damage removal and with and without ARC, is carried out using a Shimadzu SolidSpe-3700 spectrophotometer including an integrating sphere in the wavelength range 200-1200 nm. The resulting total surface reflectance including specular reflection and diffuse reflection is plotted in Figure 9, as a function of wavelength for all the samples under investigation. The reference reflectance is that of bare polished c-Si traditionally known to be in the 34% to 40% in the visible wavelength range with a measured minimum reflectance around 30%, as depicted in Figure 9. On the other hand, the reflectance of the bare mc-Si wafer is around 22% in the 800-1000 nm wavelength range due to the multigrain structure, as discussed earlier.

Minimum and most uniform reflectance in the range of wavelength under interest is observed for c-Si wafers that received initial saw damage removal in 30% KOH solution then textured in 1% KOH solution at 80°C. Although, as will be shown in Table 1, the absolute minimum is slightly smaller for wafers that did not receive a saw damage removal, the minimum reflectance extends to a wider wavelength range in wafers that received a saw damage removal and is smaller in the short to medium wavelength range (400-600 nm), which contains a significant part of the solar spectrum, easily absorbed in the cell, and hence should not be left out. The small discontinuities appearing in the reflectance curves, especially when the reflectance is high, is an artefact of the measurement due to the change of the detector at a wavelength of 1000 nm.

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# Impact of etching (texturing) temperature on the minimum reflectance

The minimum measured reflectance averaged over three different positions on the sample is listed in Table 1, and displayed in Figure 10, as a function of the etching (texturing) temperature. The reflectance from the c-Si surface textured in 1% KOH + IPA solution decreases with increasing temperature and reaches a minimum of 7.1%, when the etching temperature reaches 80°C, and starts to increase again with further increase in etching temperature, probably due to the formation of bigger structures, or to the merging of neighbouring pyramids. Under the same texturing conditions the minimum reflectance of the mc-Si surface is 20%, while a lower value slightly less than 19% could be achieved when the texturing is carried out at 90°C, due to the contribution of (100) oriented planes and other surface planes with angular proximity to the (100) orientation on the mc-Si surface.

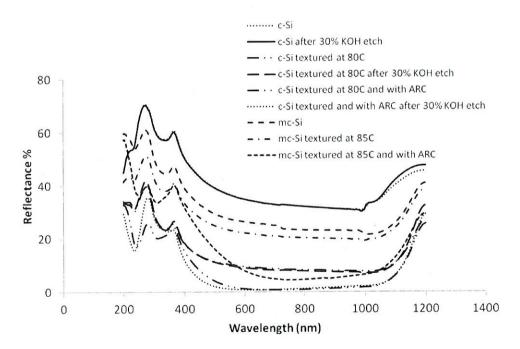


Fig. 9. Reflectance spectra of: 1) bare c-Si and bare mc-Si, 2) textured c-Si and textured mc-Si (at 80°C), 3) textured c-Si and mc-Si + ARC

# Impact of antireflection coating on the minimum reflectance

A thermal silicon dioxide  $(SiO_2)$  layer is used as an antireflection coating and designed to give a minimum reflection in the wavelength range 600-700 nm, where the solar spectrum peaks. The optimum thickness of the  $SiO_2$  layer is given by  $\lambda/4n$ , where

n=1.46 is the SiO<sub>2</sub> refractive index, leading to an optimum thickness of 110-115 nm. Such an oxide is grown in a quartz tube furnace at 1000°C in dry oxygen ambient for 150 min and produced effectively a uniform 115 nm thick blue oxide film on the surface of c-Si wafers. On the other hand, the thickness of the oxide grown on the mc-Si surface is not ideally uniform due to the different growth rate of oxide on grains with different crystallographic orientations. Its thickness, however, still lies in the same range 110-130 nm.

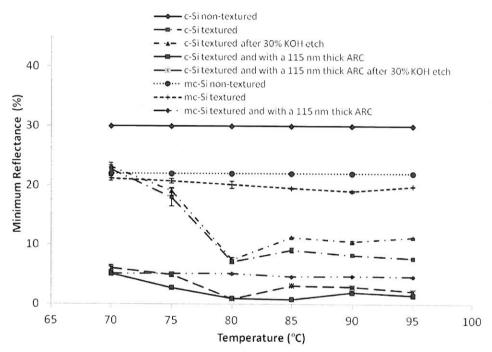


Fig. 10. Minimum reflectance as a function of the temperature of the etching solution for c-Si and mc-Si surfaces with and without Antireflection Coating (ARC).

As depicted in Figure 10 and Table 1, textured c-Si surface covered with ARC results in a minimum reflectance of 0.8%, when the texturing is carried out in the range 80-85°C. On the other hand, as can be seen in Table 2, optimum texturing temperature slightly shifts to the higher range 85-95°C for mc-Si surface and results in a minimum reflectance of 4.6%, which is not low enough for silicon solar cells. This value may differ from supplier to supplier depending on the grain composition of the surface. Therefore, in general, other methods of surface texturing should be administered for texturing mc-Si surfaces for solar cells such as acidic etching, reactive ion texturing, plasma texturing, or mechanical texturing.

Table 1. Minimum values and standard deviations for the reflectance from textured c-Si surfaces with and without ARC for various texturing solution temperatures

	c-Si textured		c-Si textured after 30% KOH etch		c-Si textured and with ARC		c-Si textured and with ARC after 30% KOH etch	
Temp	Minimum reflectance	std error	Minimum reflectance	std error	Minimum reflectance	std error	Minimum reflectance	std error
70	22.690	1.107	23.170	0.189	5.097	0.129	6.049	0.510
75	18.042	1.546	19.144	0.378	2.740	0.267	4.975	0.402
80	7.143	0.321	7.453	0.348	0.940	0.004	0.884	0.001
85	9.102	0.390	11.230	0.038	0.797	0.023	3.085	0.037
90	8.238	0.224	10.503	0.149	1.943	0.056	2.891	0.071
95	7.697	0.070	11.238	0.058	1.429	0.018	2.117	0.009

Table 2. Minimum values and standard deviations for the reflectance from textured mc-Si surfaces with and without ARC for various texturing solution temperatures.

	mc-Si te	xtured	mc-Si textured and with ARC		
Temp (°C)	Minimum reflectance	std error	Minimum reflectance	std error	
70	21.205	0.460	5.176	0.225	
75	20.706	0.385	5.134	0.110	
80	20.127	0.590	5.104	0.086	
85	19.502	0.107	4.596	0.018	
90	18.987	0.201	4.703	0.049	
95	19.818	0.052	4.591	0.062	

#### CONCLUSIONS

Alkaline texturing of (100) oriented crystalline Si and multicrystalline Si wafers in diluted 1% KOH with IPA solution are investigated. The interest in diluted solution is expressed, because 1) it results in a very high density of pyramidal hillocks leading to effective reduction in the front surface reflection, 2) it has a slow etch rate which is appropriate for controlling the size and distribution of the texture, and 3) it consumes a much smaller amount of chemicals. Etching at 70°C results in partial nucleation and in a very low surface coverage with pyramidal hillocks that develop completely after 20 minutes reaching a height of 2.5 μm. Full coverage of the surface with pyramids is achieved on c-Si is carried after 20 minutes etching at 80°C, with pyramids 3 µm high formed with an etch rate of 0.15 μm/min. The same results after texturing can be applied to (100) oriented c-Si surface that has received a saw damage removal

in a 30% KOH solution prior to texturing with a much smaller pyramidal hillocks very densely distributed on the surface. The minimum reflectance from textured c-Si surface covered with an optimally thick SiO, ARC amounts to 0.8% with a more uniform distribution over a wider wavelength range for the wafers that received saw damage removal etch prior to texturing.

On the other hand, mc-Si exhibits an initial reflectance of 22% due to large surface roughness. Only specific grains with (100) orientation or close are significantly affected by the etching solution, resulting in a reflectance drop to 19% after texturing. Applying a 115 nm thermally grown SiO, antireflection coating results in a minimum reflectance of 4.6% for mc-Si textured at 85°C.

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