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Dual buffers optical based packet switch incorporating arrayed waveguide gratings

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ABSTRACT

Optical packet switching is an upcoming and promising technology that can be used in optical data centers and in next generation data transfer due to the enormous bandwidth of optical fiber. In recently proposed OPS design to resolve contention among packets fiber delay lines (FDLs) based buffering is preferred choice. In this paper, a dual buffer based optical packet switch design is proposed, where buffer sizes are chosen intelligently thus allowing storage of large number of contending packets within limited buffer storage. Hence, using a limited number of FDLs very low packet loss rate is possible.Through simulations, it has been shown that at the load of "0.9" a very low packet loss rate of the order of "10^{-10}" is possible.To the best of our knowledge, this is the lowest packet loss rate using FDLs till date in any switch design.The proposed switch design is also compared with recently published designs to prove its superiority over other designs. The analysis of the switch is done in terms of power budget analysis, cost analysis, and packet loss performance under different buffering conditions.

Keywords: OPS, FDL, Data Centers, SOA.

INTRODUCTION

In the next generation, optical switch will play a major role not only in data transfer but also in data center applications. In data center applications communication distance is of some meters, while in optical networks distance can grow up to some thousands of kilometres. Therefore, in data center applications physical layer impairments are not so important.However, low packet loss is equally important in both data centers and optical networks. In optical switching, unavailability of optical RAMs is major setback. To solve this problem various alternatives are discussed in the literature(Singh et al., 2007, Pattavina et al.,2005, Singla et al.,2010, Singla et al., 2011, Kao et al., et al., 2010, Saha et al., 2012, Saha et al., 2012, Ye et al.,2011, Liet al., 2008, & Srivastava et al.,2010). "These include wavelength conversion, deflection routing, and buffering of contending packets in fiber delay lines", currently used as an alternative of random access memory (RAM). In fiber delay lines buffering duration of packets is limited due to the accumulated loss/noise in the buffer, as buffer is created along with some additional components (Srivastava et al., 2010). Due to the accumulation of impairments packet in the re-circulating buffer can stay for some fixed number of revolutions known as re-circulation limit. The re-circulation limit in the buffer thus also puts a limit on the number of stored packets (Srivastava et al., 2009).Thus, buffer cannot be scaled easily. As a second choice recently electronic buffering is proposed, where contending packets are stored in electronic RAMs; thus packets can remain in the buffer for longer duration without any signal power degradation (Yin et al., 2013). However, extra overhead in terms of O/E/O needs to be paid and speed limitation of electronic devices also comes into picture. Moreover, as each packet needs to be processed separately thus components like Demux and Mux are needed. The power required for the correct reception at the output also increases in comparison with optical buffering.

In optical packet switches design, two most important factors that we look for are as follows:

1) Effect of noises should be as small as possible so switch can operate at lower power.

2) Packet loss rate should also be lower.

However, to obtain low packet loss optical buffering of contending packets is proposed; this leads to accumulation of more noise. Hence, these two requirements are inversely related, and thus most of switch design fails to meet these requirements.

In optical packet switching, buffering of contending packets has been an intensive area of research for past many years. The hunt is still on for the replacement of electronic memory with optical counterpart. Slow light devices and FDL are considered as viable solution for the replacement of optical buffers. Slow light devices introduce large attenuation in signal power and are thus in-efficient.Unfortunately, as a feasible alternative solution, fiber delay lines-based buffer is only choice. Fiber delay lines-based buffer is created in three different configurations: feed-forward(Singh et al., 2007), feed-backward (Srivastava et al.,2010), and re-circulating type buffer (Srivastava et al.,2009). In these three configurations, re-circulating type buffer is the most preferred choice. In re-circulating type buffer, packets are stored in a single piece of fiber, using WDM techniques. However, for controlling, and read/write operations each wavelength is processed separately. To carry out these functionalities Demux and Mux, sometimes splitter and combiner along with SOAs/TWCs are used. To compensate the losses of optical components EDFA or SOA isused.

In addition to these, other limitations are as follows:

1. Packet can be read out from the buffer only at integral multiple of slots durations. Thus, random access is not possible.

2. Large size buffer is not feasible, due to bulky nature of FDL and re-circulation counts.

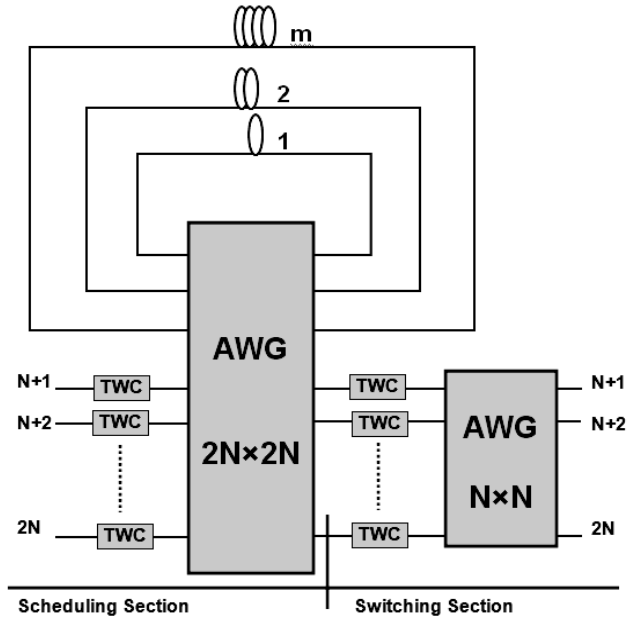
In high speed data applications where packet loss rate of the order of 10^{-9} is desired, hundreds of buffers will be needed or in other words same number of allowed re-circulations(Ye et al.,2011, Liet al., 2008). Therefore,to support these many re-circulations, packets need to be regenerated either by all-optical or by O/E conversion. Both of these methods will increase the complexity.

In this paper, dual buffer based optical switch is proposed; here optical buffer is designed very efficiently to achieve very low packet loss rate even at very higher loads.

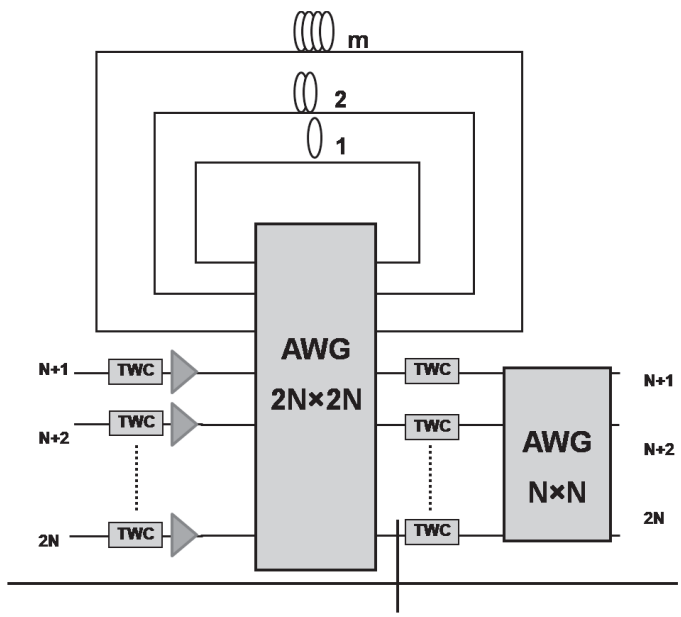
RELATED WORK

In the past many optical switch designs have been proposed and investigated. These architectures have their own pros and cons. Recently AWG based switch designs have gained attention due to the wavelength-based routing capability of AWG. A very efficient buffering based optical switch was proposed by R. Srivastava et al. (2010); later on this design is further investigated by many researchers. In 2013, H. Rastegarfaretal. proposed modifications to make buffer re-circulating(Rastegarfar et al.,2013, Rastegarfar et al., 2014). In (Shukla et al.,2016, Shukla et al.,2014,Shukla et al.,2016) placement of SOA in R. Srivastava design (Srivastava et al.,2010) is proposed and analysis is done to obtain the best possible position for placement of SOA. The comparison of two designs mentioned above (R. Srivastava and H Rastegarfar) is done in Shukla et al. (2016).

The switch designs proposed by R. Srivastava et al. (2010) and Shukla et al.(2016) are shown in Figure 1. In these designs in each fiber delay lines using WDM a maximum of N packets can be stored one for each output port. Moreover, buffer is created using pieces of fiber only without using any additional components. Thus, signal quality degradation is very less inside the buffer. In these designs packets leave the buffer on the same wavelengths at whichthey were stored; thus they will appear at the various ports of the scheduling AWG, whereby tuning their wavelengths appropriately packets can be sent to the destined outputs. In these architectures low packet loss is possible, and all the packets are stored in FDLs. The drawback of the architecture is its limited storage (m_{max}=N) and packet cannot be stored for longer duration.In Shukla et al. (2016), SOA is included at the input of the switch to compensate physical loss of the switch components; therefore received signal is much superior to R. Srivastava et al. (2010) design.



(a)



(b)

Figure 1: (a) Design of AWG based Switch (S_0) (Srivastava et al.)
(b) Design of AWG based Switch (S_1) (Vaibhav et al.).

PROPOSED DESIGN

The proposed switch design is shown in Figure 2. In the proposed modification, two AWGs based scheduling sections are combined. In the first AWG section buffering of delay lines varying form '0' to '9' slots with increment of unit slot is considered, while in the second section buffering of delay lines of '10' to '100' slots with increment of 10 slots is used. Thus, buffering delay can be written as

$$B_u^2 = \left(1 \times p + 10 \times q\right) \tag{1}$$

where $1 \le p \le 9$ and $1 \le q \le 10$ and with maximum buffering of 109 slots. Thus, using different buffer combinations delay of different slots ranging from 1 to 109 can be obtained. Using multistage design buffering can be increased exponentially; for example, three-stage buffer can be defined as

$$B_u^3 = \left(1 \times p + 10 \times q + 10^2 \times r\right) \tag{2}$$

where, $1 \le p \le 9,\ 1 \le q \le 9$ and $1 \le r \le 10$ with maximum buffering of 1099 slots.

The length calculation is important as length of the fiber will account to buffering time and total physical loss suffered by packets. In this design slot duration is equal to packet duration and it also includes duration of guard band. Hence, length for unit slot duration is

$$L = \frac{cb}{nB_r} \tag{3}$$

The above parameters are defined in Table 2. The maximum length of the fiber in loop 1 is 9*L* in loop 1 and in loop 2,100*L*.

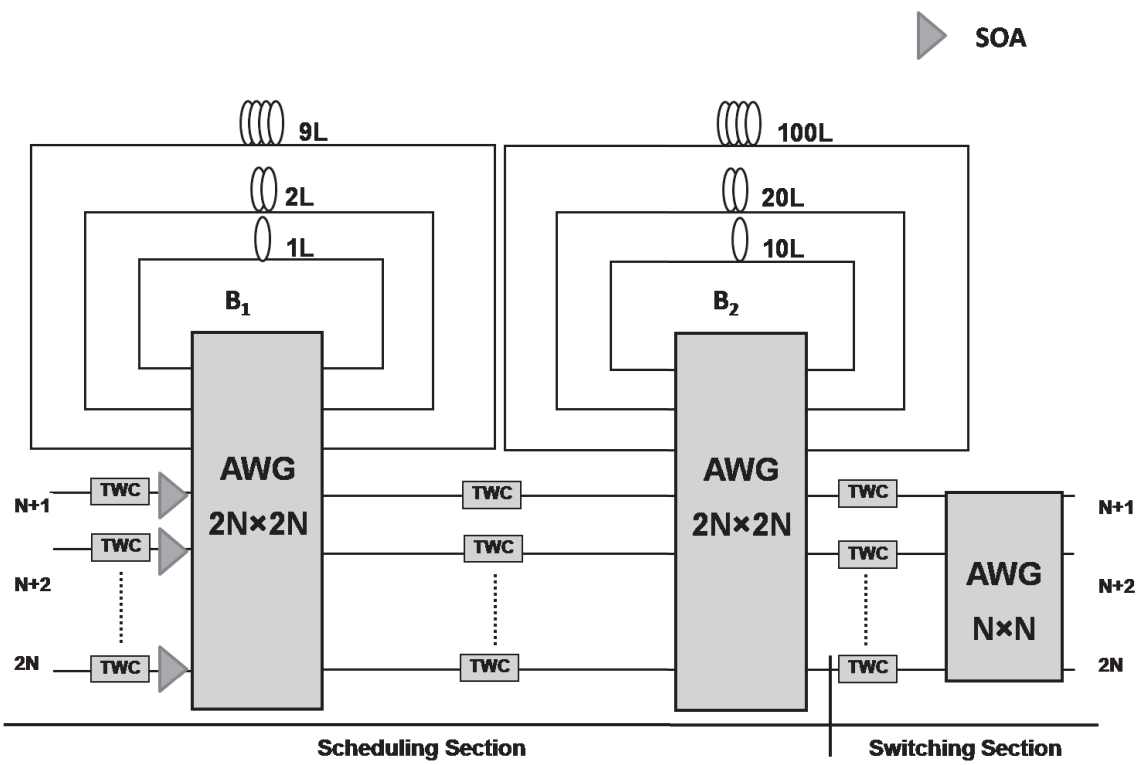


Figure 2. Proposed Design of AWG based Switch (S2).

The size of the first scheduling AWG is $2N \times 2N$, while actual switch size is $N \times N$; out of the rest of input N ports only 9 ports are chosen for connecting buffer FDLs, while the rest of the *N-9* ports are left free.Similarly, in the second scheduling AWG, *N-10*, ports remain vacant. The principle of operation of switch is similar to switch (S_1) except the additional stage for buffering of larger delay buffer.

The TWCs placed at each input port of the scheduling and switching AWGs are used to convert the wavelength of the incoming packets as per control unit decision, either to switch them in the appropriate FDL in buffer or to direct them towards the correct output ports. Consider a situation that, for a particular output port *j, k*-1 packets are stored in buffer, and at the inputs for the same tagged output j two packets arrive, one packet from the buffer will leave and incoming packets will be placed in the buffer module, which provides a delay of k slots. Here, for a packet arriving at input '*i*', would be assigned a wavelength using the relation

$$\lambda(i,k) = \lambda_{[1+(i+k-2) \bmod N]} \tag{4}$$

After the delay of 'k' time slots the buffered packet will re-appear at the input port of scheduling and due to cyclic nature of AWG it gets directed to the output port 'i' of the scheduling AWG, here either it will be placed in second buffer of longer delays or it will be forwarded towards the appropriate output 'j' using TWC of switching section.

The SOA placed next to input TWC fully compensate the losses of different components,and SOAs also adjust their gain for buffered and straight through packets. The analysis of the switch is done in terms of BER at different power levels and packet loss probability.

ANALYSIS OF SWITCH

To make fair comparisons among the switches designs, in this paper power budget analysis, packet loss probability analysis, and cost analysis are presented.

POWER ANALYSIS

In this section, loss and power analysis are proposed; here the insertion loss of the components is represented by '*L*' with superscript denoting the size and subscript denoting the component type. The total loss is modelled as '*A*', direct path,'*D*', optical buffered path,'*B*'.

Analysis for switch architecture S_1

The loss of the signal power passing through directly towards the output is

$$A_T^D = L_{TWC} L_{SOA} L_{AWG}^{2N} L_{TWC} L_{AWG}^{N} \tag{5}$$

The loss of the signal power passing through optical buffer is

$$A_T^B = L_{TWC} L_{SOA} L_{AWG}^{2N} L_b L_{AWG}^{2N} L_{TWC} L_{AWG}^{N} \tag{6}$$

Thus, the power available at the output of the switch is

$$P_{out} = P_{in} + n_{sp}(G_1 - 1) h\nu B_0 A_T^i / L_{TWC} = P_s + P_{sp} \tag{7}$$

where '*i*' can be D or B depending on direct or buffer transfer.

Analysis for switch architecture S_2

The loss of the signal power passing through directly towards the output is

$$A_T^D = L_{TWC} L_{SOA} L_{AWG}^{2N} L_{TWC} L_{AWG}^{2N} L_{TWC} L_{SOA} L_{AWG}^{N} \tag{8}$$

Thus, the power available at the output of the switch is

$$P_{out}^{D} = P_{in} + n_{sp}(G_1 - 1)h\nu B_0 A_T^D / L_{TWC} = P_s + P_{sp} \tag{9}$$

Similarly, the loss of the signal power when packet passes through the optical buffer is

$$A_T^B = L_{TWC}L_{SOA}L_{AWG}^{2N}L_{B1}L_{AWG}^{2N}L_{TWC}L_{AWG}^{2N}L_{B2}L_{AWG}^{2N}L_{TWC}L_{SOA}L_{AWG}^{N} \tag{10}$$

The output power is

$$P_{out}^{B} = P_{in} + n_{sp}(G - 1)h\nu B_0 A_T^B / L_{TWC} = P_s + P_{sp} \tag{11}$$

NOISE ANALYSIS

Due to the beating phenomenon at the receiver various components are generated, which are shot noise, spontaneous-spontaneous noise, signal-spontaneous noise, shot-spontaneous noise, and thermal noise whose variances are defined below:

$$\begin{aligned}
\sigma_s^2(b) &= 2eRP_sB_e \\
\sigma_{sp-sp}^2 &= 2R^2P_{sp}(2B_0 - B_e)\frac{B_e}{B_0^2} \\
\sigma_{sig-sp}^2(b) &= 4R^2P_sP_{sp}\frac{B_e}{B_0} \\
\sigma_{s-sp}^2 &= 2qRP_{sp}B_e \\
\sigma_{Th}^2 &= \frac{4K_BTB_e}{R_L}
\end{aligned} \tag{12}$$

The total noise variance can be obtained as

$$\sigma^2(b) = \sigma_s^2(b) + \sigma_{s-sp}^2 + \sigma_{sp-sp}^2 + \sigma_{sig-sp}^2(b) + \sigma_{Th}^2 \tag{13}$$

Finally, BER can be obtained as

$$BER = Q\left[\frac{I(1) - I(0)}{\sigma(1) + \sigma(0)}\right] = Q\left[R\left(\frac{P(1) - P(0)}{\sigma(1) + \sigma(0)}\right)\right] \tag{14}$$

$Q(x)$ is theerror function. AWG specifications are given in Table 1. The description of the above parameters with typical values is detailed in Table 2.

CALCULATIONS AND RESULTS

In this section, various calculation and results are presented. The list of parameters and their details with considered values are shown in Tables 1 and 2.

UNIT SLOT LENGTH AND LOSS CALCULATION

Considering 1500 bytes packet at the data rates of 40 Gbps, its equivalent unit slot fiber length is 62.06 meter. Thus, the maximum length would be of 6.21 km; thus maximum attenuation via fiber would be 1.24 dB.

In case of optical buffering for direct transfer of packets the loss suffered is 16 dB. In case packet passes through the buffer the loss suffered is 23.36 dB.In BER analysis, results are obtained for the packet that passes through buffer, to obtain worst BER; as for directly transmitted packet BER will be much superior in comparison to buffered packets.

RESULTS

In Table 3, power vs. BER for buffered packets is shown.In this table power is considered in sub-micro watts. Here, as the input optical power increases, the BER improves. In the switch S_1 to attain acceptable BER≤10^{-9}, minimum power is 0.3 µW and for switch S_2 minimum amount of required power is 0.6 µW. Similarly, for BER≤ 10^{-12}, minimum amount of required power is 0.4 µW and 0.8 µW for switches S1 and S2 respectively. Therefore, it can be inferred that required amount of power doubles in S2 in comparison to S1with a buffering gain of 6.81 times. This increase in buffering leads to a significant decrease in packet loss probability as detailed in the later part of the paper.

Table 1. AWG Specifications

Specification	Value
Total Supported Channels	40
Channel Spacing	100 GHz
Insertion loss	3.0 dB
Channel Crosstalk (Adjacent)	26 dB

Table 2. Parameters specifications (Srivastava et al., 2009).

Parameters	Value
Switch size (N)	16
Population inversion factor (n_{sp})	1.2
Gain of the SOA (G)	20dB
Speed of light (c)	3×10^{8} *m/s*
Number of bits in a packet (b)	12000
Bit rate (B_r)	varies
Refractive index of fiber (n)	1.45
Responsivity (R)	1.28 A/W
Electronic charge (e)	1.6×10^{-19} C
Electrical bandwidth (B_e)	20GHz
Optical bandwidth (B_o)	40GHz
TWC insertion loss (L_{TWC})	2.0 dB
Loss AWG (32 channels) (L_{AWG})	3.0 dB
Loss of the fiber (L_F)	0.2 dB/km
Loss of SOA (L_{SOA})	1 dB
Module (m)	19
Buffer (B)	109
Planck Constant (h)	6.6×10^{-34} Js
Boltzmann Constant (K_B)	$1.3810/^{-23}$ $m^2Kgs^{-2}K^{-1}$
Temperature (T)	300 K
Load Resistance (R_L)	300 K

Table 3. Power vs. BER for buffered packets.

Power (*n*W)	BER (S_1)	BER (S_2)
100	0.0011	0.0237
200	1.53×10^{-06}	7.67×10^{-04}
300	6.44×10^{-11}	2.57×10^{-05}
400	2.16×10^{-12}	8.55×10^{-07}
500	2.36×10^{-15}	2.81×10^{-08}
600	2.48×10^{-18}	9.14×10^{-10}
700	2.52×10^{-21}	2.94×10^{-11}
800	2.49×10^{-24}	9.36×10^{-13}
900	2.42×10^{-27}	2.95×10^{-14}
1000	2.30×10^{-30}	9.27×10^{-16}

COST ANALYSIS

In any device cost is in an important parameter; however due to lack of commercialization of few components a standard cost estimation is not feasible. Therefore, for relative measurement of the cost two models of FCC based on fiber-to-chip coupling (Caenegem et al., 2006) and WSU, which accounts for wavelength speed-op factor (Eramo et al., 2008) for tunable device, are used. Under WSU the cost of each TWC having tunability of '*d*' wavelengths is given.

$$C_{TWC} = (d)^b \tag{15}$$

Here, '*d*' is the conversion range and b is cost speed-up factor. The values b lies between 0.2 to 1. The cost using FCC model is evaluated by courting input and output fiber coupled to chip/device, for example, cost of *N×N, AWG is N+N=2N*.

Using WSU for TWC and FCC for other components, the cost of switch design S_1 is

$$C_{S_1}^T = C_{TWC} + C_{AWG}^{2N\times2N} + C_{B1} + C_{TWC} + C_{AWG}^{N\times N} \tag{16}$$

$$C_{S_1}^T = Na(2N)^b + Na(N)^b + 6N + 2m \tag{17}$$

Considering maximum value of *m*, then we get

$$C_{S_1}^T = Na(2N)^b + Na(N)^b + 8N \tag{18}$$

The cost of switch design S2 is

$$C_{S_2}^T = C_{TWC} + C_{SOA} + C_{AWG}^{2N\times2N} + C_{B1} + C_{TWC} + C_{AWG}^{2N\times2N} + C_{B2} + C_{TWC} + C_{AWG}^{N\times N} \tag{19}$$

$$C_{S_2}^T = 2Na(2N)^b + Na(N)^b + 12N + 38 \tag{20}$$

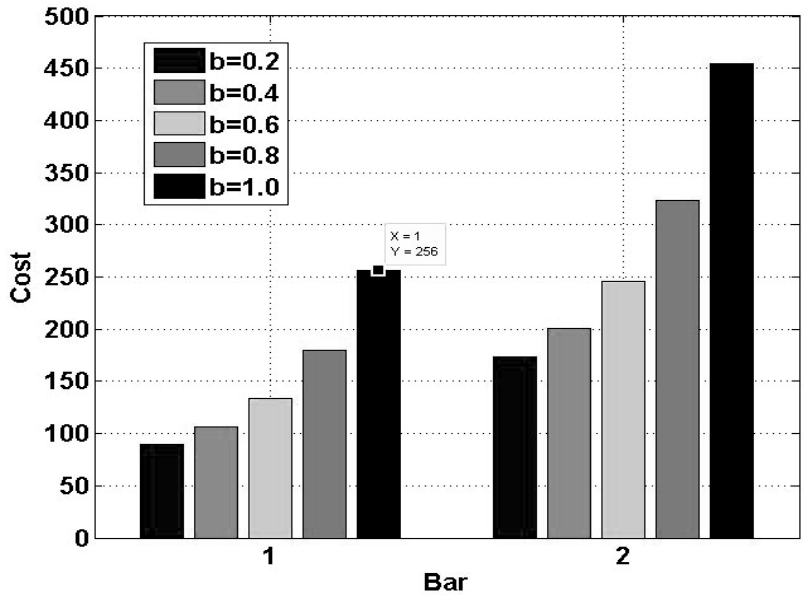


Figure 3. Cost comparison of switches.

The set of bar-1 represents the single stage switch (S_1); set of bar-2 represents the dual buffer switch (S_2) cost for various values of *b*,and the value of *b* ranges from 0.2 to 1. The cost of switch S_1 for *b* equal to 0.2 is 90.05 and for *b*=1 it is 173.98. The cost of S_2 is 84.32% higher than S_1. For *b*=1, the cost of S_1 is 256 and for S_2 is 454, and thus the cost of S_2 is 76.65% higher than cost of S_1.

SIMULATION RESULTS

In general telecommunication network can be thought as users who generate demands for network resources and protocols control the network resources and fulfil the demand. This generation of demand and network resources allocation needs to perform via simulation. This event-based method is known as discrete event simulation(DES). DES simulation is based on time increment.The performance of the switch in terms of packet loss is done using DES, while performing Monte Carlo simulation.

BERNOULLI PROCESS

Bernoulli process is discrete time version of Poisson process. Here the probability of arrival of packet in any time slot is '*p*' and is independent of other packets arrivals. Each packet can select any one of the switch output with probability '*1/N*'. Thus the probability that a generated packet will select particular output is '*p/N*'. It clearly follows that for '*k*'slots the process is binomialand arrival of k packets for tagged output is given by

$$P(N_k = k) = \binom{N}{k}\left(\frac{p}{N}\right)^k \left(1-\frac{p}{N}\right)^{N-k} \text{ where } 0 \le k \le N \tag{21}$$

The time between the arrivals is geometric with parameter '*p*'

$$P(A_n = j) = (p)(1-p)^j \tag{22}$$

'*j*' is non-negative integer.

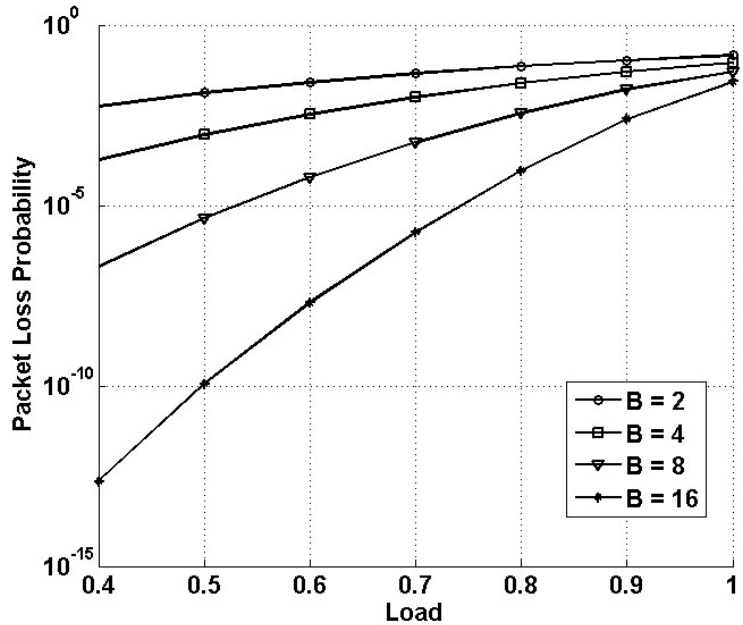


Figure 4. Loss probability vs load under various buffer combinations (S1).

In Figure 4, packet loss probability (plp) vs. load is shown for architecture S_1, while buffer varies from 2 to maximum value of 16. It can be interpreted that as the buffer size increases packet loss reduces. It is also evident from the figure that as load increases plp increases and as it crosses 0.8 mark, the plp for buffer size of16 is 10^{-4}.

In Figure 5, loss probability vs. load is plotted for architecture S2, while buffer varies. Here, very high load 0.9 to 1 is considered, while buffer size is varying from 40 to 100 with an increment of 20. It can be interpreted from the figure that at the load of 0.9, as we increase the buffer by 20, the plp improves by a factor of more than 10.

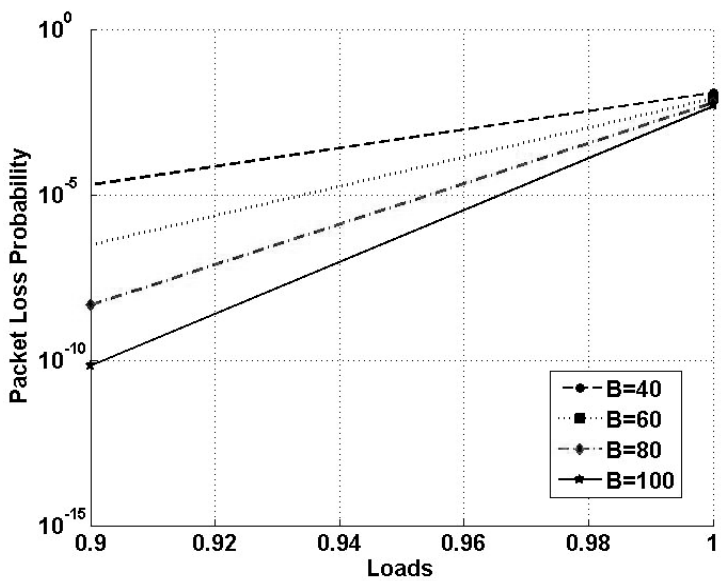


Figure 5. Loss probability vs load under various buffer combinations (S2).

It is also observable from the figure that as load increases and as it crosses 0.9 mark, the plp for buffer size of 40 is 10^{-5}, and similarly for buffer size of 100, plp is 10^{-10}. While in architecture S_1 at the load of 0.9, packet loss probability is 10^{-3}. Therefore, in plp an improvement of 10^7 is observed, which is huge in terms of packet loss rate.

Finally, in figure 6, comparison of recent switch designs is made in terms of packet loss probability. It is clear from the figure that proposed switch design outperforms previously published switch designs. Even at the load of 0.9, huge difference in packet loss probability is monitored.

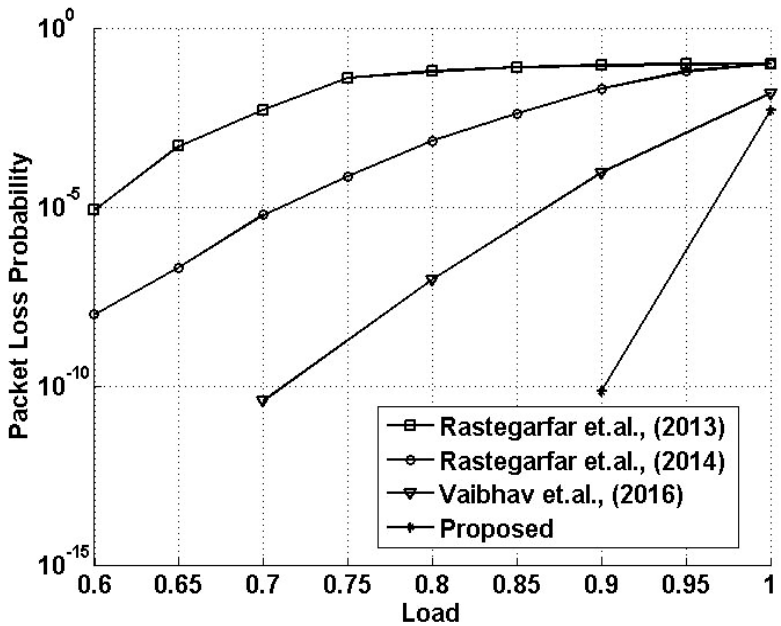


Figure 6. Comparison of recent switch designs in terms of packet loss probability.

BURSTY TRAFFIC

In reality traffic is composed of bursts. In general, the aggregation of packets leads to the burst generation. The arrival of packets is exponentially distributed, then a particular burst will have L packets within a fixed assembly time (t) and arrival rate (λ) has distribution as incomplete gamma function

$$f(t) = \frac{(\lambda t)^{L-1} e^{-\lambda t}}{(L-1)!} \tag{23}$$

Recently, a mechanism where control packet is released when first packet arrives for assembly with an estimation of burst length is proposed(Hernández et al., 2007). In this mechanism by the time burst assembles, tunable components of the switches are configured; thus overall delay reduces. In Singh et al. (2018) work it is shown that the early release of control packet with an estimate of burst length reduces delay. It is also shown that both over-reservation and waiting time can be kept small if burst length is kept equal to the mean of incomplete gamma function (Singh, et al, 2018). Thus, in case of bursty traffic FDL size can be fixed in advance with some over-reservation.

The simulation for bursty traffic arrival is done in MATLAB, considering meanburst length(λt) of 4 *(λ=1, t*=4), while for buffer full buffering capacity is considered. It is clear from the Figure 7 that even in case of bursty traffic arrival a significant difference in burst loss probability can be observed. Comparing the results at the load of 0.8, for switch S_1 burst loss probability is 5×10^{-2} while for proposed switch burst loss probability is 1.05×10^{-4}. Thus, burst loss rate is improved by a factor of nearly 476 times.

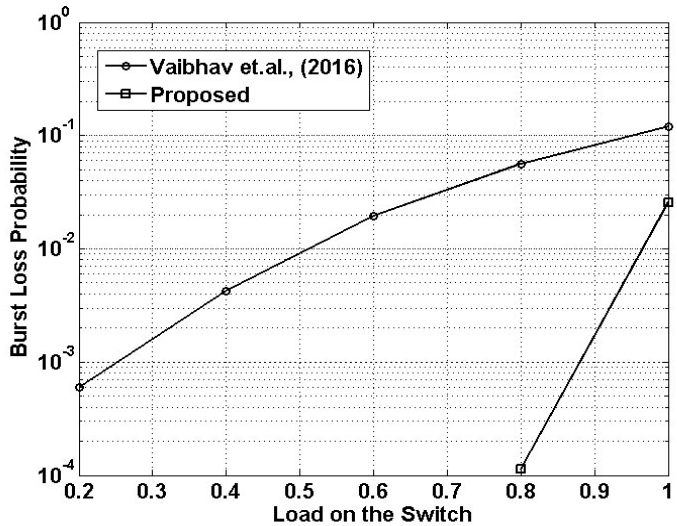


Figure 7. Comparison of recent switch designs in terms of packet loss probability.

COMPARISON OF SWITCHES

Finally, comparison of switches is presented in Table 4. In switch S_2 power doubles to maintain acceptable BER. The cost of switch S_2 is increased by 85%. The number of fiber delay lines increases from 16 to 19, while buffer size increases from 16 to 109. However, packet loss probability in case of random traffic at the load of 0.9 decreased by a factor of 10^7. Similarly, in case of bursty traffic model at the load of 0.8, burst loss is decreased by nearly 476 times.

To the best of our knowledge, at the load of 0.9, obtained packet loss rate is lowest among published switch design till date.

Table 4. Comparison of switches.

Parameters	Switch Design (S_1) (Shukla et al. 2016)	Proposed Design (S_2)
Power (BER≤10^{-9})	300 nW	600 nW
Power (BER≤10^{-12})	400 nW	800 nW
Cost (b=1)	256 units	454 units
AWGs	2	3
TWCs (Control points)	2N	3N
FDLs	N	19
Buffer	16	109
Packet loss probability (load =0.9)	10^{-3}	10^{-10}
Burst loss probability (load =0.8)	5×10^{-2}	10^{-4}

CONCLUSIONS

The design of efficient optical switch is an important problem not only in optical switching but also in optical data centers where optical switches can be used to connect Top of Rack (ToR) switches. The use of AWG in switch design makes them efficient. The proposed switch design is based on dual loop optical buffer, and loops are designed in such a way that using 19 FDLs variable delay from 1 to 109 slots can be obtained. In the proposed design at the expense of double power, and 85% higher in cost at the load of 0.9 the packet loss probability is 10^{-10} which is lowest among the published results till date.

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تحويل الحزم البصرية المرتكزة على التخزين المزدوج والمتضمنة موجهات مصفوفة

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الخلاصة

يُعتبر تحويل الحزم البصرية تقنية واعدة يمكن استخدامها في مراكز البيانات البصرية وفي نقل البيانات في الجيل القادم نتيجة لوجود نطاق هائل من الألياف البصرية. في تصميم OPS المُقترح حديثاً لحل التنافر بين الحزم، يكون التخزين المؤقت القائم على FDLs هو الخيار المُفَضل. في هذا البحث، تم اقتراح تصميم محول حزم بصرية مرتكز على التخزين المزدوج، حيث تم اختيار أحجام المخازن بذكاء، مما يسمح بتخزين عدد كبير من الحزم المتنافرة داخل مخزن مؤقت محدود. وبالتالي، فإنه باستخدام عدد محدود من FDLs، يكون معدل فقدان الحزم منخفض للغاية. ومن خلال عمليات المحاكاة تبين أنه عند الحمل بقيمة ‹0.9›، يمكن تحقيق معدل فقدان منخفض جداً وهو ‘10^{-10}’. وهذا هو أدنى معدل فقدان للحزم باستخدام FDLs حتى الآن في أي تصميم للمحولات. كما تم مقارنة تصميم المحول الحالي مع التصاميم المنشورة مؤخراً لإثبات تفوقه عليها. وتم تحليل كل من ميزانية القدرة والتكلفة وأداء فقدان الحزم في المحول تحت ظروف التخزين المؤقت المختلفة.