

## **Design of ultra-low voltage CCII utilizing level shifting technique and a dual mode multifunction universal filter as an application**

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### **ABSTRACT**

This paper presents an implementation of Ultra low Voltage Second Generation Current Conveyor (ULV-CCII). The methodology adopted for the design is the use of level shifting stage to lower the effective threshold voltage of the PMOS differential pair transistors. The combination of conventional and level shifted P-MOS differential pairs together with low voltage folded cascode output stage was used to achieve almost rail to rail operation at an ultralow supply of  $\pm 0.4V$ . This approach also benefits from increased common mode range. The CCII provides voltage transfer bandwidth of 7.8MHz and the current transfer bandwidth of 17MHz, while dissipating a nominal power of 123  $\mu W$ . A versatile dual mode universal filter is realized to validate the functionality of the ULV-CCII. The filter is capable of working in both current and voltage modes without a change in its topology. The filter employs only two CCII, two capacitors, and two resistors. The use of only positive single input CCII simplifies the implementation and relaxes the matching constraints during layout, leading to enhanced filter performance. The filter works at  $\pm 0.4V$  supply and provides all standard filter responses in the voltage mode as well as low pass and band pass response for the current mode of operation. The H-spice simulation results in 0.18 $\mu m$  TSMC CMOS technology are presented to prove the results.

**Keywords:** analog filter; current mode; current conveyor; level shifting; low voltage.

### **INTRODUCTION**

The evolution of portable electronics and wearable biomedical devices has put a serious constraint on the maximum allowable supply voltage for the battery operated devices. Furthermore, with the development of energy harvesting techniques and solar powered devices, researchers are striving hard to integrate them with Low Voltage (LV) circuits (Faseehuddin et al., 2016; Sampe et al., 2016). The rapid scaling of CMOS technology has led to miniaturization of devices that has proven rewarding for digital systems but a challenge for their analog counter parts. The major issues faced by the analog designers are the deviation from the saturation characteristics in the submicron and deep submicron technologies, the non reduction of the threshold voltage of the MOSFETs with respect to the scaling factor, and decreased impedance levels leading to lower gain in the analog systems (Khateb et al., 2011). The operational amplifier is arguably the most versatile building block for analog design, but it has certain limitations such as constant gain bandwidth product and limited slew rate, which results in limited frequency of operation (Smith & Sedra,

1968). These limitations are further aggravated in LV regime. The current mode circuits on the other hand are found more attractive for LV operation and are characterized by high bandwidth, simple structure, high slew rate, simple design, and so on (Sedra et al., 1990; Wilson, 1990). The current conveyor is the most flexible among all current mode devices and since its introduction by Sedra et al., it has been utilized in a multitude of applications including filters and oscillators (Fasehuddin et al., 2016; Horng et al., 2011).

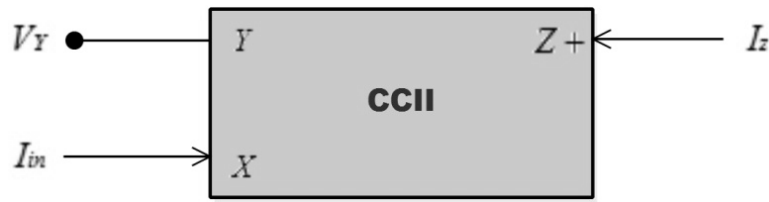
Dynamic range of the order of supply voltage is essential in low voltage environment to cater to the wide applications range. To achieve rail to rail operation, the most utilized technique is the use of parallel combination of n-channel and p-channel MOSFETs (Hwang et al., 1995). The use of complementary pairs coupled with innovative circuit techniques leads to constant and rail to rail common mode (CM) operation (Carrillo et al., 2003; Hogervorst et al., 1994; Lu & Yao, 2008). The applicability of this technique in LV regime has limitations due to extremely low supply voltage and the threshold voltage limitation which leads to signal distortion (Carrillo et al., 2003). Numerous device level and circuit level techniques have been proposed to achieve rail to rail operation that includes bulk driven MOS (Khateb et al., 2011), current driven bulk technique (Lehmann & Cassia, 2001), dynamic threshold MOS (Achigui et al., 2006), floating gate MOS (Khateb et al., 2012), quasi floating MOS (Kubanek et al., 2012), self cascode and level shifting (Huang et al., 2004), and so forth. In the bulk driven technique, the inputs are applied to the body of the MOS while their gates are tied to voltage enough to form an inversion layer (Khateb et al., 2011). This results in threshold voltage removal and achievement of rail to rail CM range at LV, but inherent low body transconductance, which is 3 to 4 times lower than the gate translates to low frequency operation. Furthermore, the input referred noise is increased and there is an upper limit on the bulk voltage to avoid excessive bulk leakage (Blalock et al., 1998). The floating gate and quasi floating gate techniques also exhibit low transconductance, consume large chip area, and require extra effort in layout design (Ramirez-Angulo et al., 2004). The most viable solution to procure LV operation would be to develop circuit level techniques utilizing gate driven MOSFETs. One such technique is level shifting the signal to appropriate level for achieving rail to rail operation.

In this research, P-MOS level shifted differential pairs are used to develop a second generation current conveyor working in ultra low voltage regime with high accuracy. First, the paper describes the basic principle utilized in the implementation followed by the complete circuit level implementation of ULV-CCII. Second, a Multi input single output (MISO) filter is proposed followed by the conclusion.

### **ULTRA-LOW VOLTAGE CURRENT CONVEYOR**

The second generation current conveyor is the most versatile current mode building block. It is basically a combination of voltage follower and a current follower. The V-I relationship and block diagram are given in matrix Equation 1 and Figure 1, respectively.

$$\begin{bmatrix} V_X \\ I_Z \\ I_Y \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$



**Figure 1.** Block diagram of CCII.

Numerous high performance implementations of the current conveyor can be found in the literature utilizing translinear loop or differential pair (Fabre et al., 1996; Surakamponorn & Kaewdang, 2014). The differential pair based implementation is the most suited for low voltage design. In differential pair design, the minimum allowable supply voltage restriction is imposed by the input differential pair stage, which equals  $V_T + 2V_{Dsat}$  where,  $V_T$  is the threshold voltage and  $V_{Dsat}$  is the over drive voltage. The most negative implication of LV supply is the reduction in the Common Mode range (CM). The CM ranges for n and p channel differential pairs are given in Equations 2 and 3. The most important challenge faced by the engineers is to achieve rail to rail input range at very low supply voltage. The most common practice utilized to provide rail to rail dynamic range is to connect n and p channel differential pairs in parallel. When the input voltage is closer to the negative supply p channel pair will be active, when the input voltage is near to positive supply n channel pair will be active and in the mid supply region both will be active. This results in variation with the input CM voltage, which is undesirable in addition extra circuits are needed to maintain constant leading to complexity and power dissipation. Moreover, the matching between the n and p channel pairs is of prime importance as the mobility of electrons ( $\mu_n$ ) is roughly 2 times higher than the holes ( $\mu_p$ ) and so to have a constant large signal behavior, we need to perform accurate geometric scaling. As is known that, and are temperature dependent and their effect on both pairs may not be equal leading to unbalancing and distortion. Furthermore, under LV voltage operation there exists a dead band where neither of the transistors are active leading to distortion. So this technique cannot be applied in LV regime. The solution is to use identical differential pairs for achieving the above mentioned objectives.

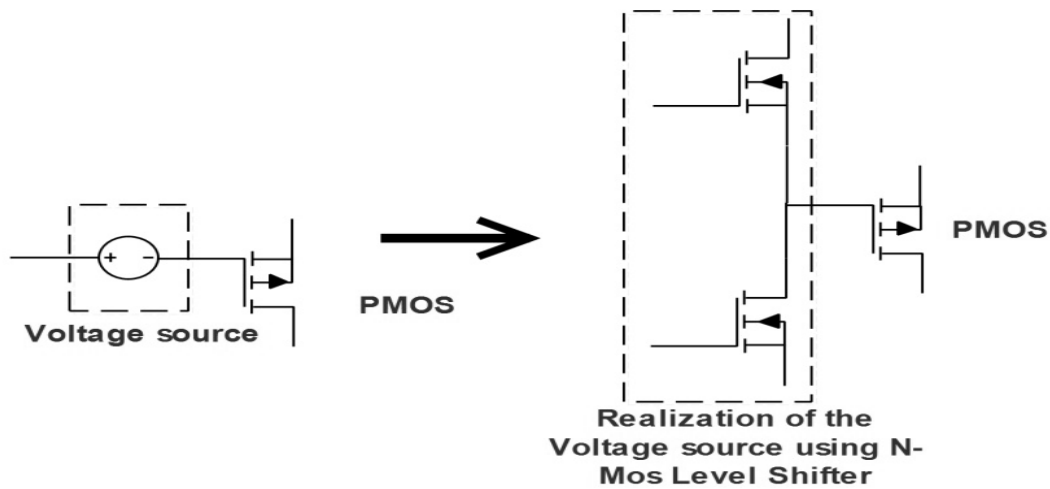
$$V_{SS} + V_T + 2V_{Dsat} \text{ to } V_{DD} \quad (2)$$

$$V_{DD} \text{ to } V_{SS} + V_T + 2V_{Dsat} \quad (3)$$

As can be inferred from Equations (2-3), if the threshold voltage can be reduced the rail to rail dynamic range and CM range can be achieved. The basic principle employed here to reduce the threshold voltage is extremely simple. If a voltage source is added with appropriate polarity at the gate of a P-MOS transistor, it results in the lowering of the threshold voltage. This happens as a result of the battery increasing the total applied voltage across the gate and source of the transistor. This increase can be visualized as a decrease in the effective threshold voltage and can be quantified as in Equation 4.

$$V_{Tnew} = V_T - V_{Sdc} \quad (4)$$

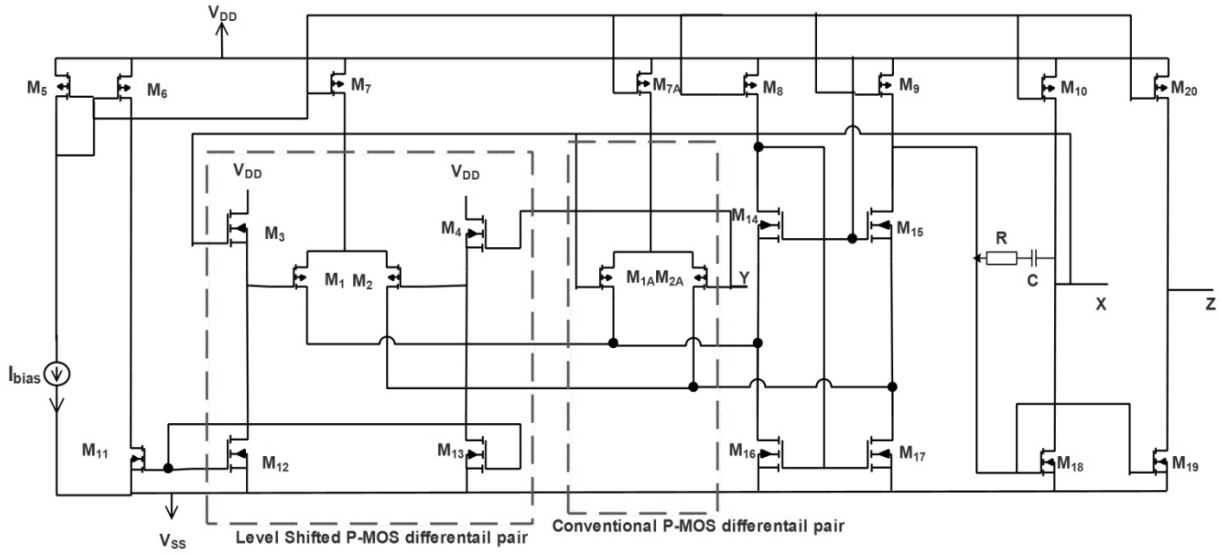
$V_{Tnew}$  is the new effective threshold voltage,  $V_T$  the threshold voltage of a conventional MOSFET, and  $V_{Sdc}$  is the dc voltage of the battery.



**Figure 2.** Threshold voltage lowering using level shifting transistor.

The transistor with reduce threshold will exhibit the same transconductance ( $g_m$ ) and output conductance of MOSFET ( $g_o$ ) as the normal transistor, and so this will not hamper the noise performance and frequency response. The voltage source can be implemented as common drain amplifier giving a voltage shift as shown in Figure 2 for P-MOS transistor. But this topology single handedly cannot obtain rail to rail operation, so for that we use a combination of level shifted differential and conventional differential pairs (Huang et al., 2004). The complete schematic of the ULV-CCII is depicted in Figure 3. The transistors M5 and M6 provide the bias current to the complete circuit. Transistors M3, M4, M12 and M13 form the level shifter stage. The transistors M1 and M2 are the P-channel differential pair, which along with the level shifter stage form the level shifted differential pair. The transistors M1A and M2A form the other conventional P-MOS differential pair. The transistors M7 and M7A provide the tail current to the level shifted differential pair transistors M1-M2 and conventional differential pair transistor M1A-M2A, respectively. Transistors M8 to M9 and M14 to M16 comprise the Folded-Cascode stage. The output stage is formed by transistors M10 and M18. The negative feedback to the X terminal helps in reducing the resistance leading to accurate voltage transfer. The current follower output stage is formed by transistors M19 and M20.

When the input voltage is near to the negative supply rail the differential pairs M1 and M2 will be working in saturation and the level shifter transistors M3 and M4 will be cutoff. When the supply voltage is near the positive supply, the differential pair M1A and M2A will be off, but now the pairs M1 and M2 will be working in saturation leading to a rail to rail operation. It is to be pointed out that in the mid supply region both pairs will be active leading to increased transconductance. The transconductance will not be constant, but as long as the loop gain is high enough this will not have a severe effect on the accuracy of the circuit (Madian et al., 2006).



**Figure 3.**CMOS implementation of level shifted low voltage CCII.

As the prime objective is to achieve low voltage operation Folded -Cascode stage is chosen for adding the currents from the differential pairs and to perform differential to single ended conversion as it exhibits low voltage compatibility, increased gain and higher common mode range (Dan&Xiaolin, 2010; Kun&Di, 2011).The miller compensation with zero nulling resistor is used to enhance the frequency response of the circuit.Due to the feedback the voltage gain between the X and Y terminals will be given by Equation 5.

$$A_v(s) = \frac{1}{1 + \frac{1}{G(s)}} \tag{5}$$

where  $G(s)$  is the gain of the OTA stages,for high values of  $G(s)$  the gain approaches unity. The output resistance of the cascode stage can be written as  $r_{out1}=r_{o9} \parallel$

$$[g_{m15}r_{o15}(r_{o17} \parallel r_{o2})] \tag{6}$$

The output impedance of the second stage of OTA and Z terminal can be evaluated from Equations (78-).

$$r_{out2} = \frac{1}{g_{oM18} + g_{oM10}} \tag{7}$$

$$r_{outz} = \frac{1}{g_{oM11} + g_{oM22}} \tag{8}$$

where  $g_o$  is the conductance of the transistors.

## SIMULATION RESULTS OF THE ULV-CCII

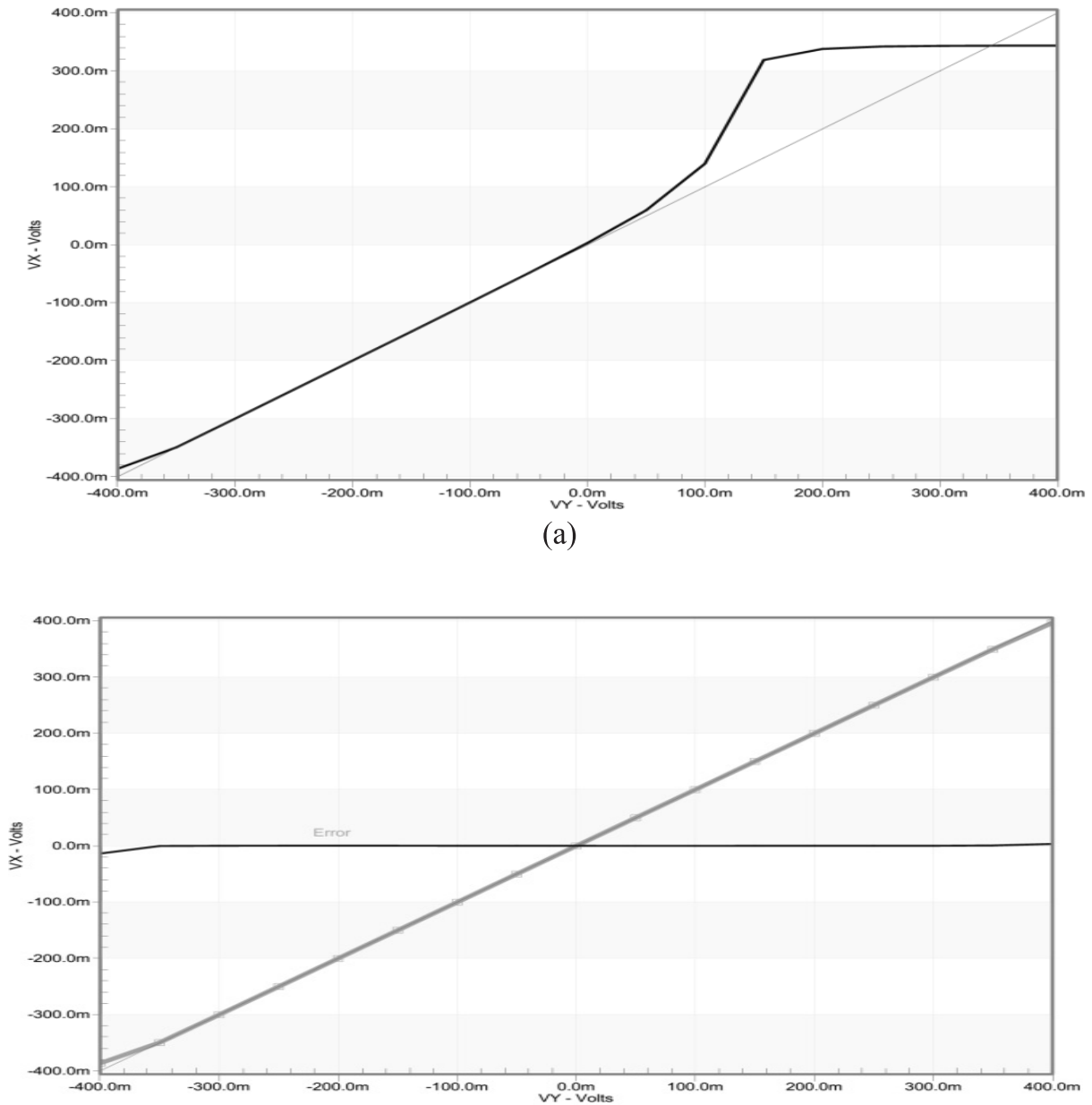
To validate the functionality of the ULV-CCII it is implemented in 0.18  $\mu\text{m}$  TSMC CMOS process and simulated in HSPICE. The functionality of the circuit was tested at  $\pm 0.4\text{V}$  supply voltage. The threshold voltages of NMOS and PMOS are 0.36V and -0.4V, and so in this technology the transistors can be kept in saturation at such a low supply voltage. The bias current is kept at 30  $\mu\text{A}$ . The aspect ratios of the transistors are given in Table 1. The value of the miller compensation capacitor is set at 4pF and that of nulling resistor is 2.25 k $\Omega$ .

**Table 1.** Aspect ratios of the transistors.

Transistors	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )
<b>M1, M2, M1A, M2A</b>	20	1
<b>M3, M4, M12, M13</b>	5	1
<b>M5, M6</b>	60	1
<b>M7, M7A, M8, M9, M11</b>	40	1
<b>M10, M20</b>	88.80	1
<b>M14, M15, M16, M17</b>	40	1.75
<b>M18, M19</b>	45.15	1

A voltage sweep is applied at the voltage input Y terminal ranging from -0.4V to 0.4V. At first, only the single conventional P-channel differential pair is used. As can be deduced from the voltage transfer characteristics given in Figure 4 (a) the dynamic range of the pair is limited to negative supply and limited part of the positive supply. Now, a complete structure was simulated as it can be inferred from Figure 4(b); the structure exhibits almost rail to rail voltage swing of  $\pm 380\text{ mV}$ . The voltage tracking error is very small at 0.4 mV.

To check the accuracy of voltage transfer, a sinusoidal wave of 100 mV P-P at 100 KHz frequency is applied at the Y node and the corresponding X terminal waveform is observed as shown in Figure 5; there is no phase mismatch between input and output wave forms. The AC analysis reveals that the gain of voltage transfer between X and Y is unity, and its range is 7.8 MHz as shown in Figure 6.



**Figure 4.** Voltage Transfer characteristics of ULV-CCII(a) using conventional P-MOS pair;(b) using level shifted PMOS and conventional P-MOS pairs combined.

The current transfer between X and Z is shown in Figure 7. The linear range is  $\pm 40\mu\text{A}$ , which is acceptable at such a low voltage. The gain of the current transfer is unity, and its frequency range is 17MHz as shown in Figure 8. To further test the accuracy, a current sinusoidal signal of  $10\mu\text{A}$  P-P at 100 KHz frequency is applied at X node and the output at the Z node is noted. This testifies the precision of the current transfer as shown in Figure 9.

The parasitic impedance at node X at low frequency is calculated to be  $34\ \Omega$ , and its behavior at higher frequency is presented in Figure 10. It can be inferred that at higher frequencies the behavior changes to inductive. The Z node impedance at low frequency is  $0.105\ \text{M}\Omega$ , which is a bit less but well within an acceptable limit as given in Figure 11.

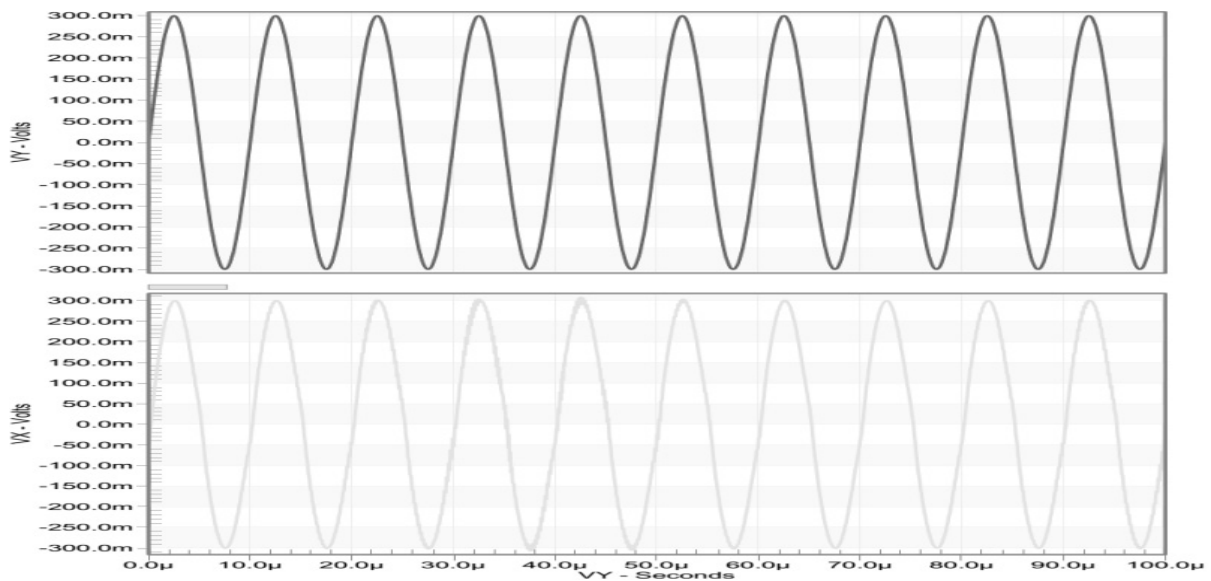


Figure 5. Transient analysis of ULV-CCII.

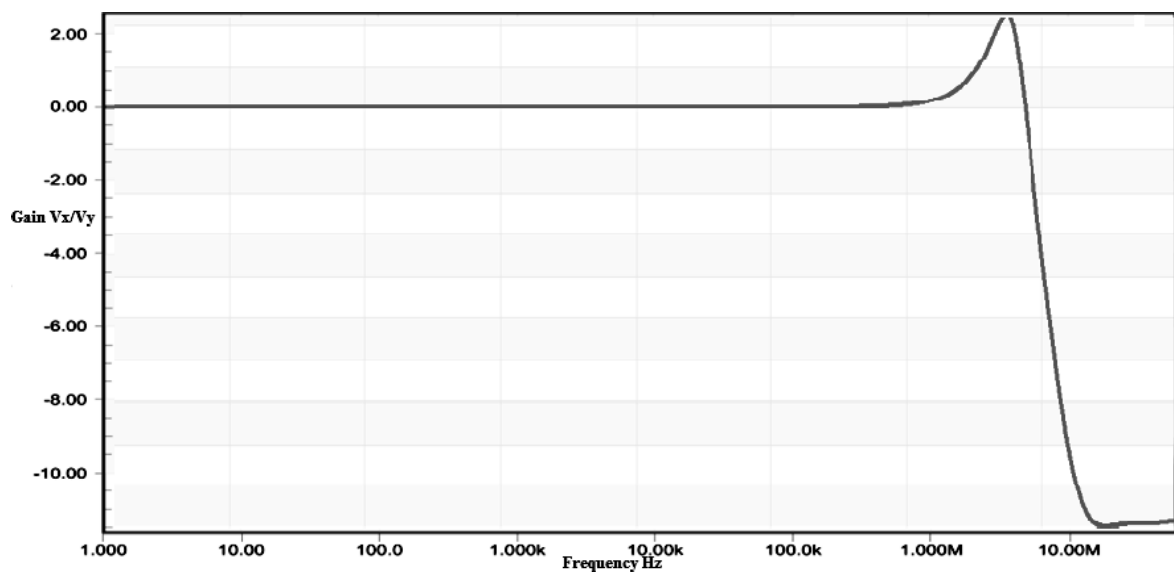


Figure 6. AC analysis of ULV-CCII.

The ULV-CCII is compared with the-state-of-the-art proposed LV CCII found in the literature. The complete comparison is given in Table 2. It can be said that the ULV-CCII exhibits good characteristics at such ultra-low voltage supply of  $\pm 0.4V$ . Furthermore, due to the use of conventional MOSFETs, the reduction in transconductance and the increase in input referred noise is avoided as observed in bulk driven and floating gate techniques. This ULV-CCII is suitable for medium frequency applications.



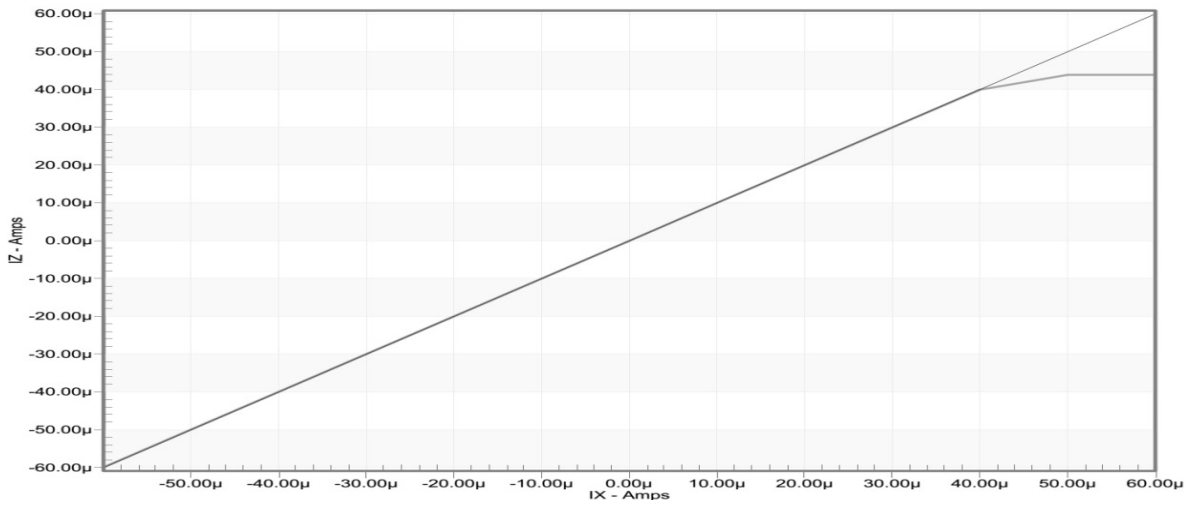


Figure 7. Current transfer characteristics of ULV-CCII.

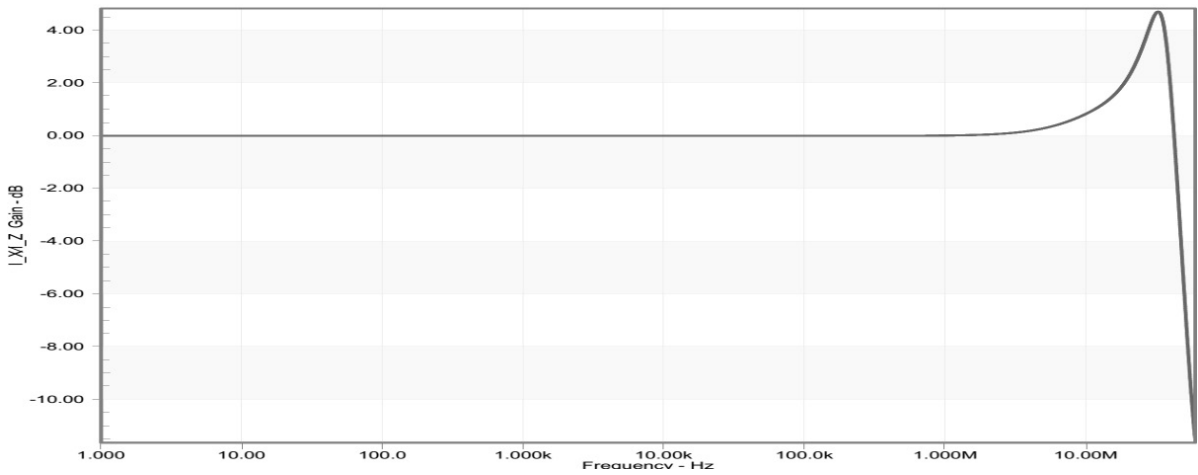


Figure 8. AC analysis of ULV-CCII.

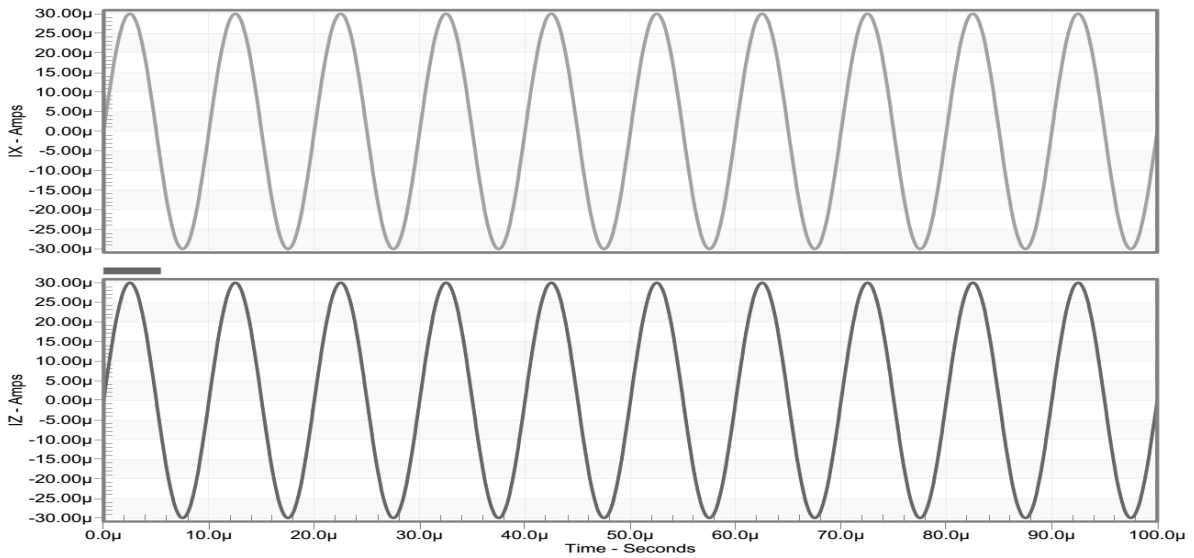


Figure 9. Transient analysis of ULV-CCII.

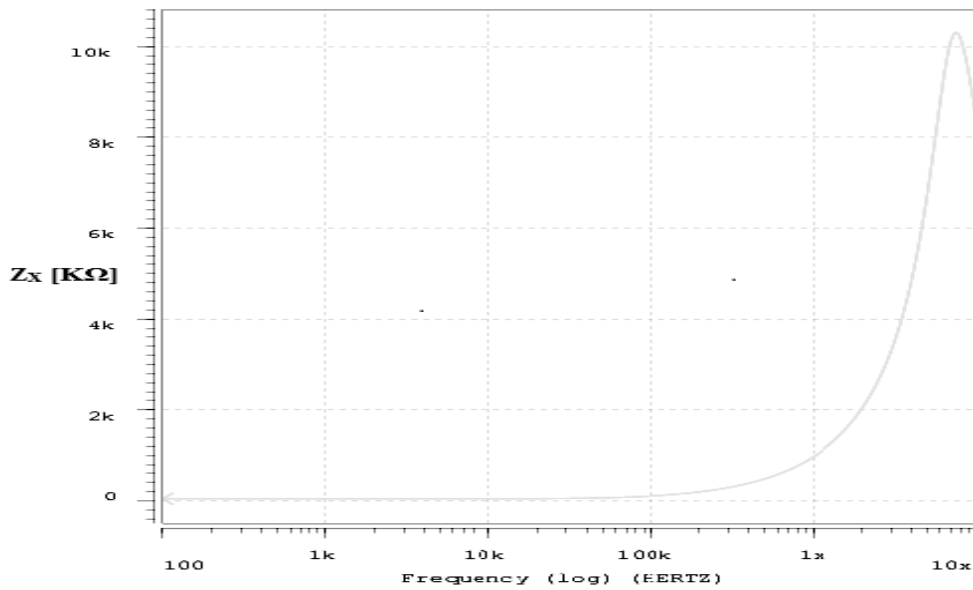


Figure10. X terminal impedance as a function of frequency.

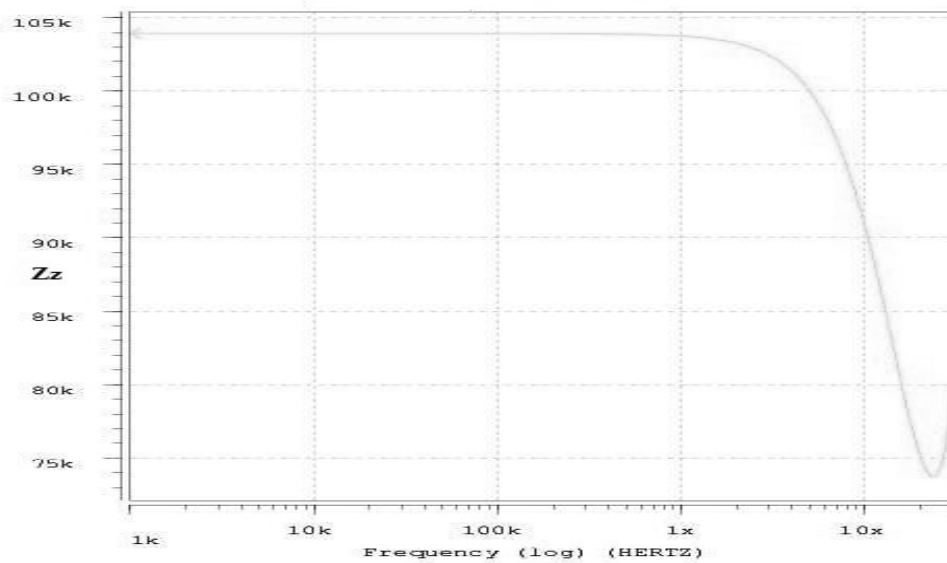


Figure 11. Z terminal impedance as a function of frequency.

### PROPOSED MULTIFUNCTION DUAL MODE FILTER

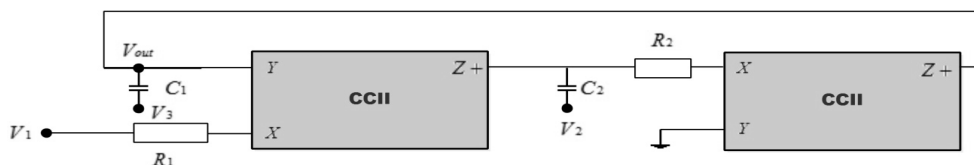
Filters are an integral part of every electronic system and so, their development remains an ever-evolving field. Active filters are extensively used in electronic systems, such as communication, signal processing, consumer electronics, instrumentation, control, and so on (Alzaher et al., 2013). The current conveyor has received considerable attention from the researchers for the filter design. This can be attributed to its excellent characteristics. The most versatile are universal filter structures as they can provide all standard functions without requiring any alteration in their topology (Alzaher et al., 2013; Horng, 2011; Soliman, 2008). To test the functionality of the proposed ULV-CCII, a Multi Input Single Output (MISO) multifunction universal filter is proposed. The designed filter is capable of working in both voltage and current modes without requiring any change in

its structure. The filter is capable of realizing Low Pass (LP), High Pass (HP), Band Pass (BP), All Pass (AP) and Notch (NP) responses in voltage mode, while, in the current mode, it provides LP and BP responses. The schematic of the voltage mode universal filter is shown in Figure 12. The filter utilizes only two current conveyors, two resistors, and two capacitors. The second order filter works by appropriately selecting the value of the three excitation inputs as given in Table 3 to realize LP, BP, HP, AP, and NP responses. The analysis of the filter structure yields the transfer function given in Equation 12.

**Table 2.** Comparison of CCII with the-state-of-the-art CCIIs available in the literature.

Parameters	(Khateb et al., 2011)	(Khateb et al., 2012)	(Stornelli & Ferri, 2013)	Proposed
	CCII	CCII+	*DDCCII	CCII+
Technology	0.18 μm	0.18 μm	0.18μm	0.18 μm
Technique Used	Bulk Driven MOSFET	Floating Gate MOSFET	Conventional MOSFET	Conventional MOSFET
Supply Voltage (V)	±0.4	±0.5	1	±0.4
Power Consumption (mW)	0.064	0.01	0.021	0.123
3 dB Bandwidth ( $I_z/I_x$ ), (MHz)	13	8.2	11	17
3 dB Bandwidth ( $V_x/V_y$ ), (MHz)	14	4.8	11	7.8
DC Voltage Range (mv)	380 to 380	-500 to 500	-700 to 700	-380 to 400
DC Current Range (μA)	-7 to 7	-30 to 30	-	-40 to 40
Current Gain ( $I_z/I_x$ )	1	1	0.98	1
Voltage Gain ( $V_x/V_y$ )	1	1	0.98	1
Node X Parasitic Impedance (Ω)	27	42	0.4	34
Node Z Parasitic Impedance (MΩ)	0.89	53	0.4	0.105

\*Differential Difference Current Conveyor(DDCCII).



**Figure 12.** Proposed filter structure.

$$V_{out} = \frac{N(s)}{D(s)} \tag{9}$$

$$N(s) = (S^2C_1C_2R_2R_1 + SC_1R_1)V_3 + V_1 - V_2SC_2R_1 \tag{10}$$

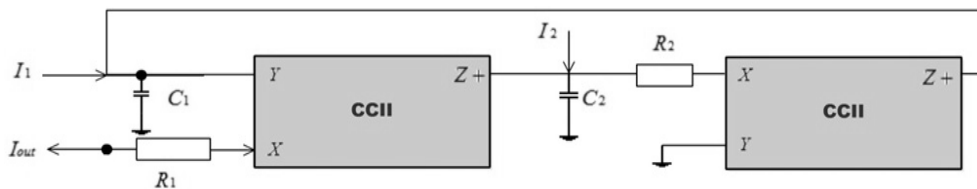
$$D(s) = S^2C_1C_2R_2R_1 + SC_1R_1 + 1 \tag{11}$$

$$V_{out} = \frac{(S^2C_1C_2R_2R_1 + SC_1R_1)V_3 + V_1 - V_2SC_2R_1}{S^2C_1C_2R_2R_1 + SC_1R_1 + 1} \tag{12}$$

**Table 3** Excitation sequence of the proposed filter

$V_{OUT}$	$V_1$	$V_2$	$V_3$
$V_{LP}$	1	0	0
$V_{HP}$	0	1	1
$V_{BP}$	0	1	0
$V_{NOTCH}$	1	1	1
$V_{AP}$	1	2	1

The current mode filter can be obtained from the same structure by grounding the two capacitors. The filter topology is presented in Figure13. Three input currents are injected appropriately according to the sequence stated in Table 4 to obtain LP and HP filter functions. The inspection of the filter gives the transfer function as presented in Equation 16. The quality factor and the pole frequency of the filter for both the modes are the same and given by Equations 17- 18, respectively.



**Figure13.** Proposed filter structure.

$$I_{out} = \frac{N(s)}{D(s)} \tag{13}$$

$$N(s) = I_1[1 + sC_2R_1] - I_2 \tag{14}$$

$$D(s) = S^2C_1C_2R_2R_1 + SC_1R_1 + 1 \tag{15}$$

$$I_{out} = \frac{I_1[1 + sC_2R_1] - I_2}{S^2C_1C_2R_2R_1 + SC_1R_1 + 1} \tag{16}$$

**Table 4.** Excitation sequence of the proposed filter.

$I_{OUT}$	$I_1$	$I_2$
$I_{LP}$	0	-1
$I_{BP}$	1	1

$$Q = \sqrt{\frac{C_2R_2}{C_1R_1}} \tag{17}$$

$$\omega = \sqrt{\frac{1}{C_1C_2R_2R_1}} \tag{18}$$

The ability of the proposed filter to work in voltage/current mode imparts flexibility and extends its application range. Furthermore, the resistors employed in the filter are connected to the X node of the CCII. This design incorporates the parasitic resistance as part of the main resistance.

**NONIDEALITIES OF CCII AND ITS EFFECT ON FILTER PERFORMANCE**

The exhaustive model depicting all the parasitic present at each node of the CCII+ is presented in Figure 14 (Fabre et al., 1995;Calvo et al., 2003). The corresponding non-ideal V-I characteristics of CCII is given by matrix Equation 22. The illustration shows the frequency variable voltage and current followers attached with their associated parasitic components. The inspection of the model reveals that X terminal exhibits resistive behavior at low frequencies and an inductive behavior at high frequencies. This is represented by a series combination of parasitic resistance and inductance. The Y node shows a resistive behavior at lower frequencies which changes to capacitive at higher frequencies. This is represented by a parallel combination of resistance and capacitance. The current output node Z has the same behavior as that of node Y. The parasitic capacitances and inductance associated with each node can be calculated using Equations 19-21.

$$L_x = \frac{R_x}{2\pi f_{X,+3dB}} \tag{19}$$

$$C_Y = \frac{1}{2\pi f_{Y,-3dB} R_Y} \tag{20}$$

$$C_Z = \frac{1}{2\pi f_{Z,-3dB} R_Z} \tag{21}$$

$$\begin{bmatrix} V_X \\ I_Z \\ I_Y \end{bmatrix} = \begin{bmatrix} \beta & Z_X & 0 \\ 0 & \alpha & 1/Z_Z \\ 1/Z_Y & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{22}$$

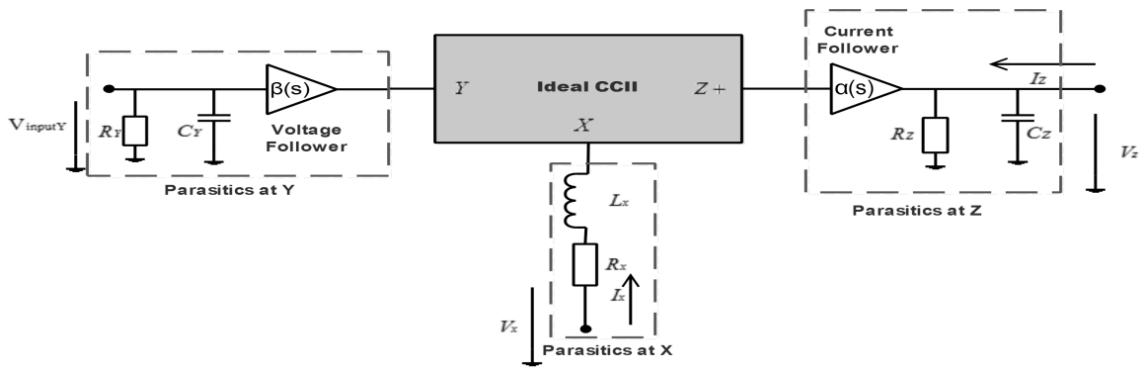


Figure 14. Non-ideal CCII model.

The current and voltage transfer of the low voltage CCII are specified by  $\alpha(s)$  and  $\beta(s)$ , respectively, as presented.

$$\beta(s) = \frac{\beta_o}{1 + s/\omega_\beta}$$

$$\alpha(s) = \frac{\alpha_o}{1 + s/\omega_\alpha}$$

where  $\alpha_o$  and  $\beta_o$  are the values of the voltage and current transfer at low frequencies. The poles associated with the current and voltage transfer are given by  $\omega_\alpha$  and  $\omega_\beta$ . Assuming the circuit is working at frequencies much below the corner frequencies of  $\alpha(s)$  and  $\beta(s)$ , we can approximate  $\alpha(s) = \alpha_o = 1 - \varepsilon_i$  and  $\beta(s) = \beta_o = 1 - \varepsilon_v$ .  $\varepsilon_i$  ( $|\varepsilon_i| \ll 1$ ) and  $\varepsilon_v$  ( $|\varepsilon_v| \ll 1$ ) denote the current and voltage tracking errors of the ULV-CCII. These non-idealities result in deviation from ideal response of the filter when realized using the CCII (Kaçar&Yeşil, 2012; Horng, 2012). To study the influence of the parasitic on the filter characteristics, we analyze the filter transfer function taking into account the current voltage transfer errors. The denominator of the non-ideal output voltage/current function, quality factor and resonant angular frequency of the filter are given in Equations 23-25.

$$D(s) = s^2 + \frac{s}{C_2 R_2} + \frac{\alpha_1 \beta_1 \beta_2}{C_1 C_2 R_1 R_2} \quad (23)$$

$$Q = \sqrt{\frac{\alpha_1 \beta_1 \beta_2 C_2 R_2}{C_1 R_1}} \quad (24)$$

$$\omega = \sqrt{\frac{\alpha_1 \beta_1 \beta_2}{C_1 C_2 R_2 R_1}} \quad (25)$$

As a result of component tolerance and non-idealities in CCII, the response of the practical filter deviates from the ideal one. To get a measure of the deviation, the concept of sensitivity is employed (Horng et al., 2012). The sensitivity is defined as

$$S_x^y = \frac{\partial y}{\partial x} \frac{x}{y} \sqrt{\frac{\alpha_1 \beta_1 \beta_2}{C_1 C_2 R_2 R_1}} \quad (26)$$

The active and passive sensitivities of  $\omega$  and  $Q$  of the proposed dual mode multifunction filter are:

$$S_{C_1}^\omega = S_{C_2}^\omega = S_{R_1}^\omega = S_{R_2}^\omega = -S_{\alpha_1}^\omega = -S_{\beta_2}^\omega = -S_{\beta_1}^\omega = -\frac{1}{2}$$

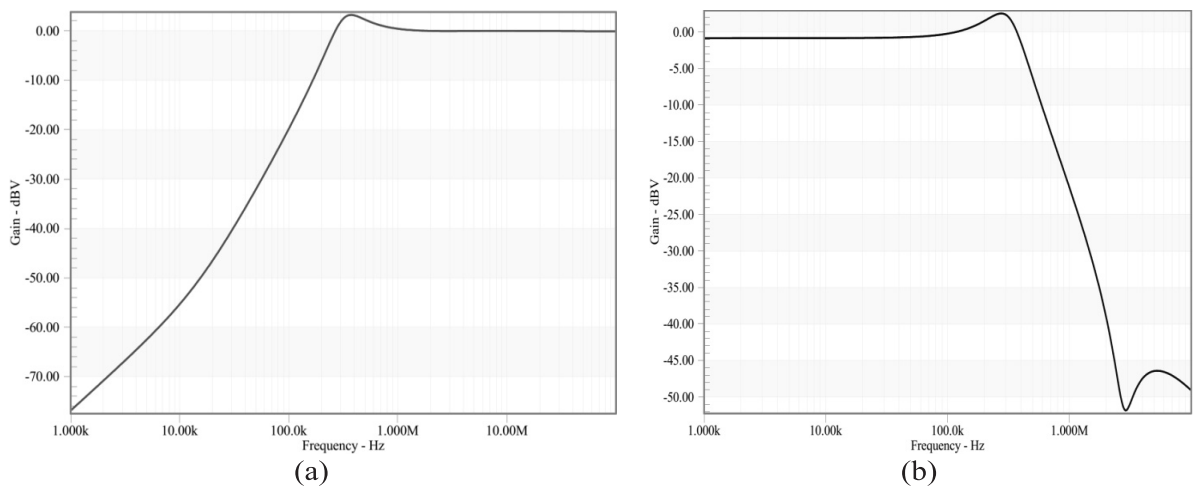
$$S_{C_1}^Q = S_{R_1}^Q = -\frac{1}{2}$$

$$S_{C_2}^Q = S_{R_2}^Q = S_{\alpha_1}^Q = S_{\beta_2}^Q = S_{\beta_1}^Q = \frac{1}{2}$$

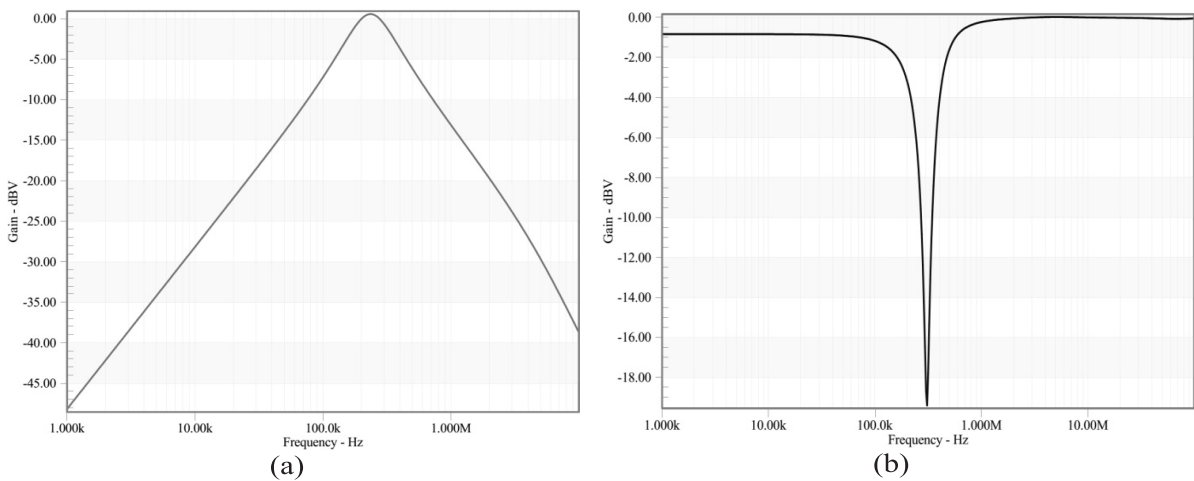
The inspection shows that all the active and passive sensitivities of the filter are low.

### SIMULATION RESULTS OF THE FILTER

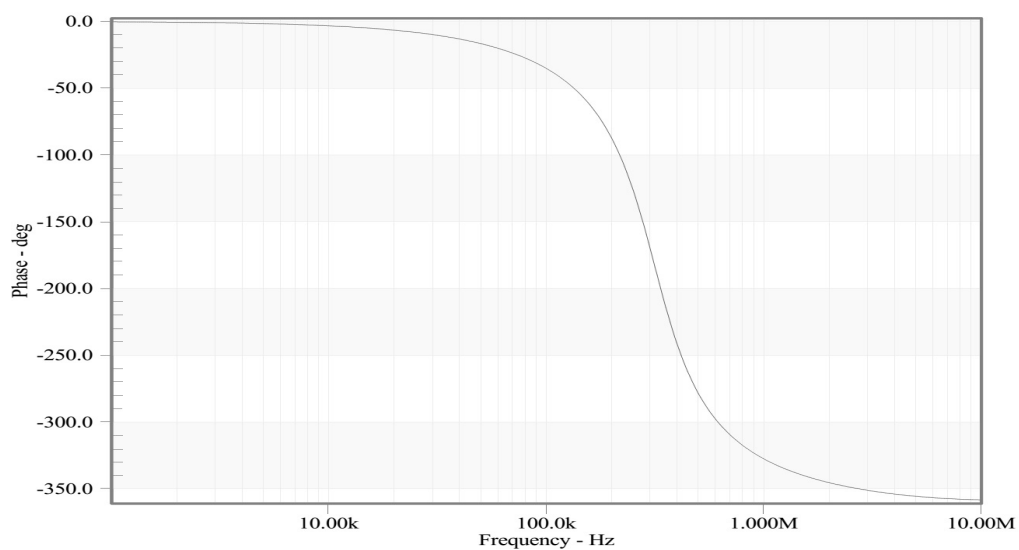
To demonstrate the workability of the proposed filter structure it is implemented in HSPICE using the newly developed ULV-CCII. The supply voltage is kept at  $\pm 0.4V$  and the bias current is set at  $30\mu A$ . The value of the passive components are fixed at  $C_1 = 100pF$ ,  $C_2 = 100pF$ ,  $R_1 = 5K$ ,  $R_2 = 5K$ . The Figures 15-16 give the simulation results of the LP,HP, BP and NP responses of the voltage mode filter. The phase response of the AP filter is given in Figure 17.



**Figure 15.** Simulated frequency response of the filter:(a)high pass;(b)low pass.



**Figure 16.** Simulated frequency response of the filter:(a)band pass;(b)notch pass.



**Figure 17.** Simulated phase response of all pass filters.



The same filter is configured as current mode and designed for  $Q=1$ . The values of the components are selected as  $C_1 = 250pF, C_2 = 250pF, R_1 = 5K, R_2 = 5K$ . The Figure 18 gives the simulation results for the current mode implementation. To establish the signal processing capability of the filter time domain analysis is performed on the filter configured as LP for both voltage mode and current mode of operation. The results are presented in Figures 19(a-b).

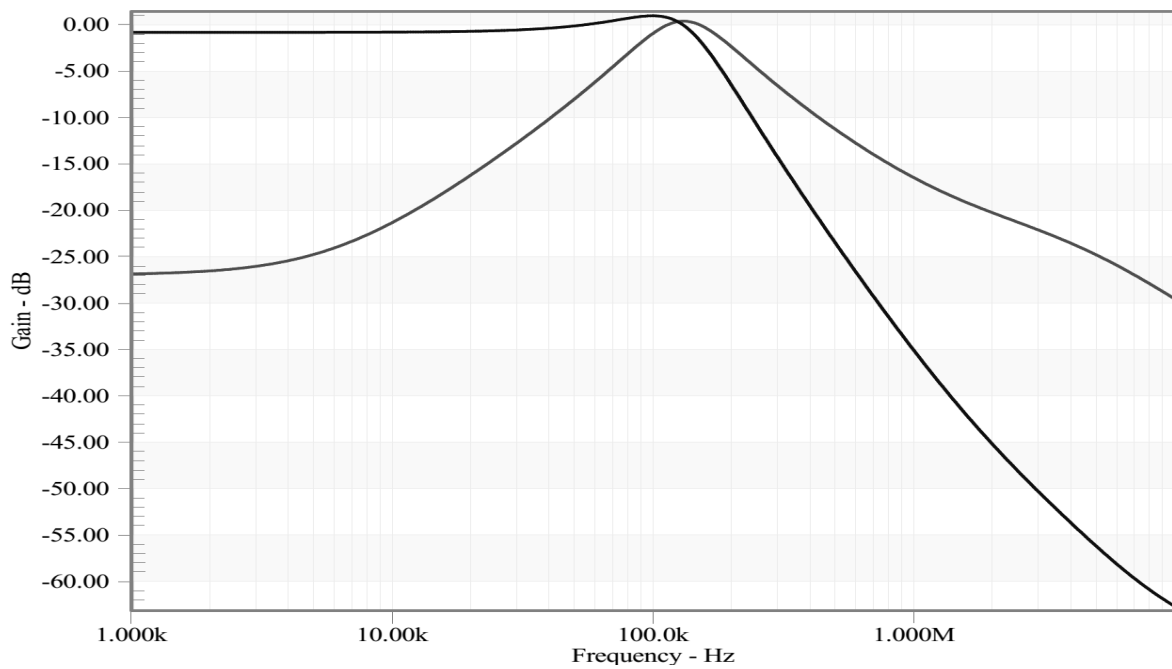


Figure 18. Simulated frequency response of the current mode filter.

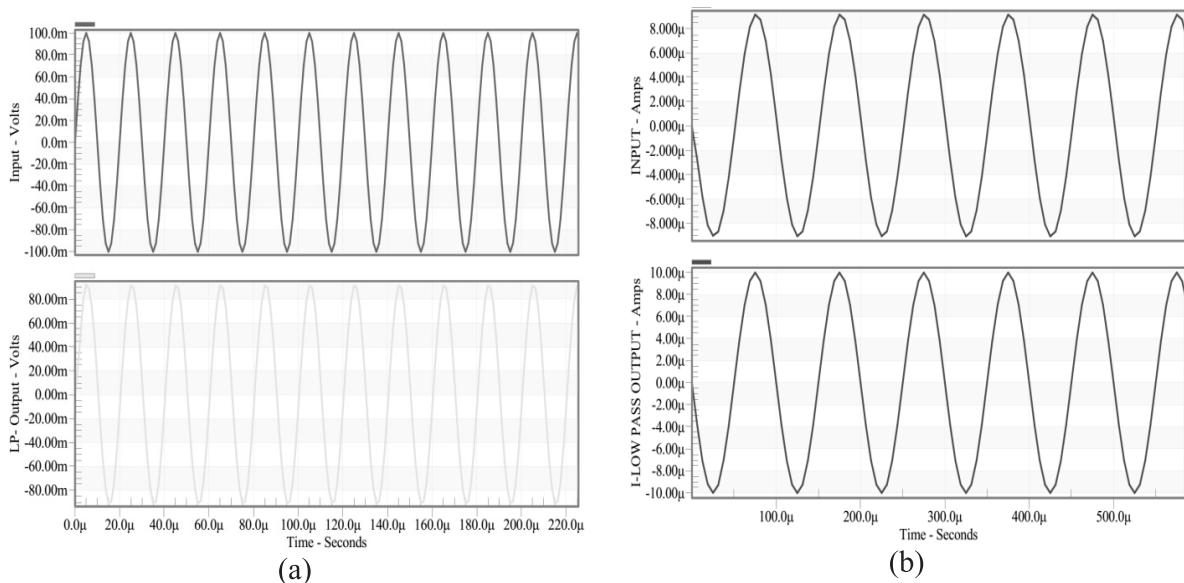


Figure19. Time domain analysis of the LP filter:(a)voltage mode;(b)current mode.

## CONCLUSIONS

An ULV-CCII design is discussed based on the level shifting technique. The simple implementation of the ULV-CCII employed a combination of conventional and level shifted PMOS differential pairs to attain rail to rail operation. The use of identical differential pairs overcame the offset introduced due to mobility difference between NMOS and PMOS transistors and enabled distortion less operation at an ultra-low supply of  $\pm 0.4V$ . The CCII is characterized by reasonable current and voltage transfer frequencies making it ideal for medium frequency applications. A dual current/voltage mode universal filter is also proposed providing HP, LP, BP, AP and NP responses in voltage mode and LP, BP responses in the current mode. The filter employed only two ULV-CCII and a minimum number of passive components. The effect of non-idealities on the response of the filter is also studied.

## ACKNOWLEDGMENTS

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## تصميم ناقل تيار من الجيل الثاني (CCII) بجهد منخفض جداً باستخدام تقنية تغيير المستوى و فلتر عالمي متعدد الوظائف ثنائي الأطوار

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### الخلاصة

يقدم هذا البحث تطبيقاً لناقل تيار منخفض الجهد من الجيل الثاني (ULV-CCII). المنهجية المعتمدة للتصميم عبارة عن استخدام تقنية تغيير المستوى لخفض جهد العتبة الفعلي لزوج من الترانزستورات التفاضلية PMOS. تم استخدام تركيبية مكونة من زوج PMOS تفاضلي تقليدي متغير المستوى ونظام كاسكود (cascade) مطوي منخفض الجهد لتشغيل السكة الحديد عند أقل مستوى من الإمدادات يعادل  $0.4V \pm$ . ويستفيد هذا النهج كذلك من نطاق النمط المشترك المتزايد. يقدم CCII عرض نطاق نقل الجهد يعادل 7.8 ميغاهرتز وعرض نطاق نقل التيار يعادل 17 ميغاهرتز بينما تبعد قدرة اسمية تبلغ 123 ميغاواط. لاحظنا أن فلتر شامل ذو نمط مزدوج متعدد الاستخدامات يؤكد صحة فعالية ULV-CCII. الفلتر قادر على العمل في نمط التيار والجهد دون تغيير في طوبولوجيا الخاصة به. يستخدم الفلتر اثنين فقط من ناقلات التيار من الجيل الثاني، واثنين من المكثفات واثنين من المقاومات. يؤدي استخدام CCII موجبة وأحادية المدخل إلى تبسيط عملية التنفيذ وتخفيف معوقات التوافق أثناء التصميم فقط مما يؤدي إلى تحسين أداء الفلتر. يعمل الفلتر عند التغذية بمقدار  $0.4 \pm$  فولت ويوفر جميع استجابات الفلاتر القياسية في نمط الجهد وكذلك استجابة تمرير الترددات المنخفضة وتمرير مجال الترددات بالنسبة للتشغيل في نمط التيار. يتم تقديم نتائج محاكاة H-Spice في تقنية TSMC CMOS بطول 0.18 ميكرومتر لإثبات النتائج.