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تحكم إلكتروني جديد لأسس سلسلة / موازية لوسي لمحاكاة لأدوات الحث المؤرض

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الخـلاصـة

الهدف من هذه الورقة البحثية هو اقتراح سلسلة جديدة / موازية لوسي لمكونات الحث مؤرض مع الحد الأدنى من متطلبات العناصر النشطة والسلبية. كل دائرة محاكاة تم تقديمها توظف أحد الجهد عبر موصل مكبر للصوت (VDTA) جنبا إلى جنب مع مكثف واحد متصلا بالأرض. جميع نظم المحاكاة المقدمة هي محض خالية من المعادلات الحرة مع مرفق ضبط الإلكترونية ولا تحتاج إلى أي شرط من مكونات مطابقة. في جميع التشكيلات المقترحة، تم تحقيق الاستخدام الكامل لمرحلة المدخلات من VDTA المستخدمة، باستثناء سلسلة واحدة LR. ويدرس أيضا أداء تكوينات المحاكاة المقدمة في ظل ظروف غير مثالية وكذلك مع المقاومة الطرفية من (VDTA). يتم تأكيد سلوك السلسلة المقترحة / موازية R-L لدوائر المقاومة من قبل تطبيق بعض الأمثلة. وقد تم التحقق من صحة التحليل النظري من خلال تشغيل محاكاة SPICE مع TSMC CMOS بمقدار 0.18 ميكرون لمتغيرات العملية.

Novel electronically controllable grounded series/parallel lossy inductor simulator configurations

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ABSTRACT

The objective of this research paper is to propose novel series/parallel lossy grounded inductor simulation configurationswith the minimum requirement of active and passive elements. Each presented simulator circuit employs one voltage differencing transconductance amplifier(VDTA) along with a single capacitor connected to ground. All the presented simulators are purely resistor-free realizations with electronic tuning facility and do not need any requirement of component matching. In all the proposed configurations, full utilization of the input stage of employed VDTAs has been achieved, except forone series LR circuit. The performance of the presentedsimulation configurations is also studied under non-ideal conditions as well as with the terminal parasitic impedances of VDTA. The behavior of the proposed series/parallel R-L impedance simulation circuits is confirmed by some application examples. The theoretical analysis has been validated by running SPICE simulations with TSMC CMOS 0.18 μm process parameters.

Keywords: Electronic tuning; grounded capacitor; lossy inductor simulator; no component matching; single capacitor.

INTRODUCTION

Inductor is a popular member of the passive element family, which find several applications in electrical engineering. A conventional inductor is a spiral inductor,which unfortunately exhibits many disadvantageous features such as huge size and large weight, generation ofundesired harmonics of original signal, radiation of electromagnetic signals,and linear dependence of quality factor on the dimensions that are restricted to the design of an inductor with high quality factor and small size. Hence, in the last two decades, the interest has been comprehensively directed towardsthe realization of active element based configurations, which can simulate the behavior of passive conventional inductors. Some grounded/floating inductance simulation circuits using different active components have been reported in Prescottet al.(1966); Senani et al.(1978); Senani et al.(1978); Arslan et al.(2003); Yuce et al.(2008); Prasad et al.(2010); Kacaret al.(2010); Prasad et al.(2012) and reference-cited therein.In addition to the simulation of pure inductances, the simulation of lossy inductors is also a popular research area recently.The lossy grounded inductor simulators have broad range of applications in active filters, sinusoidal oscillators, and series/parallel resonance circuits. Numerous grounded series/parallel R-L circuit simulation configurations employing different active components have been available inthe literature(Ford et al.,1966; Nandi et al.,1977; Nandi et al., 1978; Soliman et al., 1979; Nandi et al., 1979; Paulet al.,1981; Liu et al.,1994; Wang et al., 1998; Cam et al., 2004; Incekaraogluet al., 2005; Yuceet al., 2006; Yuceet al., 2006; Yuceet al., 2009; Kumar et al., 2010; Kacaret al., 2011; Metinet al., 2011; Kacaret al.,2014). Unluckily, all these proposed simulation circuits experience one or more of the

following disadvantages: (i) employment of more than one active element; (ii) requirement of more than one capacitors; (iii) use of passive elements in floating states, which is not suitable for monolithic integration; (iv) unavailability of electronic tuning; (v) lack of non-interactive tuning of equivalent inductance;and (vi) need for passive component matching. Therefore, the objective of this research paper is to report some new series/parallel R-L grounded impedance simulators with the following useful features: (i) minimum need of active and passive elements (one VDTA and onecapacitor); (ii) employmentof ground connected capacitor; (iii) no requirement of any external resistance; (iv) availability of electronic tuning facility; (v) availability of non-interactive tuning of realized inductance; (vi) no element matching constraints; and (vii) no deviation in behavior in non-ideal environment.

THE PROPOSED CONFIGURATIONS

VDTA is a versatile modern active building block (ABB) (Bioleket al., 2008), finding many applications in designing of active filters (Prasad et al., 2013; Prasad et al., 2013),sinusoidal oscillators (Prasad et al.,2013; Srivastava et al., 2014),and inductance simulation configuration (Prasad et al., 2012). The electrical symbolic representation of VDTA has been illustrated in Figure 1, where two voltage input terminals are VP and VN and threeoutput ports are Z, X+ and X- . All the ports of VDTA are high impedance ports. The implementation of VDTA using CMOS technology has been proposed by Yesil in 2011 (Yesilet al., 2011).

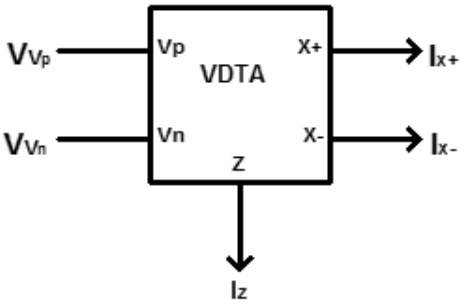


Figure 1. Electrical symbolic representation of VDTA.

The current-voltage relationships between different ports of VDTA can be described by the following hybrid matrix equation set.

$$\begin{bmatrix} I_Z \\ I_{X^+} \\ I_{X^-} \end{bmatrix} = \begin{bmatrix} g_{m_1} & -g_{m_1} & 0 \\ 0 & 0 & g_{m_2} \\ 0 & 0 & -g_{m_2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \quad (1)$$

The proposed grounded series/parallel R-L impedance simulators are shown in Figure 2.

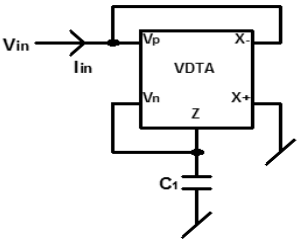


Fig.2 (a)

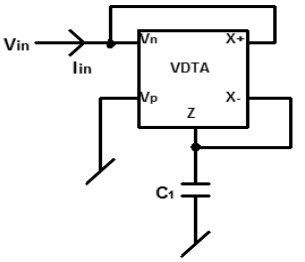


Fig. 2(b)

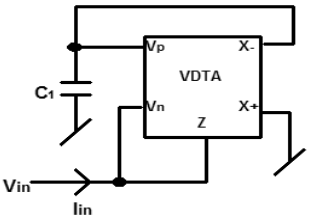


Fig. 2(c)

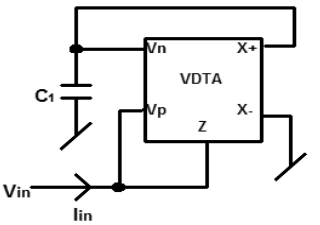


Fig. 2(d)

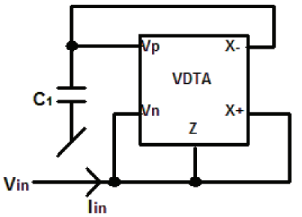


Fig. 2(e)

Figure 2. Proposed grounded series/parallel R-L simulators.

The input impedances, equivalent inductances, and equivalent resistances of the proposed circuit are given in Table 1, where "s" is a Laplace operator.

Table 1. Proposed series/parallel R-L configurations.

Figure No.	Input impedance (Z_{eq}= sL_{eq}+ R_{eq})	Equivalent inductance (L_{eq})	Equivalent resistance (R_{eq})	Type
Fig. 2(a)	$Z_{eq} = \frac{sC_1}{g_{m1}g_{m2}} + \frac{1}{g_{m2}}$	$\frac{sC_1}{g_{m1}g_{m2}}$	$\frac{1}{g_{m2}}$	+L series with +R
Fig. 2(b)	$Z_{eq} = \frac{sC_1}{g_{m1}g_{m2}} + \frac{1}{g_{m1}}$	$\frac{sC_1}{g_{m1}g_{m2}}$	$\frac{1}{g_{m1}}$	+L series with +R
Fig. 2(c)	$Z_{eq} = \frac{1}{\frac{g_{m1}g_{m2}}{sC_1} + g_{m1}}$	$\frac{sC_1}{g_{m1}g_{m2}}$	$\frac{1}{g_{m1}}$	+L parallel with +R
Fig. 2(d)	$Z_{eq} = \frac{1}{\frac{g_{m1}g_{m2}}{sC_1} - g_{m1}}$	$\frac{sC_1}{g_{m1}g_{m2}}$	$-\frac{1}{g_{m1}}$	+L parallel with -R
Fig. 2(e)	$Z_{eq} = \frac{1}{\frac{g_{m1}g_{m2}}{sC_1} + g_{m1} - g_{m2}}$	$\frac{sC_1}{g_{m1}g_{m2}}$	$\frac{1}{g_{m1} - g_{m2}}$	+L parallel with ±R

One can observe from Table 1 that the proposed circuits can simulate series realization of (+R) with (+L) and parallel realizations of (+R) with (+L), (-R) with (+L), and (±R) with (+L). From the expressions of L_{eq} and R_{eq} it is clear that, in all the configurations, both L_{eq} and R_{eq} are electronically tunable by g_{m1} and/or g_{m2}. The circuits of Fig. 2(a), 2(b), and 2(c) provide independent control of Leq by g_{m1} and circuit of Fig. 2(d) by g_{m2} without disturbing R_{eq}. In the configuration shown in Fig. 2 (e), R_{eq} can be positive or negative depending upon the values of g_{m1} and g_{m2}. Hence, this configuration can be used as a parallel (+R)-(+L) circuit by taking g_{m1} larger than g_{m2} or (-R)-(+L) circuit by setting up gm1 smaller than gm2. The values of g_{m1} and g_{m2} can be adjusted easily by changing the bias currents of VDTA. Hence, the nature of this configuration can be changed electronically.

NON-IDEAL ANALYSIS

In a non-ideal environment, the current-voltage relations between different terminals of VDTA can be defined using the below given current-voltage equations:

$$I_Z = \beta_Z g_{m_1}\left(V_P - V_N\right) \tag{2}$$

$$I_{X+} = \beta_{x+} g_{m_2} V_Z \tag{3}$$

$$I_{X-} = \beta_{x-} g_{m_2} V_Z \tag{4}$$

where β_Z, β_{X+} and β_{X-} are the errors in transconductance gains under non-ideal conditions.

To examine the performance of the presented simulators under non-ideal environment, these configurations are revisited with non-ideal current-voltage Equations (2)-(4). The input impedances, equivalent inductances, and equivalent resistances of proposed circuits under non- ideal conditions are given in Table 2.

Table 2. Proposed series/parallel R-L configurations under non-ideal conditions.

Figure No.	Input impedance (Z_{eq}= L_{eq}+ R_{eq})	Equivalent inductance (L_{eq})	Equivalent resistance (R_{eq})	Type
Fig. 2(a)	$Z_{eq} = \frac{sC_1}{g_{m1}g_{m2}\beta_Z\beta_{X+}} + \frac{1}{g_{m2}\beta_{X+}}$	$\frac{sC_1}{g_{m1}g_{m2}\beta_Z\beta_{X+}}$	$\frac{1}{g_{m2}\beta_{X+}}$	+L series with +R
Fig. 2(b)	$Z_{eq} = \frac{sC_1}{g_{m1}g_{m2}\beta_Z\beta_{X+}} + \frac{\beta_{X-}}{g_{m1}\beta_Z\beta_{X+}}$	$\frac{sC_1}{g_{m1}g_{m2}\beta_Z\beta_{X+}}$	$\frac{\beta_{X-}}{g_{m1}\beta_Z\beta_{X+}}$	+L series with +R
Fig. 2(c)	$Z_{eq} = \frac{1}{\frac{g_{m1}g_{m2}\beta_Z\beta_{X-}}{sC_1} + g_{m1}\beta_Z}$	$\frac{sC_1}{g_{m1}g_{m2}\beta_Z\beta_{X-}}$	$\frac{1}{g_{m1}\beta_Z}$	+L parallel with +R
Fig. 2(d)	$Z_{eq} = \frac{1}{\frac{g_{m1}g_{m2}\beta_Z\beta_{X+}}{sC_1} - g_{m1}\beta_Z}$	$\frac{sC_1}{g_{m1}g_{m2}\beta_Z\beta_{X+}}$	$-\frac{1}{g_{m1}\beta_Z}$	+L parallel with -R
Fig. 2(e)	$Z_{eq} = \frac{1}{\frac{g_{m1}g_{m2}\beta_Z\beta_{X-}}{sC_1} + g_{m1}\beta_Z - g_{m2}\beta_{X+}}$	$\frac{sC_1}{g_{m1}g_{m2}\beta_Z\beta_{X-}}$	$\frac{1}{g_{m1}\beta_Z - g_{m2}\beta_{X+}}$	+L parallel with ±R

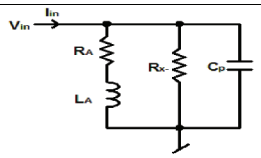
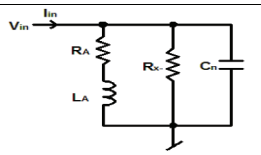
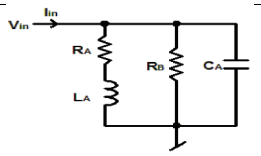
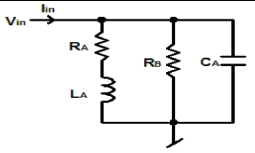
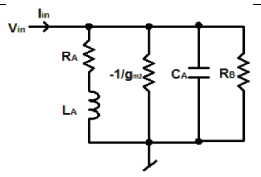
On comparing the expression of Table 1 with Table 2, it can be illustrated that the behavior of the proposed simulators under non-ideal conditions remains the same as the ideal behavior. The values of Req and Leq are deviated from ideal values, but as the values of βx+, βx- and βz are very near to unity, deviations in Req and Leq are very minor. Hence, under non-ideal conditions, the performance of the proposed simulators matches closely with the ideal performance.

EFFECTS OF PARASITICS

In this section, the behavior of the proposed series/parallel grounded R-L impedance simulators is evaluated inthe presence of parasitic impedances of VDTA terminals. In VDTA realization, using CMOS (Yesilet al., 2011), finite grounded parasitic resistances come into viewat P, N, and Z ports, while finite grounded parasitic capacitances appear at X+, X-, and Z ports.

Theequivalent circuits of the presented grounded series/parallel R-L circuit simulators considering the terminal parasitic impedances of VDTA have been given in Table 3.

Table 3. Equivalent circuits ofthe proposed configurationsunder the influence of VDTA parasitics.

Figure No.	Equivalent circuit under the influence of parasitics	Component values
Fig. 2(a)		$R_A = \frac{\left(\frac{1}{R_Z} + g_{m2}\right)}{(g_{m1}g_{m2})}, L_A = \frac{(C_1 + C_z + C_n)}{(g_{m1}g_{m2})}$
Fig. 2(b)		$R_A = \frac{\left(\frac{1}{R_{x-}} + \frac{1}{R_Z} + g_{m2}\right)}{(g_{m1}g_{m2})}, L_A = \frac{(C_1 + C_z)}{(g_{m1}g_{m2})}$
Fig. 2(c)		$R_A = \frac{\left(\frac{1}{R_{x-}}\right)}{(g_{m1}g_{m2})}, L_A = \frac{(C_1 + C_p)}{(g_{m1}g_{m2})}, R_B = \frac{1}{\left(\frac{1}{R_z} + g_{m1}\right)}, C_A = C_z + C$
Fig. 2(d)		$R_A = \frac{\left(\frac{1}{R_{x+}}\right)}{(g_{m1}g_{m2})}, L_A = \frac{(C_1 + C_n)}{(g_{m1}g_{m2})}, R_B = \frac{1}{\left(\frac{1}{R_z} + g_{m1}\right)}, C_A = C_z + C_p$
Fig. 2(e)		$R_A = \frac{\left(\frac{1}{R_{x-}}\right)}{(g_{m1}g_{m2})}, L_A = \frac{(C_1 + C_p)}{(g_{m1}g_{m2})}, R_B = \frac{1}{\left(\frac{1}{R_{x+}} + \frac{1}{R_z} + g_{m1}\right)}, C_A = C_z + C_n$

APPLICATION EXAMPLES

The configurations shown in Fig. 2(a), 2(c), and 2(d) are chosen as examples to confirm the working potential of the proposed series/parallel R-L impedance simulators by constructing some application circuits using these configurations.To demonstrate the performance of series (+R)-(+L) circuit simulator presented in Fig.2(a), we use it in the structure of the second order current mode low-pass filter (LPF) shown in Fig.3(a).

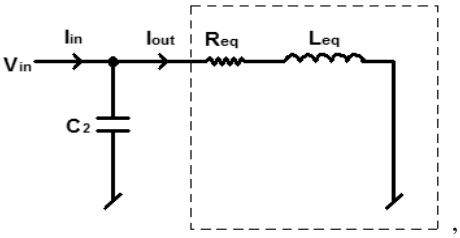


Fig. 3(a)

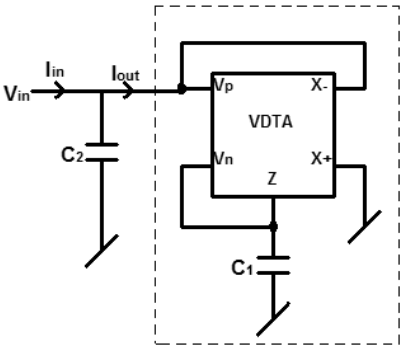


Fig. 3(b)

Figure 3. Second order current mode low-pass filter: (a) passive realization; (b) active realization using series (+R)-(+L) simulator proposed in Fig. 2(a).

The current transfer function of LPF shown in Figure 3(b) is given by

$$\frac{I_{out}}{I_{in}} = \frac{g_{m1}g_{m2}}{s^2C_1C_2 + sC_2g_{m1} + g_{m1}g_{m2}} \tag{5}$$

To examine the working of parallel (+R)-(+L) circuit simulator proposed in Fig. 2(c), a second order voltage mode high pass filter (HPF) has been designed as shown in Fig. 4(b).

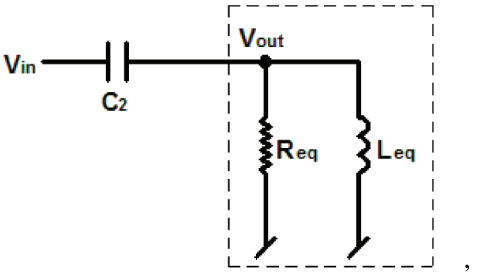


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Fig. 4(a)

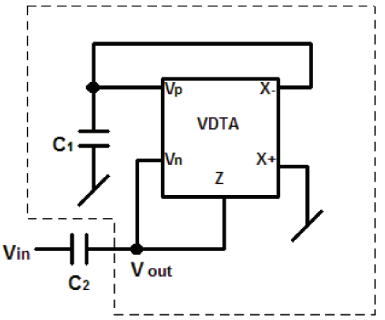

Fig. 4(b)

Figure 4. Second order voltage mode high-pass filter; (a) realization using passive R-L-C: (b) active realization using parallel (+)R-(+L) simulator proposed in Fig. 2(c).

The frequency response of this HPF is shown in Figure 9. By routine analysis, the voltage transfer function of the realized HPF is given by

$$\frac{V_{out}}{V_{in}} = \frac{s^2 C_1 C_2}{s^2 C_1 C_2 + s C_1 g_{m1} + g_{m1} g_{m2}} \tag{6}$$

To illustrate the application of parallel (-R)-(+L) simulator shown in Fig. 2(d), it is used in construction of a second order oscillator as shown in Figure 5.

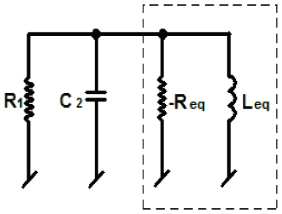

Fig. 5(a)

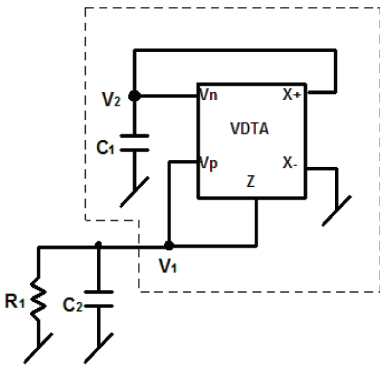

Fig. 5(b)

Figure 5. Second order oscillator; (a) passive realization: (b) active realization using parallel (-R)-(+L) simulator proposed in Fig. 2(d).

The condition of oscillation (CO) and frequency of oscillation (FO) of the oscillator given in Fig. 5(b) are

$$\frac{1}{R_1} - g_{m1} \le 0 \tag{7}$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{8}$$

SIMULATION RESULTS

To validate the theoretical analysis, SPICE simulations were performed employing CMOS VDTA (Yesilet al., 2011).The DC supply voltages were chosenas±0.9 VDC with all the biasing currents of VDTA being equal to150 μA. Series R-L simulator inFig.2(a) is simulated with C1=0.01nF, 0.05nF, and 0.1nF. The magnitude and phase responses of input impedance of the circuit, shown in Fig. 2(a), have been shown in Figures 6 and 7, respectively. From the input impedance expression of Fig. 2(a) given in table1, it can be seen that, for a high value of C_1, the value of L_{eq} is high in comparison to lossy part R_{eq} and the behavior of this series lossy inductor becomes inclined more towards a lossless inductor. For further high values of C_1, the value of R_{eq} will be very small in comparison to L_{eq} and the configuration will work like a pure lossless inductor. This effect can be illustrated by magnitude response plots shown in Figure 6 The initial "horizontal part" of frequency response is due to the existence of lossy term "R_{eq}". As the value of

C_1 increases, the value of L_{eq} becomes high, and the flat part of response becomes comparatively narrower than remaining inclined,which clearly indicates that, on increasing "C_1", the behavior of the proposed circuit starts inclining towards the behavior of lossless inductor. Parallel R-L simulator of Fig. 2(c) is also simulated with C_1=0.01nF, 0.05Nf, and 0.1nF. The magnitude and phase responses of the input impedance of this circuit have been shown in Figures 8 and 9. Figure8 shows that the input impedance magnitude is low for small values of "C_1" and the curve is more flat, which can be verified by the mathematical expression given in Table 1.

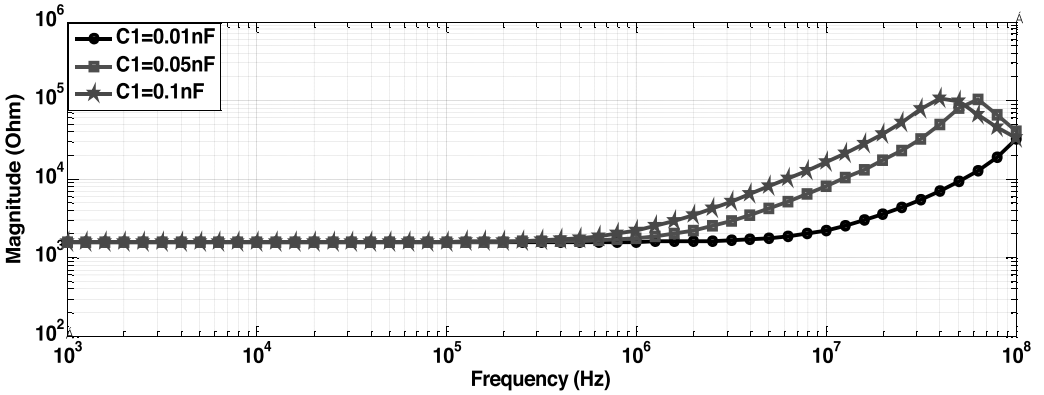

Figure 6. Magnitude response of series (+R)-(+L) simulator proposed in Fig. 2(a).

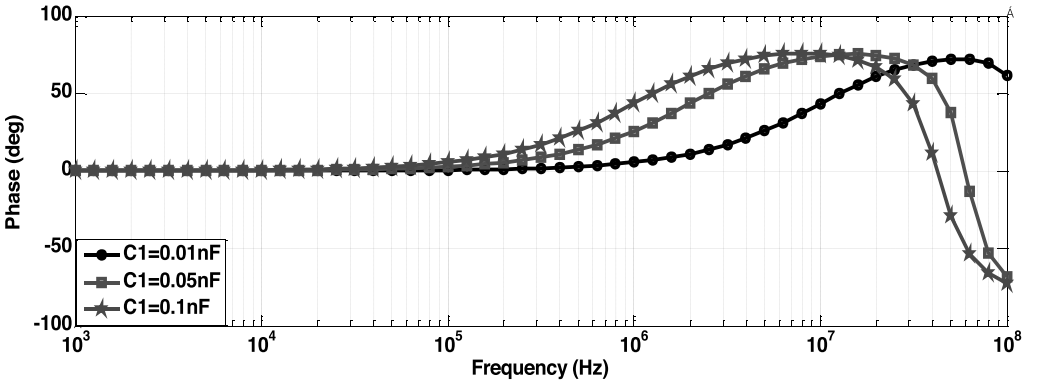

Figure 7. Phase response of series (+R)-(+L) simulator proposed in Fig.2(a).

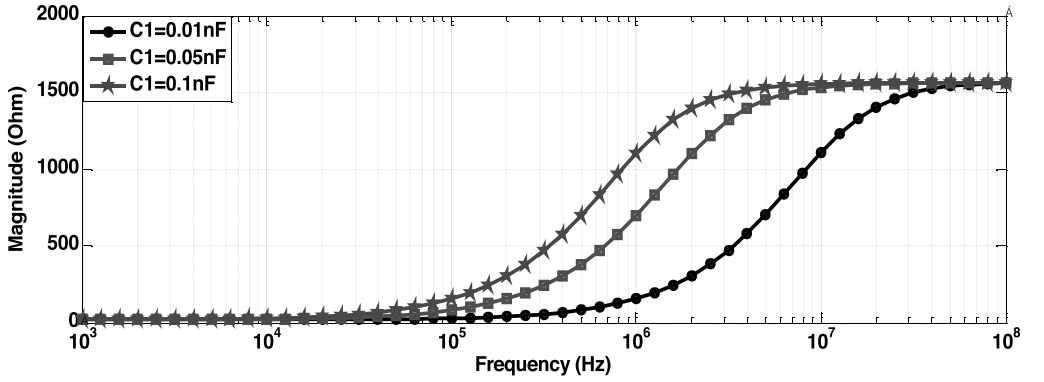

Figure 8. Magnitude response of parallel (+R)-(+L) simulator proposed in Fig. 2(c).

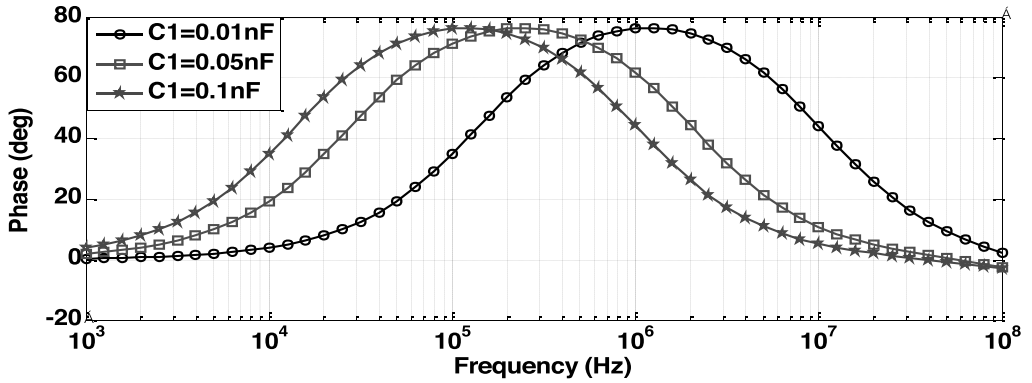

Figure 9. Phase response of parallel (+R)-(+L) simulator proposed in Fig. 2(c).

To show the electronic controllability facility in series R-L simulator shown in Fig.2(a), the simulation has been performed for a different set of bias current values with C_1=0.01nF. The simulation plots are shown in Figure10, which clearly illustrate that, on increasing the bias currents, the values of g_{m1} and g_{m2} are increasing and the input impedance is decreasing. Electronic tunability of parallel R-L simulator shown in Fig. 2(c) has been demonstrated in the plots shown in Figure11 selecting C_1=0.01nF.

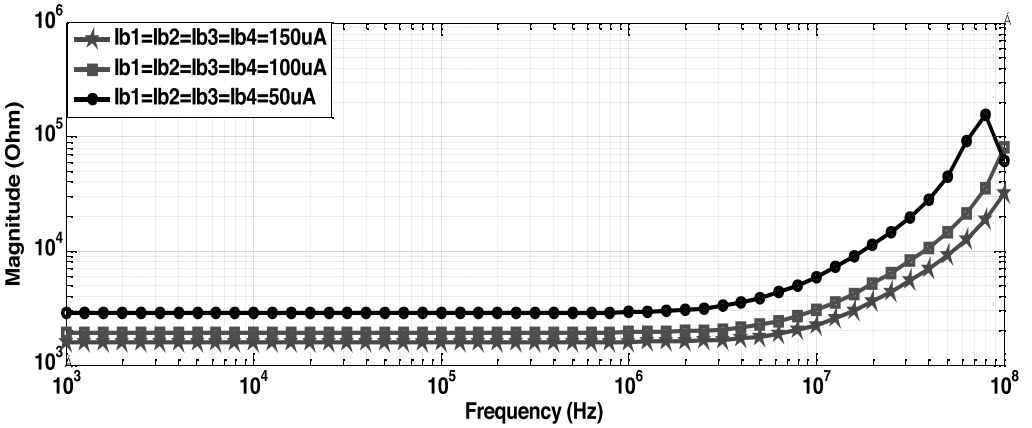

Figure 10. Response of series (+R)-(+L) simulator shown in Fig. 2(a) for different bias currents.

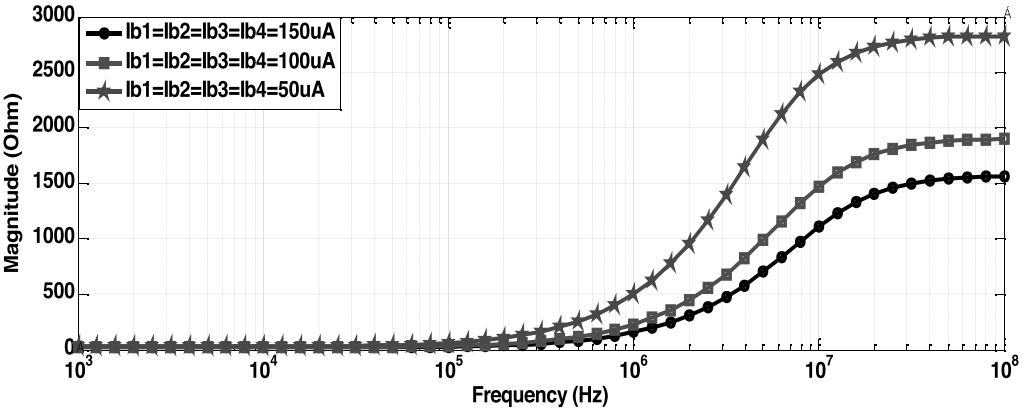

Figure 11. Response of series (+R)-(+L) simulator proposed in Fig. 2(c) for different bias currents.

The realized LPF shown in Fig. 3(b) is simulated with passive component values selected as C_1=0.01nF and C_2=0.02nF. The simulated filter response is shown in Figure 12.

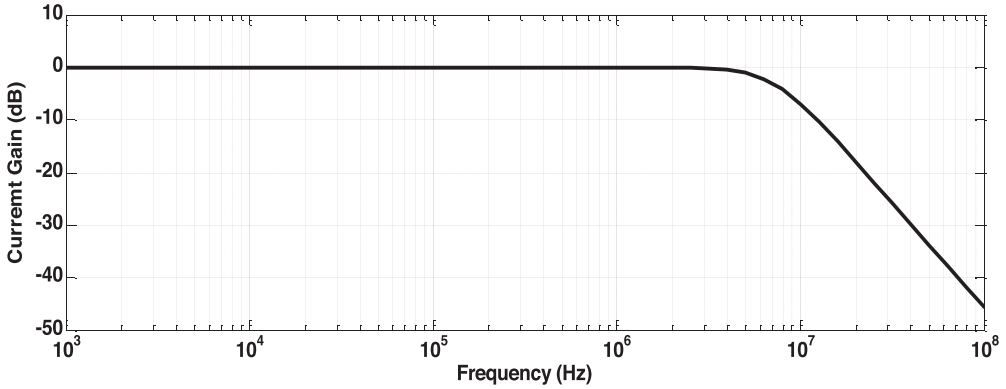

Figure 12. Frequency response of second order current mode low-pass filter shown in Fig. 3(b).

For simulation of high-pass filter shown in Fig. 4(b), the following component values are chosen: C_1=0.02nF and C_2=0.01nF. The frequency response of this high pass filter has been shown in Figure 13.

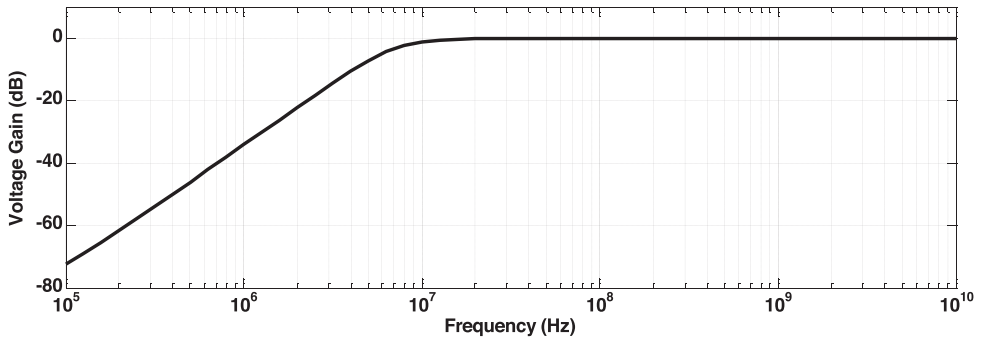

Figure 13. Frequency response of second order voltage mode high-pass filter shown in Fig. 4(b).

The passive elements' values used for the simulation of the oscillator shown in Fig. 5(b) are as follows: C_1=C_2= 0.1nF and R_1= 1.7 kΩ. Fig. 14(a), 14(b), and 14(c) show the transient and steady state responses of voltage outputs V_1 and V_2. The phase difference between V_1 and V_2 is found to be 89.67^0, which confirms the quadrature phase relationship between V_1 and V_2. Fig. 14(d) shows the frequency spectrum of voltage V_1 where FO is found to be 1005.6 KHz, while the ideal value of FO is 1010 KHz. So, the simulated value is inclose agreement with the ideal value.

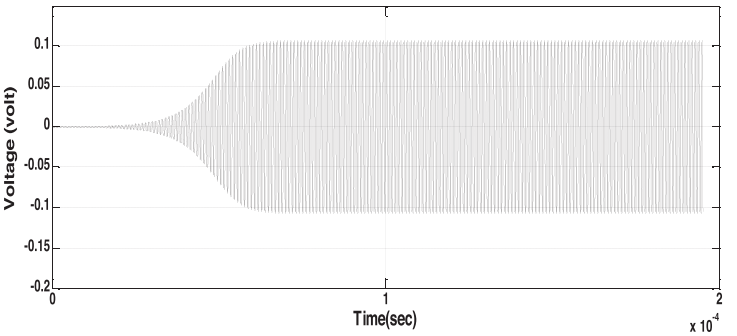

Fig. 14(a)

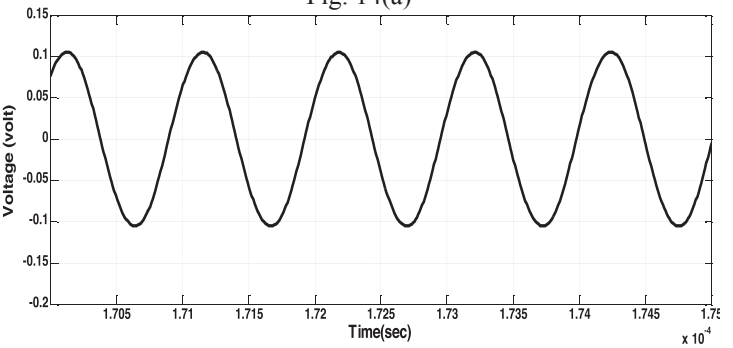

Fig. 14(b)

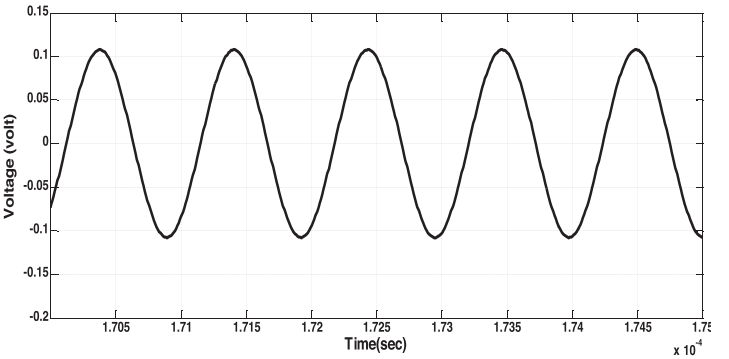

Fig. 14(c)

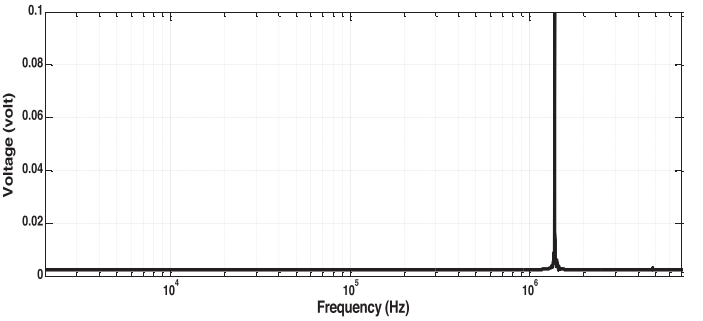

Fig. 14(d)

Figure 14. Responses of oscillator shown in Fig. 5(b):(a) transient response of V1 and V2;(b) steady state response of V1; (c) steady state response of V2; (d) frequency spectrum.

The comparison of the proposed grounded series/parallel R-L simulators with the previously proposed same type of circuits is given in Tables 4 and 5.

Table 4. Comparison with previously proposed grounded series R-L circuit simulators.

Ref.	Fig. No.	Number of active element	Number of resistor	Number of capacitor	Electronic control of "Leq"and "Req"	Non-Interactive control of "Leq"	Need of element matching
Nandiet al., 1977	Fig.2(a)	1	1(F)+ 1(G)	1(F)	No	No	No
Nandi et al., 1978	Fig. 1	1	1(F)+ 1(G)	1(F)	No	No	No
	Fig. 2	2	1(F)+ 1(G)	1(F)	No	Yes	No
	Fig. 2	2	2(F)+ 1(G)	1(G)	No	Yes	No
	Fig. 2	2	1(F)+ 1(G)	1(F)	No	Yes	No
Nandi et al., 1979	Fig.1(a), Fig.1(b)	2	2(F)+ 2(G)	1(G)	No	Yes	Yes
Paul et al., 1981	Fig. 1	1	2(F)+ 2(G)	1(F)	No	Yes	Yes
Liuet al., 1994	Fig. 1	1	1(F)+ 1(G)	2(G)	No	Yes	Yes
Wang et al., 1998	Fig.2(b)	1	1(F)+ 1(G)	1(F)	No	No	No
Incekaraogluet al., 2005	Fig.2(a)	1	1(F)+ 1(G)	1(G)	No	No	No
	Fig.2(b)	1	2(F)+ 1(G)	1(F)	No	No	No
Yuce et al., 2009	Fig.2 – Fig.5	1	1(F)+ 1(G)	1(F)	No	Yes	No
Kacaret al., 2011	Fig.2(b)	1	1(F)+ 1(G)	1(F)	No	No	No
Metinet al., 2011	Fig.2(b)	1	2(F)	1(F)	No	Yes	No
	Fig. 2(f)	1	2(F)+ 1(G)	1(F)	No	No	No
Kacaret al., 2014	Fig.2(c) – Fig.2(f)	1	1(G)	1(G)	No	Yes	No
Proposed	Fig.2(a), Fig.2(b)	1	0	1-(G)	Yes	Yes	No

G* Grounded. F* Floating

Table 5.Comparison with previously proposed grounded parallel R-L circuit simulators.

Ref.	Fig. No.	Number of active element	Number of resistor	Number of capacitor	Electronic control of both "Leq"and "Req"	Non-Interactive control of "Leq"	Need of element matching
Ford et al., 1966	Fig.1(a)	1	2(F)	1(F)	No	No	No
Solimanet al., 1979	Fig.2(a)	1	1(F)	1(G)	No	Yes	No
Pauletal., 1981	Fig.1	1	2(F)+2(G)	1(F)	No	Yes	Yes
Wang et al., 1998	Fig.2(a)	1	1(F)+1(G)	1(F)	No	Yes	No
Cam et al., 2004	Fig.2(a), Fig.2(b)	2	4(F)	1(F)	No	Yes	No
Incekaraogluet al., 2005	Fig.3(a), Fig.3(b)	1	1(F)+1(G)	1(G)	No	No	No
Yuceet al., 2006	Fig.3(a), Fig.3(b)	1	1(F)+1(G)	1(F)	No	No	No
Yuceet al., 2006	Fig.2	1	1(F)+1(G)	1(G)	No	No	No
Kumar et al., 2010	Fig.1	1	2(F)+2(G)	1(F)	No	No	No
Kacaret al.,2011	Fig.2(c)	1	1(F)+1(G)	1(F)	No	Yes	No
Metinet al., 2011	Fig.2(c)	1	2(F)+1(G)	1(F)	No	No	Yes
	Fig.2(d)	1	3(G)	1(F)	No	No	No
	Fig.2(e)	1	2(F)+1(G)	1(F)	No	Yes	No
Proposed	Fig.(2c), Fig.2(d)	1	0	1(G)	Yes	Yes	No
	Fig.2(e)	1	0	1(G)	Yes	No	No

G* Grounded. F* Floating

CONCLUSION

This paper proposes some new grounded series/parallel lossy inductor simulators using VDTA. All the presented configurations are very compact with a minimum requirement of active and passive elements (single VDTA and one capacitor). The proposed configurations have several profitable points such asthe use of grounded capacitor, facility of electronic tuning, non-interactive tuning of equivalent inductance, and no need of any element value matching. To check the workability of the presented circuits, some application examples are given. SPICE simulations are included to confirm the theoretical analysis.

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