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# أمثلة التيار الذاتي الدفع لتيار مضاعف الطوري المتحول تحويل الجسري DC-DC مع مغناطيس متكامل

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## الخلاصـة

في هذه الورقة، تصميم الذاتي الدفع لتيار مضاعف (CD) الطوري المتحول تحويل الجسري (PSFB) مع مغناطيس متكامل (IM) تم اقتراحها. في مراحل التصميم، متعرج الأول للمحول ينقسم الى متعرجين والمحاثتين وتكامل يتم في قلب محول القوى. وبالإضافة إلى ذلك، فإنه قد تم استخدام التشغيل الذاتي لتحكم موازي وبتزامن مع الجانب الثانوي. تتولد إشارات ذاتية باستخدام الموجة الثانوية في محول الكهرباء. وبالتالي فإن كثافة الطاقة للمحول تزداد مع استخدام قلب مغناطيسي واحد فقط. وتحليل فقدان التحليلي تم عرضها لتقييم عناصرالتصميم الأمثل. عملية تصميم المقترح تم انجازها لعينة تعمل على 80kHz ومعدل (1KW 12V-83A). أخيرا، يتم مقارنة كفاءة النتائج التي تم الحصول عليها مع محول (DRCT) و 10% زيادة الكفاءة تم الحصول عليها مع طريقة التصميم المقترح.

# Optimization of a self-driven current-doubler phase shifted full bridge DC-DC converter with integrated magnetic

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## ABSTRACT

In this paper, a design approach of a self driven current doubler (CD) phase shifted full bridge converter (PSFB) with integrated magnetic (IM) is proposed. In the design procedure, primary winding of transformer split into two windings and output inductors are integrated in the power transformer's core. In addition, self-driver is used to drive parallel connected synchronous rectifier on the secondary side. Self-driving signals are generated using directly secondary in power transformer. Therefore, power density of the converter is increased using only one magnetic core. An analytical loss analysis is presented to evaluate optimum design parameters. Operation of proposed design is achieved by a prototype operating at 80kHz and rated 1kW (12V-83A). Finally, the obtained efficiency results are compared to the performance of diode rectified center tapped (DRCT) conventional PSFB converter and 10% increasing efficiency is achieved with proposed design approach.

**Keywords:** Current doubled rectifier; design optimization; integrated magnetic; phase shifted full bridge converter; self-driver.

## INTRODUCTION

Recently, research in the area of power converters area has focused on high power density, due to the advantage of cost reduction, limited space and weight requirements in some application areas like telecom/data center, electric vehicle/aircraft (Kolar et al., 2008). Besides, in data center application, increasing energy consumption due to more energy demand and rising energy price require high efficiency power conversion. Therefore, high efficiency and high power density power conversion is getting more important key parameter in converter design in order to save energy and reduce cooling size.

PSFB converter is used widely for data center or telecom applications due to its high conversion efficiency, high power density, simple control structure and low electromagnetic interface (EMI) (Zhao et al., 2009; Badstuebner et al., 2011; Badstuebner et al., 2010; Kim et al., 2014; Gu et al., 2013; Zhao et al., 2008; Biela

et al., 2009 & Xu et al., 2005). In the low output voltage and high output current applications, center tapped rectifier or current doubled rectifier structures given in Fig. 1 is preferred (Badstuebner et al., 2011 & Badstuebner et al., 2010). The main advantage of current doubler rectifier is reduced conduction loss of secondary winding compared to center tapped rectifier especially in the high output current and low output voltage applications. However, usage of three magnetic components increases the size and cost of the overall system. To solve this problem, integrated magnetic structures are proposed (Xu et al., 2000; Chen et al. 1997 & Jin et al., 2014).

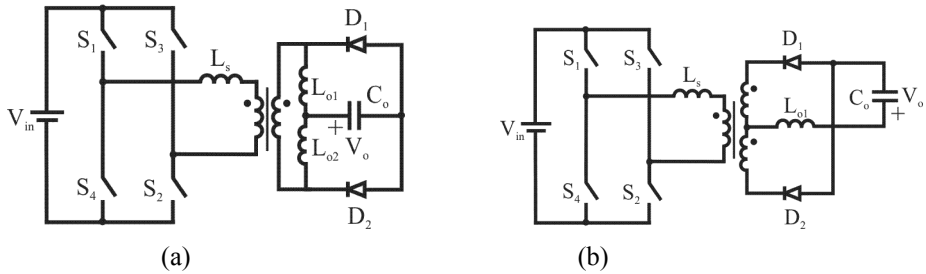



**Fig. 1.** Circuit diagram of the current doubled rectifier (a) and (b) the center tapped rectifier.

Using synchronous rectifier (SR) is a very common way to cope with high conduction losses especially in the low output voltage applications (Xu et al., 2005; Xie et al., 2001 & Zhang et al., 2003). In (Badstuebner et al., 2010), a design evaluation which uses parallel connected SRs in order to obtain best efficiency has been proposed and 99% efficiency has been achieved at 25 kHz operation frequency. However, active gate driver design for parallel connected SRs increases complexity and makes systems heavy due to the requirement of large PCB surface to place SRs drivers and their isolated power supply. Obviously, self-driving method directly using power transformer to generate driving signals seems more attractive compared to active gate drive method, due to its simplicity and easy implementation, especially when SRs are connected in parallel.

In this paper, a synchronous rectified PSFB converter design approach for server adapter is presented. A current doubled rectifier is determined for the secondary side of the converter and the IM model proposed by Xu (2000) is used to eliminate the use of three different magnetic components and decrease the connection losses. In addition, parallel connected SRs are used for current doubled rectifier on the secondary side, to reduce high conduction losses and a self-driven circuit is determined to avoid the need for an additional active control circuitry on the secondary. Thus, the transformer, the output inductor and the self-driver of SR are integrated in one transformer. The operation of the design approach and its analytical loss analysis are presented. The loss breakdown of the proposed design approach is also extracted and compared to conventional DRCT PSFB converter. The performance of the proposed design is

validated by a prototype rated 1kW, with 12V output voltage and 350V-400V DC input voltage. Finally, an efficiency comparison is given for synchronous rectified self-driven CDIM PSFB converter and DRCT conventional PSFB converter.

## THE OPERATION OF SYNCHRONOUS RECTIFIED CURRENT DOUBLER PHASE SHIFTED FULL BRIDGE CONVERTER

The schematic diagram of the synchronous rectified CD PSFB converter is shown in Fig. 2. Here, $S_1$-$S_4$ are the primary side switches and they include antiparallel diodes and parasitic capacitors. $SR_1$ and $SR_2$ represent the parallel connected synchronous rectifier in order to reduce conduction losses. $L_s$ is the equivalent inductance, which is the sum of total leakage inductance and additional inductance connected in series to primary side. TR is the high frequency power transformer with N turns ratio, $L_{o1}$, $L_{o2}$ and $C_o$ are output filter components and $V_{in}$ is the input voltage source.

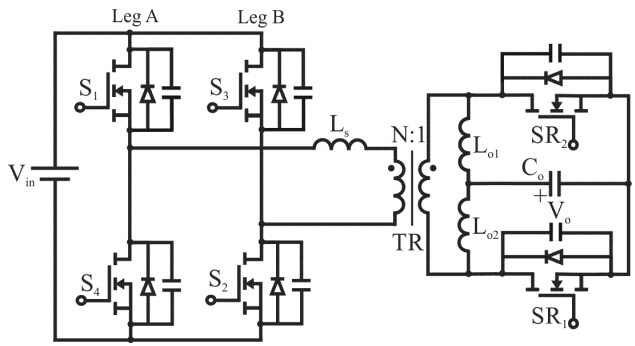
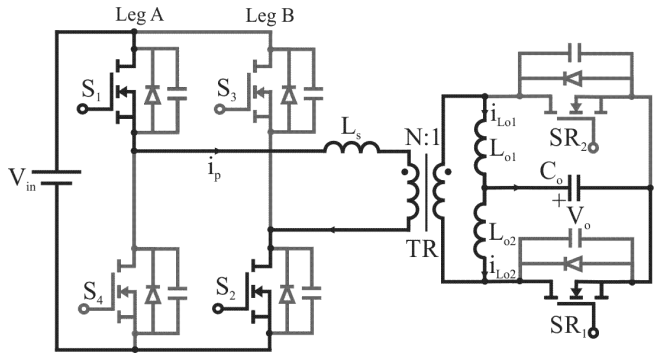



**Fig. 2.** The schematic diagram of synchronous rectified CD PSFB.

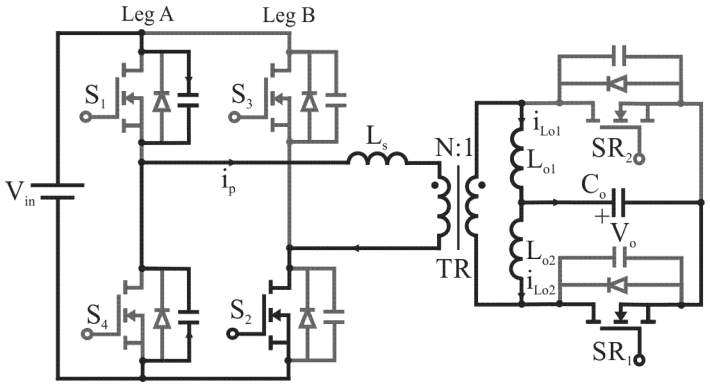
In the analysis of the circuit, semiconductor devices, inductors and capacitors are assumed to be ideal. Also it is assumed that output inductances are high enough and their current is constant for one switching cycle. The half switching period of the converter consists of five modes. The equivalent circuit diagram of the operation modes and operational key waveforms are shown in Fig. 3 and Fig. 4, respectively.

### State 1: ($t_o$-$t_1$)

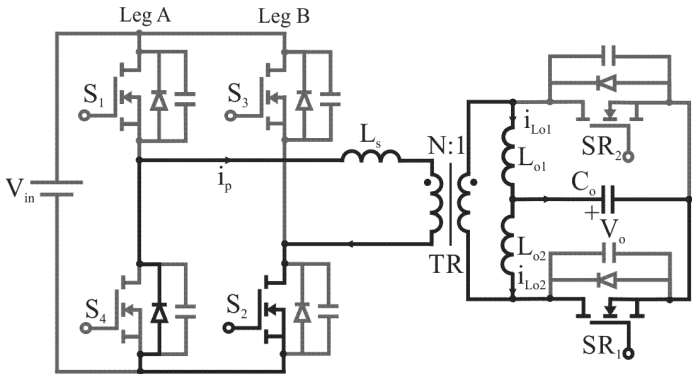
In this state, $S_1$ and $S_2$ are turned on and $V_{in}$ is applied to across the primary of the transformer. The primary current increases linearly from $I_{p1}$ to $I_{p\text{-}pk}$. On the secondary side, $L_{o1}$ charges and $L_{o2}$ discharges by the conduction of $SR_1$. $SR_1$ carries both inductors current. The power is transferred from the input to the output. The variation of the current through the primary windings and the output inductors can be written as follows,



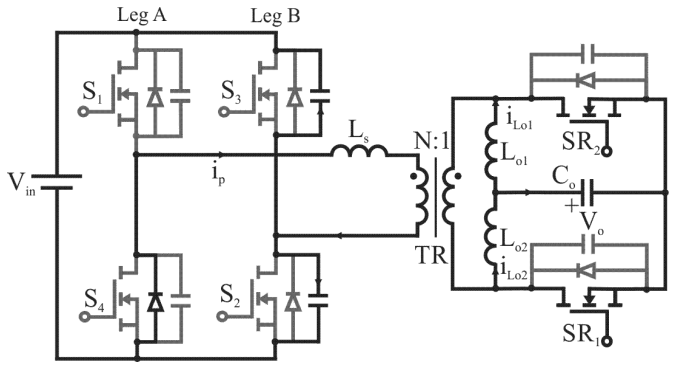

(a) ($t_o$-$t_1$)



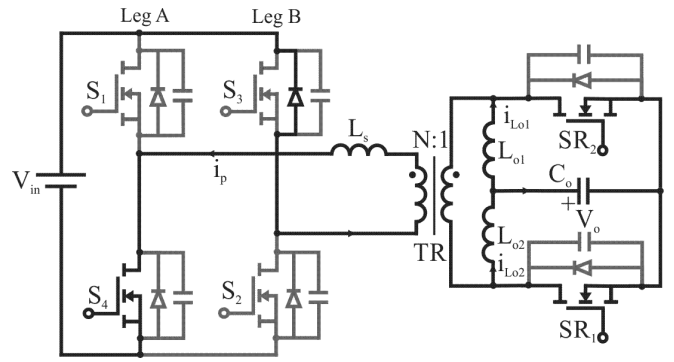

(b) ($t_1$-$t_2$)




(c) (t2-t3)




(d) (t3-t4)




(e) (t5-t6)

**Fig. 3.** The circuit scheme of the CD PSFB converter.

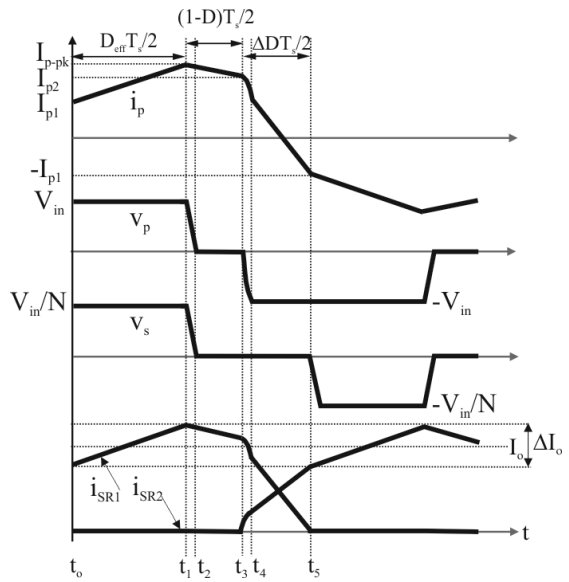



**Fig. 4.** Operational key waveforms of CD PSFB converter.

$$\frac{di_p}{dt} = \frac{V_{in} - V_o'}{L_{o1}' + L_s} \tag{1}$$

$$\frac{di_{Lo1}}{dt} = \frac{V_{in} - V_o'}{L_{o1}' + L_s} \tag{2}$$

$$\frac{di_{Lo2}}{dt} = -\frac{V_o}{L_{o2}} \tag{3}$$

Where, $V_o$' and $L_{o1}$' are the reflected $V_o$ and the reflected $L_{o1}$ to the primary side, respectively and they can be written as

$$L_{o1}' = N^2 L_{o1} \tag{4}$$

$$V_o' = NV_o . \tag{5}$$

**State 2: (t1-t3)**

At $t=t_1$, $S_1$ is turned-off so that the output capacitors of $S_1$ and $S_4$ are charged and discharged, respectively by the stored energy in the output filter. Since the output current is high enough, ZVS turn on of $S_1$ can be achieved easily. At $t=t_2$, the converter starts working in the freewheeling mode; the primary side of transformer is short-circuited by the conduction of anti-parallel diode $D_4$ and $S_2$ MOSFET. Therefore, there is no power transfer from the input to the output during this interval. Thus, the current slope of the primary and the output inductors during the freewheeling mode can be written as

$$\frac{di_p}{dt} = -\frac{V_o'}{L_s + L_{o1}'} \tag{6}$$

$$\frac{di_{Lo1}}{dt} = -\frac{V_o'}{L_s + L_{o1}'} \tag{7}$$

$$\frac{di_{Lo2}}{dt} = -\frac{V_o}{L_{o2}} . \tag{8}$$

The change of primary current is determined by the $L_{o1}$ and $L_s$. At the end of this stage, the primary current reaches $I_{p2}$ and the operation of the converter passes to the active stage.

**State 3: (t3-t5)**

At $t=t_3$, $S_2$ is turned-off and $S_4$ is turned-on so that the output capacitor across $S_2$ and

$S_3$ is charged and discharged, respectively by the stored energy in $L_s$. The antiparallel diode of $S_3$ conducts after the fact that the output capacitor of $S_3$ discharges completely at $t=t_4$. Then a negative input voltage, $-V_{in}$, is applied to the primary side by the conduction of $D_3$. During this stage both $SR_1$ and $SR_2$ are naturally turned on for output current commutation. Therefore, secondary side of transformer is short-circuited and there is no power transfer from the input to the output during this interval. At the beginning of this state, the charge/discharge interval is very short, so it can be neglected. Thus, the current slope of primary and output inductors can be written as follows:

$$\frac{di_p}{dt} = -\frac{V_{in}}{L_s} . \tag{9}$$

$$\frac{di_{Lo1}}{dt} = -\frac{V_o}{L_{o1}} \tag{10}$$

$$\frac{di_{Lo2}}{dt} = -\frac{V_o}{L_{o2}} \tag{11}$$

The transformer leakage inductance during this mode creates lost duty cycle, $\Delta D$, so that no energy transfer from the input to the output and it can be defined approximately as

$$\Delta D \approx \frac{2(I_o/2)L_s f_s}{NV_{in}} . \tag{12}$$

Where $f_s$ is the switching frequency, $I_o$ represents the load current. At the end of this state, the primary current is changed from $I_{p2}$ to $-I_{p1}$ and the half switching period is completed. The same operation principle with inverse direction of primary current and voltage also works for the remaining half cycle.

The rms primary current is calculated according to given switching states and key waveforms as in Fig. 3 and Fig. 4, respectively as follows:

$$I_{p-rms}{}^2 = \frac{2}{T_s}\left[\begin{array}{l} \int_{t_0}^{t_1}(I_{p1} + \frac{(I_{p-pk} - I_{p1})2f_s}{D_e}t)^2 dt \\ + \int_{t_1}^{t_3}(I_{p2} + \frac{(I_{p-pk} - I_{p2})2f_s}{(1-D)}t)^2(t)dt \\ + \int_{t_3}^{t_5}(I_{p2} - \frac{(I_{p2} + I_{p1})2f_s}{\Delta D}t)^2(t)dt \end{array}\right] . \tag{13}$$

Where D is the duty ratio including ΔD and $D_e$ is the effective duty ratio. $D_e$ can be extracted from voltage gain of converter as

$$D_e = \frac{2V_o N}{V_{in}} . \tag{14}$$

Thus D can be written as

$$D \approx \frac{2V_o N}{V_{in}} + \frac{2(I_o/2)L_s f_s}{NV_{in}} . \tag{15}$$

The operation points of the primary current obtained from switching states can be written as follows:

$$I_{p-pk} = \frac{1}{N}\left(\frac{I_o}{2} + \frac{\Delta I_o}{2}\right) \tag{16}$$

$$I_{p1} = \frac{1}{N}\left(\frac{I_o}{2} - \frac{\Delta I_o}{2}\right) \tag{17}$$

$$I_{p2} = \frac{1}{N}\left[\frac{I_o}{2} + \frac{\Delta I_o}{2} - \frac{V_o'}{L_{o1}' + L_s}(1-D)\frac{1}{2f_s}\right] \tag{18}$$

The same calculation method also works for the secondary current and the switch current.

## INTEGRATED MAGNETIC MODEL

In the proposed design approach, the integrated magnetic model given in (Xu *et al.*, 2000) is used to obtain high efficiency and power density. Fig. 5 shows the magnetic structure. In the model, output inductors are integrated in the main transformer using an air-gap in the central leg. In addition, small flux variation in the central leg is achieved changing primary and secondary connections. Thus, the flux in one outer leg decreases while the flux in the other leg increases and this principle results in low flux variation and low core loss in the central leg.

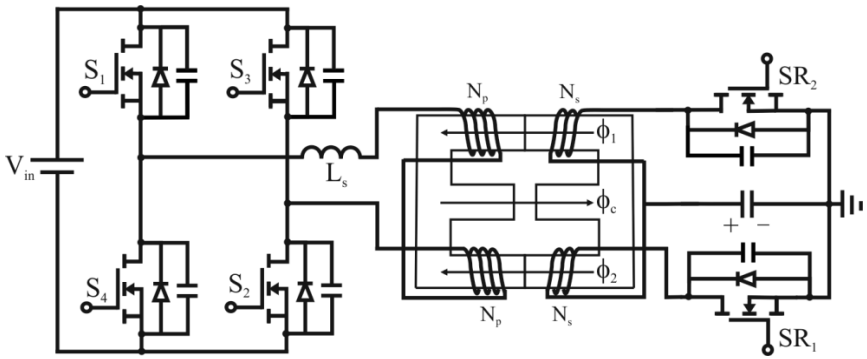


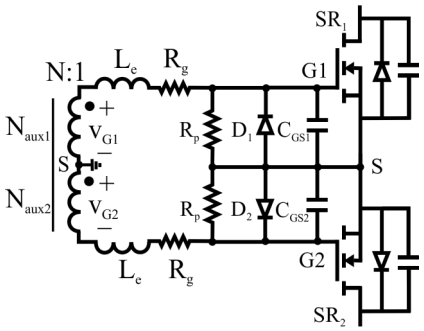

**Fig.5.** The used magnetic model integrating output inductors in the transformer core (Xu *et al.*, 2000).

Integration of output inductor in the transformer core changes the operation principle of the CD PSFB converter. When the primary voltage is positive, $SR_1$ conducts and the current flows only through the lower side secondary windings. The current flow in upper side secondary windings is blocked by $SR_2$. When the primary voltage is negative, the output current flows through the upper side secondary windings. However, the current and voltage variations of the transformer are same as given in Fig. 4.

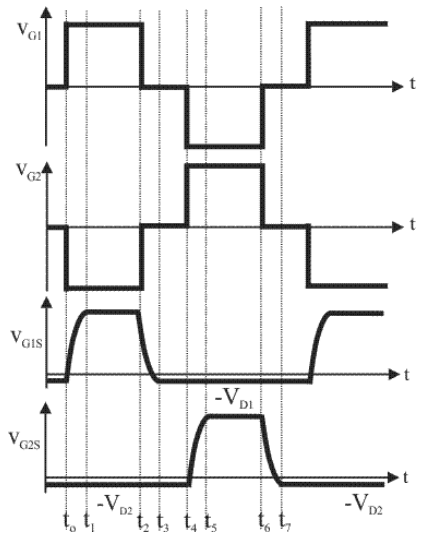
## SELF-DRIVEN PROCEDURE

The self-driven method uses directly power transformer to generate the control signals so its implementation is very simple, cheap and it has an advantage where power density/weight is important like electric vehicle and data center applications (Kolar et al., 2008; Zhao et al. 2009; Badstuebner et al., 2011 & Badstuebner et al., 2010). In this study, auxiliary windings are directly used to drive parallel connected SRs. The circuit schematic of the self-driven circuit, its operational waveforms and its integration in main transformer are given in Fig. 6. Here, the auxiliary windings are integrated directly in the outer legs of the transformer and placed between primary and secondary windings to obtain high coupling.

In the circuit schematic, $C_{GS1}$ and $C_{GS2}$ are the equivalent gate-source capacitance of each SR. $G_1$ and $G_2$ are the gate terminals of the parallel connected SRs and S is the source terminal. Where $L_e$ is the sum of the leakage inductance that comes from the transformer and the trace inductance on the gate line of the parallel connected SRs. The trace inductance is not neglected here as the long interconnection to the gate terminals of the parallel connected SRs. $R_g$ is the gate resistance, which helps the damping of resonance between large gate capacitance and $L_e$ inductance. $R_p$ provides the balance of gate voltages and also helps the damping of resonance on the gate line.




(a)

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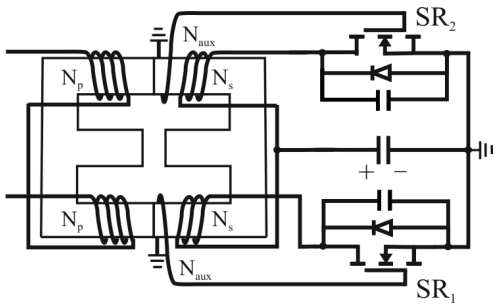


(c)

**Fig. 6.** Self-driven circuit (a), its operational waveforms (b) and its integration in main transformer (c).

When the voltage applied to auxiliary windings is positive, the upper side capacitor is charged and the lower side one is discharged. When $C_{GS2}$ discharges completely, $D_2$ diode conducts and the gate voltage of $SR_2$ is clamped to $-V_{D2}$. When there is a voltage transition of the transformer, each gate voltage stays at zero level and body diodes conduct the current instead of SRs. When the auxiliary voltage is negative, $C_{GS2}$ starts to charge and $C_{GS1}$ discharges. After discharge of $C_{GS1}$, $D_1$ conducts and the gate voltage of $SR_1$ is clamped to $-V_{D1}$. Here, conduction of $D_1$ and $D_2$ diodes results in lower conduction loss during the turn-off state.

The performance of self-driver depends on coupling between the auxiliary winding and rest of windings of the transformer. Leakage inductance of auxiliary winding should be as small as possible to get reliable and quality driving signal. Therefore, auxiliary windings are placed between the primary and the secondary windings in each outer leg of the transformer (Alou *et al.*, 2001).

## LOSS ANALYSIS

### Semiconductor Losses

Semiconductor loss at the primary side includes conduction loss, gate drive loss, turn-off switching loss and output capacitor's discharge loss during the turn-on transition under the partial load conditions. The conduction loss of one switch can be written as

$$P_{sw,con} = I_{sw,rms}{}^2 . R_{DS,on} \tag{19}$$

Here, $I_{sw,rms}$ is the rms value of the current flowing through the MOSFETs. Since the turn-off current for each leg is different so the turn-off switching losses have to be calculated separately. Turn-off switching loss for leg A can be calculated as follows

$$P_{sw,off} = \frac{1}{2} V_{in} I_{p-pk} f_{sw} t_{rv} . \tag{20}$$

Where $I_{p\text{-}pk}$ is the turn-off switch current of switches in leg A and $t_{rv}$ is the voltage rising time given in datasheet.

Due to ZVS turn-on properties of the converter topology, turn on switching loss can be neglected. However, under partial load condition dead time is not enough to discharge output capacitor of MOSFETs in leg B and turn-on switching loss takes place as a function of the remain voltage across the output capacitors. Therefore, capacitors have to be discharged by the MOSFETs and turn-on switching loss under partial load conditions can be written as

$$P_{sw,on} = \frac{1}{2} C_{p,LegB} V_{rem}{}^2 f_{sw} \quad (21)$$

Here, $C_{p,LegB}$ equivalent output (parasitic) capacitor of MOSFETs in Leg B and $V_{rem}$ is the remain voltage which has to be discharged by the MOSFET. If turn-on resistance of MOSFET is neglected, remaining voltage can be calculated based on the series resonant circuit composed of $L_s$ additional inductance and output capacitance of the MOSFET,

$$V_{rem} = V_{in} - \sqrt{\frac{L_S}{C_{p,LegB}}} I_{pr,rms} \quad (22)$$

The gate drive loss can be calculated based on the switching frequency, total gate charge, $Q_{gate}$, obtained from datasheet, and applied $V_{gs}$ voltage to the gate terminal. Drive loss for secondary side can be calculated as follows

$$P_{Drive} = Q_{gate} f_{sw} V_{gs} \quad (23)$$

On the secondary side, SRs losses consist of conduction loss and gate charge losses. Due to the fact that SRs are turned on and off, while the body diode conducts, switching losses can be neglected. Body diode of SR conducts when self driver voltage drops under the threshold voltage during the freewheeling interval and output current commutation stage. Therefore body diode conduction losses should also be taken into consideration. The reverse recovery losses at the beginning of the conduction period can be neglected due to zero voltage drop across the SR. However, at the end of conduction period, reverse recovery loss occurs because of the voltage rising across the SR. Reverse recovery power losses can be calculated as follows

$$P_{BDrr} = Q_{rr} f_{sw} V_{DS,SR} \quad (24)$$

Here, $Q_{rr}$ is the reverse recovery charge of the body diode and $V_{DS,SR}$ is the drain-source voltage of the SR and it is determined by

$$V_{DS,SR} = \frac{V_{in}}{N} + V_o \quad (25)$$

The conduction losses for parallel connected SRs on the secondary side can be written as given in equation (26). Here, $I_{rms,SR}$ is the rms value of the SR current and $n_{SR}$ is the number of parallel connected SRs.

$$P_{sw,SR} = \frac{I_{rms,SR}{}^2 . R_{DS,on}}{n_{SR}} \quad (26)$$

The body diode conduction losses can be calculated as

$$P_{D-SR,con} = 2.I_{D-SR,av} V_{D-SR,FW} \tag{27}$$

where $I_{D\text{-}SR,av}$ is the average value of the body diode current and $V_{D\text{-}SR,FW}$ is the voltage drop of the body diode.

**Magnetic components losses**

Magnetic components losses include core and winding loss of the transformer and output inductor. In the determined IM model, the flux density in each core leg is different compared to the conventional transformer design. The variation of flux density in each leg of the transformer can be calculated as:

$$\Delta B_1 = \frac{V_o D T_s}{2 N_s A_{c1}} \tag{28}$$

$$\Delta B_2 = \frac{V_o (1-D) T_s}{2 N_s A_{c2}} \tag{29}$$

$$\Delta B_c = \frac{V_o (1-2D) T_s}{2 N_s A_{cc}} \tag{30}$$

Where $N_s$ is the secondary turns ratio and $A_{c1}$, $A_{c2}$, $A_{cc}$ are the cross section areas of each outer legs and center leg, respectively. To prevent core saturation, maximum flux variation in each leg should be taken into consideration (Chen *et al.*, 1997). The maximum flux density $B_m$ can be defined as half of the peak to peak flux variations given above. Used integration magnetic model gives small magnetic flux density variation in the central leg as defined in (30) and leads to decreased core losses.

The output inductor is adapted by and air-gap in the central leg. DC flux caused by constant output current in the central leg and core saturation can be checked by

$$B_{c-dc} \approx \frac{N_s I_o}{A_{cc}(2\Re_c + \Re_o)} . \tag{31}$$

Where $_c$ and $_o$ are the reluctance of the center leg and each outer legs of the transformer, respectively. The core loss can be calculated according to Steinmetz equation given in (Venkatachalam *et al.*, 2002).

$$P_c = K f_{sw}{}^{\alpha} B_m{}^{\beta} V_C \tag{32}$$

In the above equations, K, $\alpha$ and $\beta$ can be extracted from curve fitting and $V_C$ defines the core volume.

To obtain large filling factor, foil windings are considered for transformer and output inductor. The DC resistance of the foil windings can be calculated as follows according to physical parameters of the foil such as length, $l_f$, thickness, $t_f$, and width, $w_f$:

$$R_{dc} = \frac{\rho l_f}{t_f w_f} \tag{33}$$

The copper loss of the transformer taking into consideration dc resistance can be calculated according to given calculations for the rms value of the primary and the secondary current.

The volume of the core is determined based on core losses and winding losses. The maximum flux density close to saturation leads to small core or less primary turns number and also increased core losses. The minimum core losses can be obtained with large core but copper losses will increase due to longer turns of foil or litz wire. However, increasing copper loss can be handled with larger foil width or much more multiple litz wires. In this work, core and copper losses are determined as close to each other to reach optimum design.

## OPTIMIZATION AND EXPERIMENTAL RESULTS

The design optimization is carried out taking into consideration a constant switching frequency. The prototype of the circuit is designed for 80 kHz operating frequency, 400 V as input voltage, 12 V as output voltage and 1 kW as output power. Optimized components of synchronous rectified CDIM PSFB and DRCT PSFB converter according to losses analysis given above are presented in Table 1. Cool MOS switches are used in each design approach and five MOSFETs in parallel are used on the secondary side for synchronous rectified CDIM PSFB converter design.

According to losses analysis given above, calculated loss breakdown for synchronous rectified CDIM PSFB and conventional DRCT PSFB is extracted and given in Fig. 7. As shown in the graph, the total losses are dominated by the rectifier conduction losses due to the low output voltage and high output current. Usage of SRs in parallel decreases the conduction losses by half compared to DRCT PSFB design. Determined self-driving method does not allow SRs to conduct in whole conduction period. When auxiliary winding voltage is zero during freewheeling mode and output current commutation mode, high output current flows through the body diode and limits the benefit of parallel connected SRs.

**Table 1.** Optimization of circuit components

| **Components** | **Optimization of SRCD-IM PSFB for $D_{eff}$=0.82** | **Optimization of DRCT PSFB for $D_{eff}$=0.41** |
|---|---|---|
| Integrated Magnetic | Epcos E65/32/27<br>N87 Material, $N_p$=12, $N_s$=1<br>$B_m$=0.12T | Epcos E65/32/27<br>N87 Material, $N_p$=12, $N_s$=1<br>$B_m$=0.07T |
| Primary Winding | Copper Foil,<br>$t_f$=0.1mm $w_f$=36mm | Copper Foil,<br>$t_f$=0.1mm $w_f$=36mm |
| Secondary Winding | Copper Foil<br>$t_f$ =0.2mm $w_f$=36mm | Copper Foil<br>$t_f$ =0.2mm $w_f$=36mm |
| $S_1$-$S_4$ MOSFETs | Cool MOS SPW55N80C3 | Cool MOS SPW55N80C3 |
| $SR_1$-$SR_2$/DR | 5xIRFP4110Pbf | DSS2x101-015 |
| Output Inductor | 1.3µH, $B_{c\text{-}dc}$=0.2T | 1µH, AMCC320, $N_{Lo}$=1, $B_{c\text{-}dc}$=0.1T |
| Additional Inductor | 1.8µH | 1.8µH |
| Output Capacitor | 12x22µF Ceramic Capacitor | 12x22µF Ceramic Capacitor |

Measured current and voltage waveforms of primary and secondary side are given in Fig. 8 and 9, respectively, and are good match with the theoretical analysis. Fig. 10 shows the output current and the voltage across SR.

To evaluate performance of the synchronous rectified CDIM PSFB converter and conventional DRCT PSFB converter, an efficiency comparison is given in Fig. 11. The efficiency of DRCT PSFB converter is measured with the removal of the control signal of the SRs in CDIM PSFB converter design. The efficiency of the synchronous rectified CDIM PSFB converter, fully loaded, is 10% higher than DRCT conventional PSFB converter. To increase the efficiency more, the self-driving circuit behavior should be improved further to providing full conduction of parallel connected SRs.

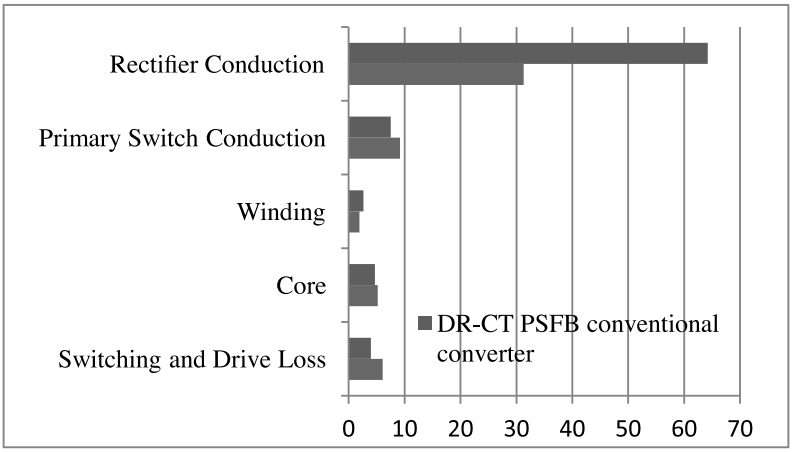


**Fig. 7.** Calculated losses breakdown comparison of synchronous rectified CDIM and DRCT PSFB converter.

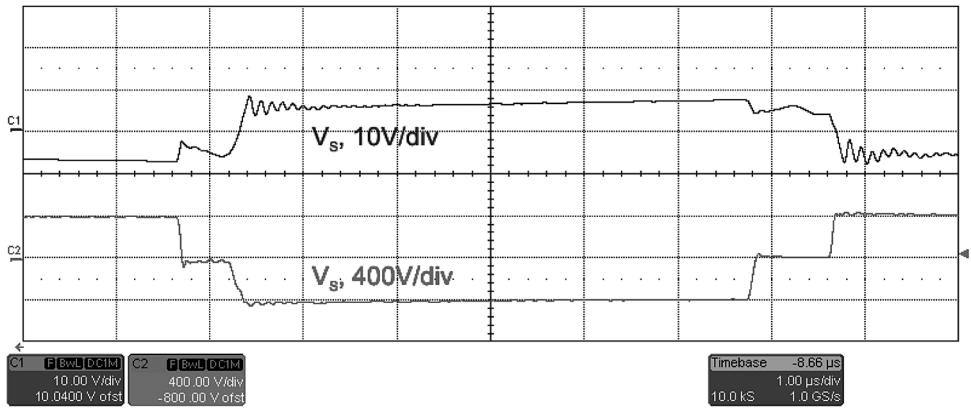


**Fig. 8.** The voltage and the current waveforms of primary side.

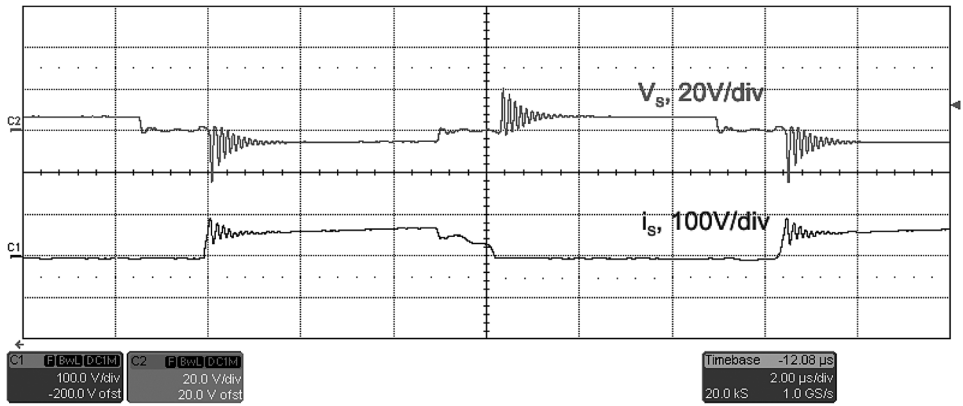


**Fig. 9.** The voltage and the current waveforms of secondary side.

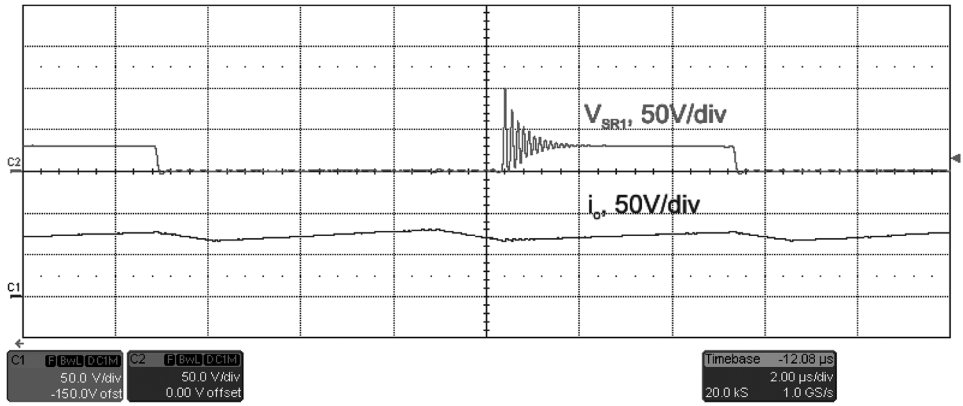


**Fig. 10.** The waveforms of the voltage across SR and the output current.

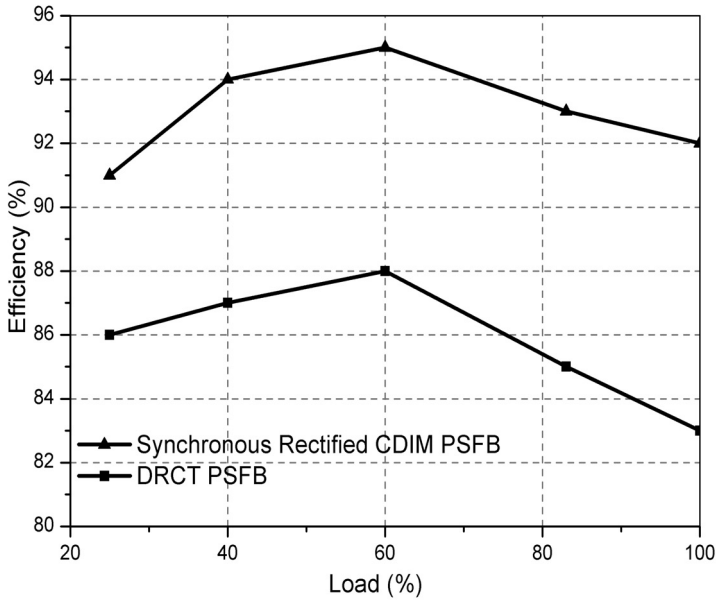


**Fig. 11.** Measured efficiency comparison of synchronous rectified CDIM PSFB converter and DRCT conventional PSFB converter.

## CONCLUSION

In this work, a design study of a self-driven synchronous rectified CDIM PSFB converter for server adapter applications is described analytically and its operation is validated experimentally. In this design approach, implementation of IM and parallel connected synchronous rectifier increases efficiency compared to conventional DRCT rectified PSFB converter with separate magnetic. The design is planned for 1kW output power, 350V-400V input voltage and 12V output voltage. Due to low output voltage and high output current application, total loss is dominated by SR conduction loss. To increase efficiency further, performance of self-driving method should be improved to prevent body diode conduction and its high conduction losses. Obtained maximum efficiency is around 10% higher than conventional diode rectified center tapped PSFB converter at full output condition.

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