Zero Voltage Switching Self-oscillating PWM Inverter in Induction Heating Applications

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ABSTRACT

A new phase shifted zero voltage switching (ZVS) self-oscillating pulse width modulation (PWM) high frequency stage-3 inverter with flying capacitor and neutral point clamp diodes for an induction heating application is presented in this paper. To achieve the peak voltage with less- harmonic output at above resonant frequency, this network has been customized and changed in reference with full-bridge network topology. Then, an input dc voltage equal to $V_{d/2}$ applied to control stress of device voltage. The model is operational between 50 and 80 kHz at the rated 440V dc voltage and can feed maximum power of 1000W to the grid. The heating as well as hardening of the iron has been done at 800°C temperature. The principle of operation of phase shifted AM-ZVS-PWM inverter along with the experimental results are presented in this paper to verify the performance of the system.

Keywords: Induction heating, Stage-3 inverter, Zero-Voltage switching, Amplitude modulation (AM).

INTRODUCTION

In past few years, many authors have performed the half and full bridge prototype of the high frequency soft switching PWM converters. Although, FB-PWM posses desirable characteristics of hard and soft switching neglecting losses such as conduction and commutation losses (Ó. Lucía et al., 2014 , T. Lubin et al., 2009, T. Hirokawa et al., 2012 and

H.W. Koertzen et al., 1995). However, it may not be possible to get adequate switches in high level of input voltage. These aspects occur mainly in inverter topologies that use the bridge inverter structure. This phase shifted AM Zero voltage switching PWM inverter applied for induction heating applications is proposed to diminish the voltage problem of the switches and conduction losses due to maximum voltage rating of switches. Switching losses are also increased during commutation process due to increased switching frequency (I. Millánn et al., 2011 and H.P. Park et al., 2018). Even, on applying soft switching methods the switching losses in power supply units can be substantially enough because of the less conversion efficiencies (C. Jiang et al., 2017 and K. T. Chau et al., 2017). Due to hard switching operation the power losses of the switches are lower than snubberless circuit. At high frequencies switching losses are less in resonant inverter mode (F. Canales et al., 2002 and H. P. Ngoc et al.,2011). For high frequency phase shifted ZVS operation MOSFET are the suitable device for resonant inverter though it possess relatively high stress on device, flow of current and conduction losses and also suitable for wide range voltage and current applications. These inverter operates at frequency greater than resonant switching frequency (H. Sarnago et al., 2014). Hence, based on such features, a phase shifted AM-ZVS-PWM inverter for series mode of resonant is shown in Figure 1.

NETWORK MODEL

Figure 1 shows the circuit configuration of phase shifted AM-ZVS-PWM converter for induction heating applications. To design the operational circuit of this high frequency inverter four MOSFETs ($S1, S1', S2, S2'$) are used. The voltage and current rating of MOSFETs are 400V and 12A respectively. The rating of capacitor used as snubber capacitor ($C1, C2, C3, C4$) is 440pF which is interlinked to drain terminal and source terminal of each MOSFET switch. Filter inductor and filter capacitor are denoted by L_f and C_f respectively. The smoothing capacitors C_{dc1} and C_{dc2} for dividing input voltage, flying capacitor C_{ss} and neutral voltage clamping diodes D5, D6 are used. The output terminals A and B in the phase

shifted AM-ZVS-PWM inverter are connected to input of the transformer having turn ratio of 3:1. I_{pr} , L_{pr} , R_{pr} are the current ,and I_{se} ,L_{se} , R_{se} are the primary and secondary currents, inductances and resistances respectively.

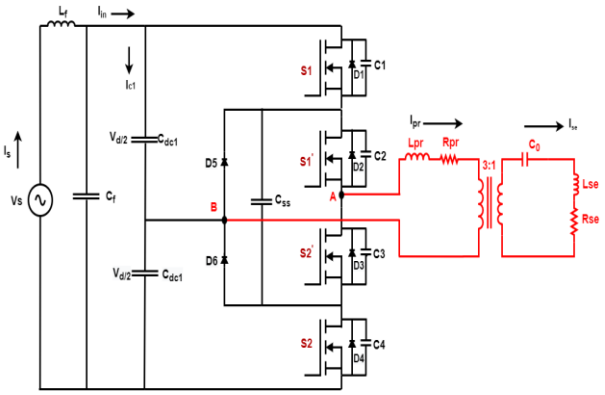


Figure 1. AM-ZVS-PWM network of the proposed system.

PRINCIPLE OF OPERATION

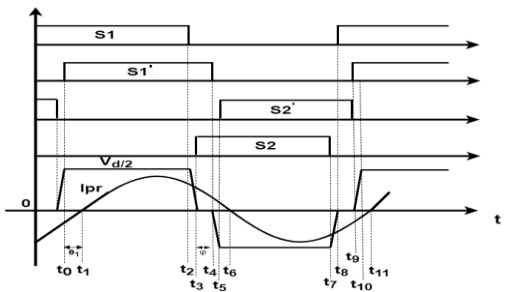
The AM-ZVS-PWM inverter operation for induction heating application is explained from the equivalent network of the induction system. The basic operating principle of induction system is identical to the transformer. In induction system, the main coil is the primary winding and the output terminal where the load is connected is the secondary winding having single turn as represented in Figure 1. The resistance and inductance in the secondary winding is denoted by R_{se} and L_{se} and in the primary winding by R_{pr} and L_{pr} respectively, as shown in Figure 2. The L_{eq} and R_{eq} which shows the equivalent value and mathematically developed as depicted in equation (1) and (2). All these particular components are added to C_0 referred to the primary side and mathematically depicted in equation (3), in which the number of turn in induction coil is denoted by N and in the transformer side is by n.

$$L_{eq} = L_{pr} + 1^2 L_{se} \quad (1)$$

$$R_{eq} = R_{pr} + 1^2 R_{se} \quad (2)$$

$$C_{eq} = 3^2 C_0 \quad (3)$$

The resonant circuit connected in series and



operates under resonating condition of the proposed inverter as given in Figure 1. The resonating capacitor C_0 resonating with L_{eq} . Therefore, the overall process of proposed inverter and the operational waveforms at a particular phase shifted angle φ can be evaluated in ten different modes as depicted in Figure 3. Figure 4 shows the turn on and turn off sequence for modes 1 & 2 respectively, after applying discrete Fourier transformation to the output voltage V_{out} the RMS value of switching frequency is obtained. The resonant converters can be considered as AM sinusoidal waveforms after neglecting harmonics. The effect of dead time in the converter on switching sequence is shown in figure 5.

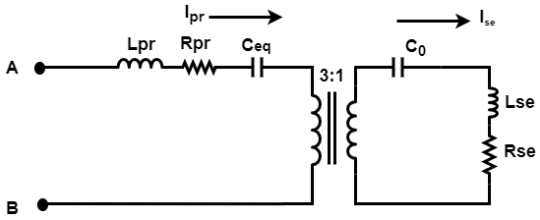


Figure 2. Equivalent network of the proposed system.

Figure 3. Operational waveforms at particular phase shifted ϕ.

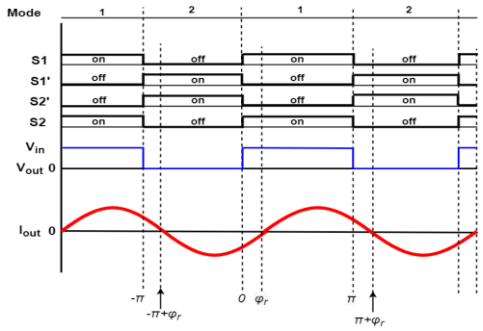


Figure 4. Gate signal sequence and output waveform mode 1 & 2

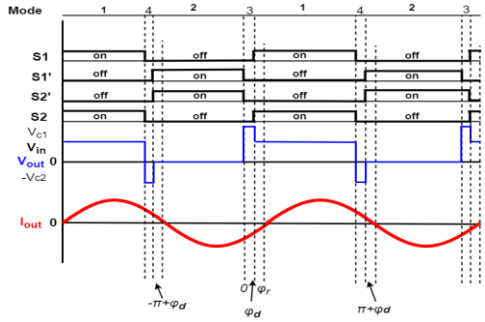
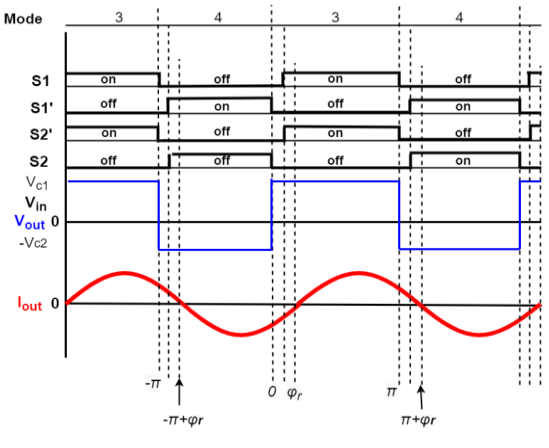


Figure 5. Gate signal sequence and output waveform mode 1 & 2 considering dead time.

In mode 3 and 4 both capacitors have voltage then the switching sequence are presented in Figure 6, in which dead time is considered and assumes the voltage of both the capacitors should be greater than zero. Similarly, Figure 7 represents the switching sequence where only voltage of capacitor C2 is considered which is zero under mode 3 and 4.



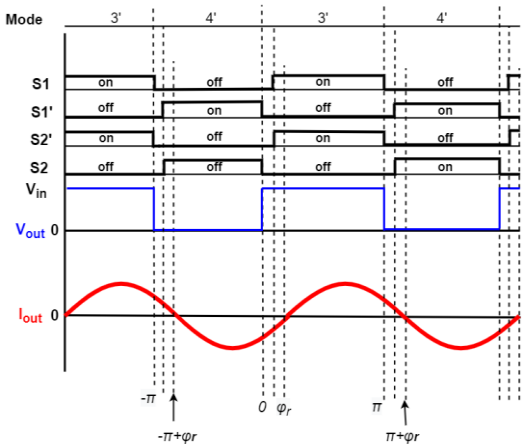


Figure 6. Switching signal sequence and output waveform when capacitors having voltage.

Figure 7. Gate signal sequence and output wave Capacitor C_2 reaches 0V.

Figure 8 and 9 shows the characteristics of capacitor voltage in mode 1, 2 and mode 3, 4 respectively. The voltage appears in Figure 8 consists of two components namely offset voltage component and main frequency component of alternating current. The small ripples are always observed in voltage across capacitors during the complete operation as shown in Figure 9. The operational modes of overall proposed phase shifted AM-ZVS-PWM inverter is presented in Figure 10.

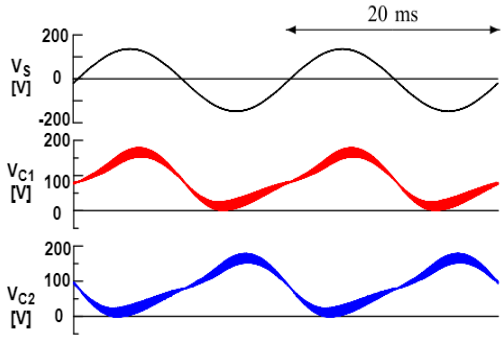


Figure 8. Characteristics of capacitor voltage in mode 1 mode 2.

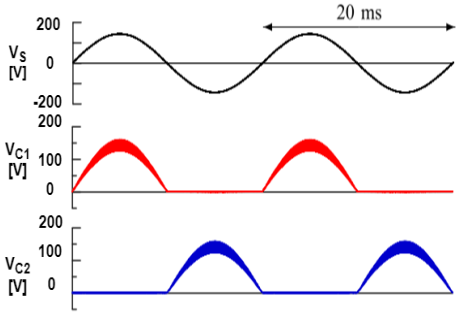


Figure 9. Characteristics of capacitor voltage in mode 3 and mode 4.

Mode-1 $(\mathbf{t_1 - t_2})$: The power passed from the input side to the load terminal with its parameters like C_{eq} , R_{eq} , and L_{eq} respectively. The S 1 and S 1′ gets ON at this operating mode. However, the amplitude of the primary side voltage is identical with secondary side voltage i.e; $V_{d/2} = V_{ab}$. The circuit diagram is shown in Figure 10(a).

Mode-2 $(\mathbf{t_2 - t_3})$: Under this mode of operation, S 1 is turned OFF at time t_2 . This discharges C4 as well as the input current charges C1 pass through C_{ss} (the flying capacitor). Moreover, the diode D_1 starts to operate when the voltage of capacitor C1 exceeds the input voltage $V_{d/2}$. Simultaneously, the diode D_4 starts to operate when the voltage of capacitor C4 decays to zero. This event can be understood from the Figure 10 (b)

Mode-3 ($t_3 - t_4$): Under this mode of operation, C1 gets fully charged as well as C4 is completely discharged. The input current (I_{pr}) freewheels through Diode D_5 and S 1′. S 2 begins to conduct at this time. Figure 10 (c) shows the circuit.

Mode-4 ($t_4 - t_5$): In this mode, the switch S 1′ gets completely OFF at time t_4. Then the voltage across C2 increased up to $V_{d/2}$ and the voltage of capacitor C4 decays to zero. The diode D_4 conducts in this mode as shown in Figure 10(d).

Mode-5 ($t_5 - t_6$): Figure 10 (e) shows the input current (I_{pr}) freewheeling with diode D_3 and D_4 at t_5. Hence, at zero voltage switching condition switches S 2′ and S 2 gets turned ON.

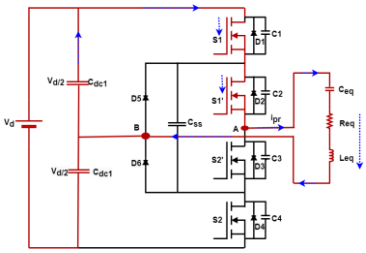
Mode-6 ($t_6 - t_7$): At this mode, the input current (I_{pr}) starts to flow in the opposite direction i.e.; from S 2′ and S 2 at t_6. In this mode of operation the input current (I_{pr}) reaches the load current in the output side as shown in figure 10(f).

Mode-7 ($t_7 - t_8$): During this time period t_7, S 2′ is in ON condition but S 2 is at OFF condition. Now, due to input current flowing through the flying capacitor C_{ss}, the voltage across capacitor C4 increases and voltage across capacitor C1 decreases, as presented in Figure 10(g).

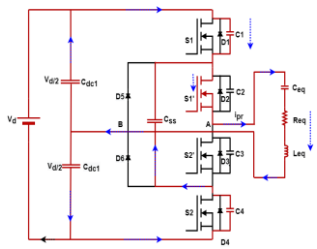
Mode-8 ($t_8 - t_9$): In this mode of operation, C_1 is charged and C_4 is discharged completely. Now, the input current (I_{pr}) freewheels through diode D_6 and switch S 2′. Switch S 1 is about to begin conduction at this time. Figure 10 (h) shows the circuit.

Mode-9 ($t_9 - t_{10}$): Switch S 2′ gets OFF at t_9. The input current flows through C2 and C4, due to which the capacitor voltage C4 increases up to $V_{d/2}$ and decays to zero across C2. The diode D_1 is in ON condition. This switching phenomenon is shown in the Figure 10 (i).

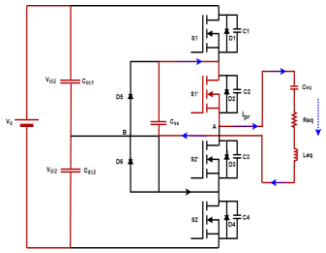
Mode-10 ($t_{10} - t_{11}$): Under this mode at time t_{10}, the input current (I_{pr}) freewheels through diodes D_1 and D_2. Hence, under zero voltage switching condition switches S 1 and S 1′ gets turned ON.



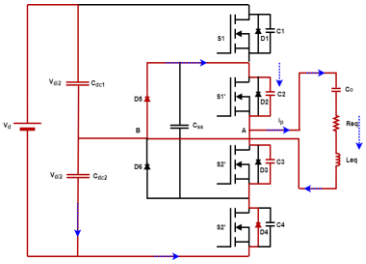
(a) Mode-1 operates during (t_1-t_2)



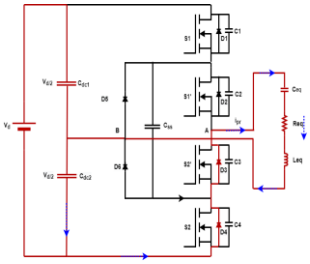
(b) Mode-2 operates during (t_2-t_3)



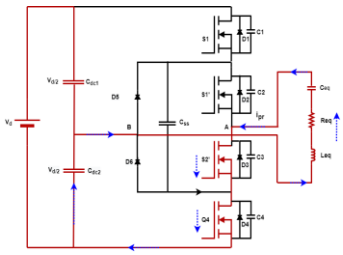
(c) Mode-3 operates during (t_3-t_4)



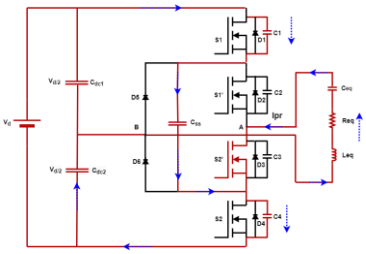
(d) Mode-4 operates during (t_4-t_5)



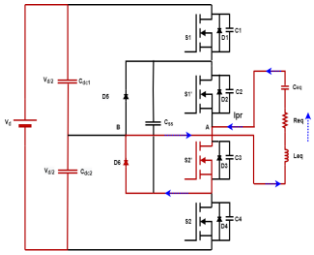
(e) Mode-5 operates during (t_5 - t_6)



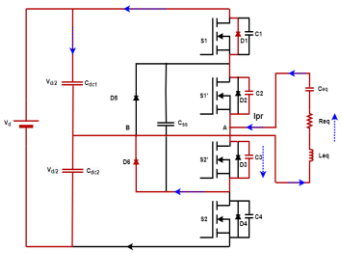
(f) Mode-6 operates during(t_6 - t_7)



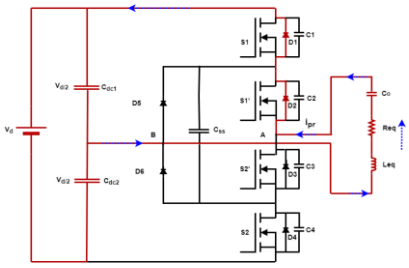
(g) Mode-7 operates during (t_7 - t_8)



(h) Mode-8 operates during (t_8 - t_9)



(i) Mode-9 operates during (t_9 – t_{10})



(j) Mode-10 operates during (t_{10} - t_{11})

Figure 10. Different modes of switching operation of proposed inverter.

The expression of input current (I_{pr}) for all operation modes is shown in equation (4), here θ_1 shows the displacement of power factor.

$$I_{pr} = \frac{4\left(\frac{V_d}{2}\right)\text{Cos}\left(\frac{\emptyset}{2}\right)\text{Cos}(\theta_1)}{\pi R_{eq}}\text{Sin}(wt - \theta_1) \quad (4)$$

ANGLE AT ZERO PHASE SHIFT CONDITION

Few modes were not same with the phase-shifted PWM technique, as the angle of phase-shifted φ is decays to zero. Figure 11 shows the operational wave forms. The instantaneous value of Vs and the phase shift angle φ_S , i.e. output power dependent on the ZVS conditions of $S1 - S2$, are expressed as follows:

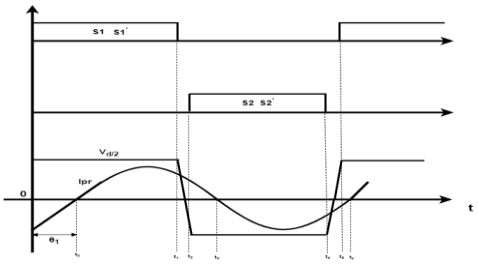


Figure 11. Operational waveforms: ZPS condition

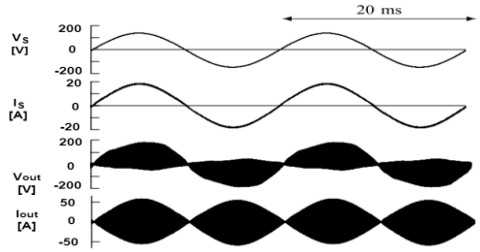


Figure 12. Input and output waveforms in mode 1 and 2

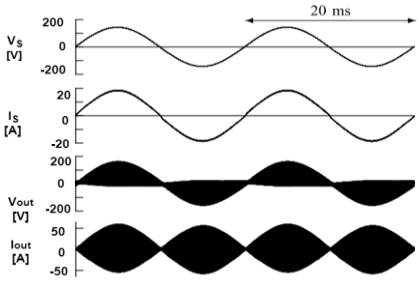


Figure 13. Input and output waveforms in mode 3 and 4.

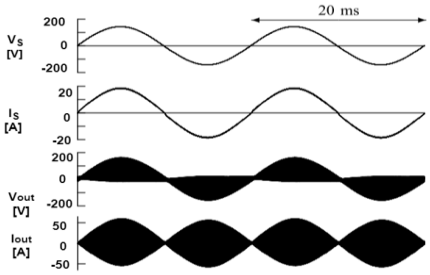


Figure 14. Input and output waveforms of proposed phase shift control.

$$i_{S1,off} > \frac{v_{S1\prime,off}}{Z_{r,fixed}} \quad (5)$$

$$i_{S1\prime,off} > \frac{v_{S1,off}}{Z_{r,fixed}} \quad (6)$$

$$Z_{r,fixed} = \sqrt{\frac{L_0}{C_{s1}+C_{s2}}} \quad (7)$$

$$i_{S2\prime,off} > \frac{v_{S2,off}}{Z_{r,cont.}} \quad (8)$$

$$i_{S2,off} > \frac{v_{S2\prime,off}}{Z_{r,cont.}} \quad (9)$$

$$Z_{r,cont.} = \sqrt{\frac{L_0}{C_{s3}+C_{s4}}} \quad (10)$$

Where $V_{S1,off}$ and $V_{S2,off}$, off are the switching voltage of switches placed opposite to each

other. Similarly, $i_{S1,off}$ and $i_{S2,off}$, are the switching currents flowing opposite to each other. These currents, turn off the switching transition correspondingly. Figure 12 and 13 presented the input and output waveforms in mode 1,2 and 3,4 respectively. The amplitude of the phase currents $i_{S2',off}$, and $i_{S2,off}$, are less than the $i_{S1,off}$ and $i_{S1',off}$ because of pulse width modulation technique. Therefore, to expand the area of zero-voltage switching, the switches S 2 and S 2′ operates without any auxiliary circuits and are set at $Z_{r,cont.}>Z_{r,contition}$. The overall switching behavior is as follows;

Mode-1 ($t_0 - t_1$): At this section, the operation mode of S 1 and S 1′ are identical with the condition of previous mode of phase shifted pulse width modulation. Hence S 1 and S 1′ gets turned ON.

Mode-2 ($t_1 - t_2$): Under this section of (t_1- t_2) duration, S 1 and S 1′ gets OFF. While, due to flow of primary current (I_{pr}) , C1 and C2 getting where as C3 and C4 gets discharged. Hence, small amount of discharged current from C4 is flowing through the flying capacitor C_{ss}.

Mode-3 ($t_2 - t_3$): The path for flow of current is identical to the mode 5 of previous operation. At this stage, the input current (I_{pr}) flows through the diode D_3 and D_4. After that, S 2′and S 2 gets turned ON for zero-voltage switching condition during freewheeling. Figure 14 shows the input and output waveforms at proposed phase shift control technique.

Mode-4 ($t_3 - t_4$): The operation at this section is identical to Mode-6 of the previous section.

Mode-5 ($t_4 - t_5$): During this mode the switches S 2′and S 2 gets turned OFF at particular time t_4. The input current (I_{pr}) charges capacitor C3 and C4 but C1 and C2 gets discharged, correspondingly. Hence, small amount of discharged current from C2 is flowing through the flying capacitor C_{ss}.The direction of flow of current is illustrated in the Figure 14.

Mode-6 ($t_5 - t_6$): The flow of primary input current (I_{pr}) through phase-shifted scheme of PWM condition similar to the previous section of mode 10 and then under ZVS conditions S 1 and S 1′gets ON particularly at the time of freewheeling.

Harmonic analysis of current signal is done and found the THD value of 13.71% which is better as compared to other modulation methods as shown in Figure 15 and in Table 1.

DESIGN SPECIFICATION

The proposed inverter utilizing phase-shifting control of PWM technique were used as a prototype model as shown in Figure 16 and the specifications of particular parameters are listed in Table 2.

Table 1. Comparison of THD in different PWM techniques

PWM technique	THD(%)
PD-PWM	21.40
POD-PWM	24.67
APOD-PWM	24.34
Proposed AM-ZVS-PWM	13.71

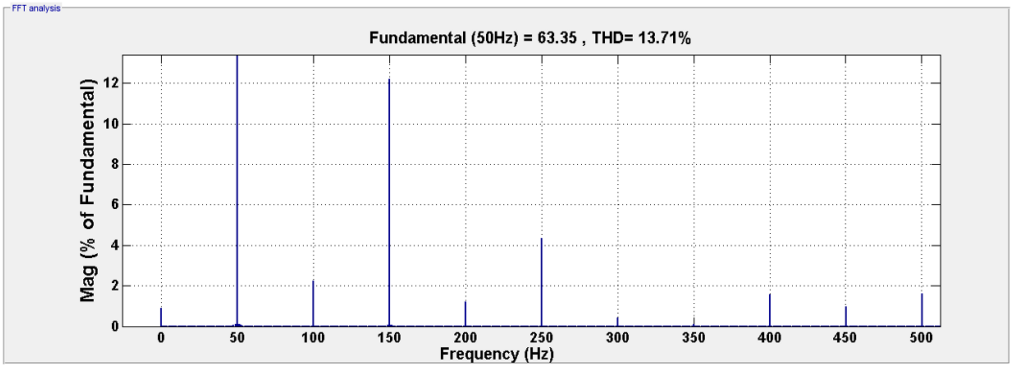


Figure 15. Harmonics analysis of AC side.

Table 2. Circuit parameters

Description	*Values*
AC main frequency	50 Hz
Filter Inductor, L_f	500μH
Filter capacitor, C_f	4 μF
Filter capacitor, C_{dc1} & C_{dc2}	5.5 μF
Flying capacitor, C_{ss}	5 μF
Snubber capacitor, C1-C4	440pF
Switching frequency, f_{sw}	≥ 50 kHz
Rated power	1KW
D_5 and D_6	14CPD05

Turn ratio of transformer, n	3
DC Voltage	440V
C_0	4.2nF
Equivalent inductance, L_{eq}	0.32mH
Equivalent resistance, R_{eq}	13 ohm

An AM-ZVS-pulse width modulation technique based inverter working at the said the switching frequency and utilizing switches were executed in the research lab to check the proposed hardware. It was presented that there exist a dead - time of 700 ns with 0.78 duty cycle highest from the investigation in the power equipment's. The output waveforms of modified circuit for accomplishing the zero voltage - switching have appeared in Figure 8 as referenced early. From the output results it very well may be seen that the zero-voltage exchanging highlights do exist as in when they are working at V_{ds} approaching zero all MOSFETs do turn-on. The exploratory outcomes show the legitimacy of the examination and that they are like the reproduction results.

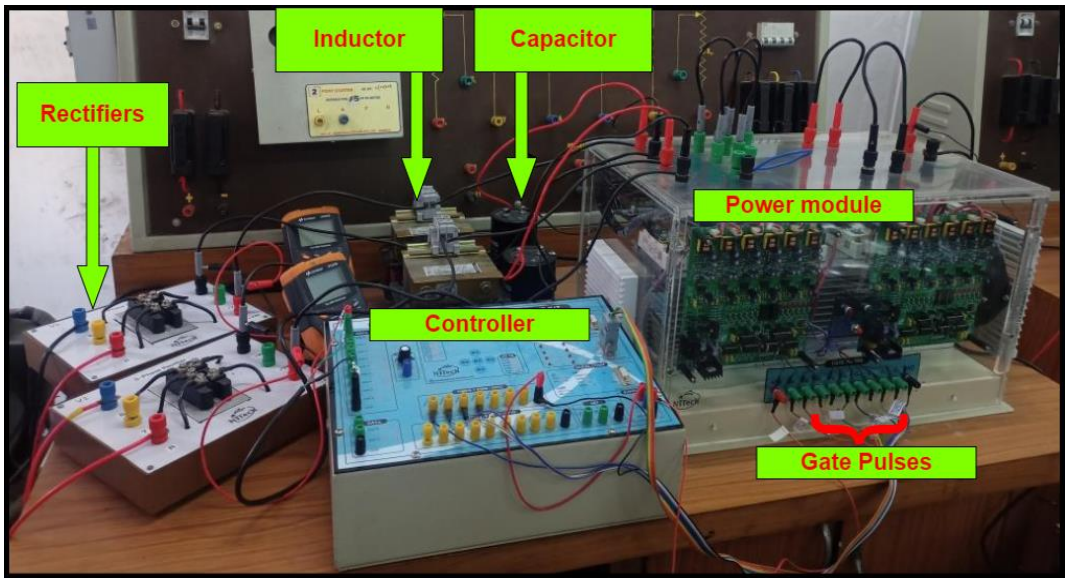
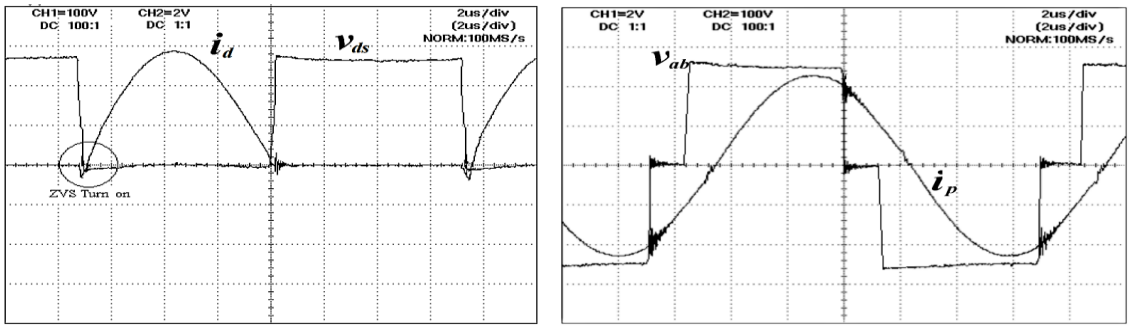


Figure 16: Prototype experimental kit.

Figure 17(a) & (b) shows the yield voltage and essential current at stage moved edge $\phi = 0°$ and $\phi = 45°$. The exchanging resonance is above than the resonance of the essential current slacks the output voltage constantly. Consequently, under ZVS conditions all MOSFETs can be accomplished constantly. As appeared in Figure 17(a), the waveforms

under an alternate point ϕ additionally meet yield power necessity for acceptance heating at ϕ = 0◦ . Additionally, when contrasted and the iron-bar temperature tried for ϕ = 45◦,the waveform of a productivity of framework isn't decreased to such an extent as appeared in Figure 17(b). The most elevated effectiveness at appraised is 91 percent and output power evaluated is 1 kW. The stage moved phase shifted PWM control scheme just as the AM-ZVS-PWM inverter is useful and can be subjected to substantially high power equipment's, for example: IGBT for heating usage. Figure 18 shows the different operation mode relationship between power loss and its output power under phase shift control. Figure 19 shows the switching frequency at different mode and control of phase shift with respect to output power. In Figure 20 power conversion efficiency for mode 1 to 4 is been considered at various output power.



(a) (b)

Figure 17: Voltage $V_{drain-source}$ and current id of MOSFET switches at (a) angle φ = 0 ° (b) angle φ = 45°.

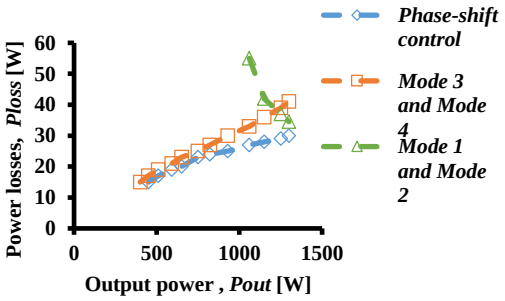


Figure 18: Power loss P_{loss} vs Output power P_{out}

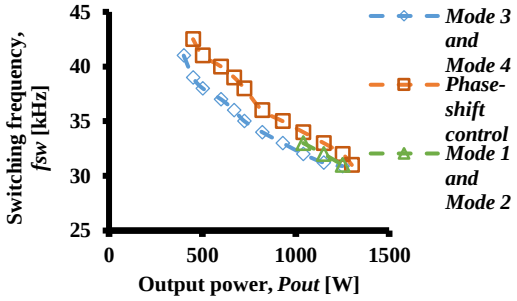


Figure 19: Relationship between switching frequency f_{sw} and Output power P_{out}

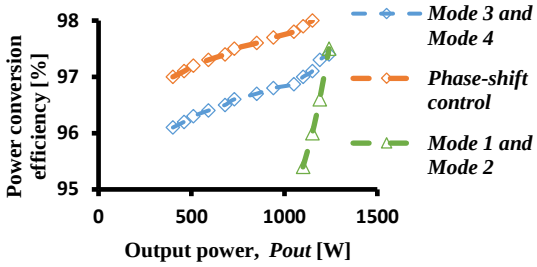


Figure 20: Relationship between power conversion efficiency η and output power P_{out}.

CONCLUSION

The output power delivered by the proposed phase shifted AM-ZVS-PWM inverter can be further increased by utilizing peak amplitude of calculated dc input voltage. The observed voltage around the switches is a part of the primary voltage. The proposed method present a phase difference between gate signals to enable capacitor voltage control in half-bridge inverters and achieve zero voltage switching, thereby making synchronous rectification possible in all the switches. This method regulates the capacitor voltage within a reasonable range by adjusting the phase shift angle between the two half-bridge converters. The operational circuit of the proposed inverter produces a sinusoidal current which has low harmonics. Furthermore, the power conversion efficiency can be improved by the proposed switching sequence. At output power of 1 KW efficiency is evaluated as 91 percent. To verify the working of proposed system theoretical examination, numerical analysis and real time experimental work are presented here.

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