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Practically Realizable Circuits for OTRA and their Implementation in Oscillators

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ABSTRACT

In this paper, practical circuits for operational transresistance amplifier (OTRA) realizable in lab using commercial ICs have been designed and proposed. 3 structures based on operational amplifier (OPAMP-LM741), operational transconductance amplifier (OTA-CA3080) and current conveyors II (AD844) have been proposed. In these proposed designs, conditions to mimic the current-voltage behavior of OTRA have been formulated using active and passive components. Moreover, these components are also used to achieve flexibility in transresistance gain of implemented OTRA. The behavior of the proposed OTRA structures have been validated using LTSPICE. Furthermore, to represent practical usability of these designs oscillator circuit have been designed and implemented on software and experimentally also on bread board. All the results prove the OTRA operation of the designed circuits and their usability in the practical environment.

Keywords: Operational transresistance amplifier (OTRA); Operational amplifier (OPAMP); Operational transconductance amplifier (OTA); Current conveyor-II (CCII).

INTRODUCTION

Current mode signal processing has become increasingly popular in the last four decades due to improvements in bandwidth, slew rate, power consumption etc. [1]. These developments have led to a wide variety of current conveyors and other related building blocks such as current voltage convey or (CVC), dual output current conveyor (DOCC), differential voltage current conveyor (DVCC), differential difference current conveyor (DDCC), third generation current conveyors (CCIII), inverting current conveyors (ICC), fully-differential current conveyors (FDCC), Operational floating conveyor (OFC), Operational transresistance Amplifier (OTRA), Current differencing buffered amplifier (CDBA), Current differencing transconductance amplifiers (CDTA), Voltage differencing transconductance amplifier (VDTA), Current follower transconductance amplifier (CFTA), Four terminal floating nullor (FTFN) etc. [2-4]. Despite their usefulness ICs of such blocks are not commercially available. In this work, objective is to achieve terminal characteristics of a block using commonly available ICs like OPAMP (LM741), CCII+ (AD844), OTA (CA3080) etc.

Operational transresistance amplifier (OTRA) is a high gain, current input and voltage output device. Due to its attractive features like high gain and bandwidth it has involved considerable attention of analog designers and has led to the development of various applications in recent times. OTRA is being used as an alternative basic building block used for realization of a wide variety functions like various filters, oscillators, multivibrators, frequency dependent negative resistor, simulated inductors, MOS-C biquads etc. [2, 5].

It has been observed that OTRA IC is not commercially available. However, a specific OTRA IC named Norton Amplifier LM3900 designed by National Semiconductors is available in market. Though, it has its own limitations. It does not offer the virtual ground characteristic as required at the input terminals of an OTRA and input current is allowed to flow in one direction only [2]. The former disadvantage limits the functionality of the Norton amplifier whereas the later calls for the use of external DC bias circuits leading to complex and clumsy designs even for simple functions.

In this paper, 3 different OTRA configurations have been proposed and implemented using the above mentioned commercially available ICs. Moreover, oscillators have been designed using these proposed OTRAs. The simulations have been carried out in LTSPICE and verified experimentally to justify the authenticity of these circuits. The paper is organized as follows: section 2 explains the functioning of an OTRA. Implementation of OTRA using various basic building blocks is illustrated in section 3. Brief description of OTRA based oscillator circuit is given in section 4. All the simulation and experimental results are presented in section 5, which is followed by conclusions drawn in section 6.

OPERATIONAL TRANSRESISTANCE AMPLIFIER (OTRA)

Operational Trans-Resistance Amplifier (OTRA) is a three-terminal device. Its schematic symbol and equivalent mathematical model is shown in Figure 1 (a) and Figure 1(b) respectively [6, 7].

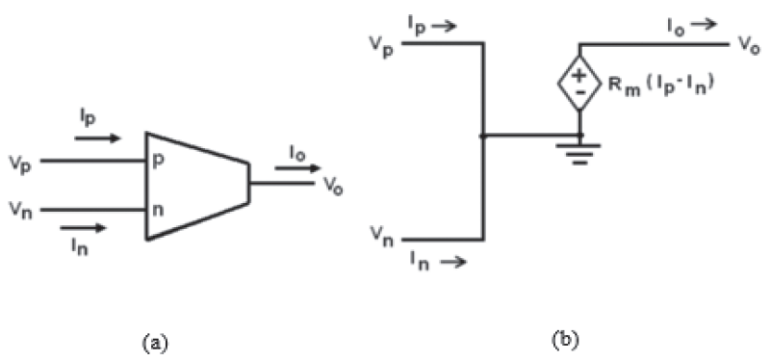

Figure 1. OTRA (a) Schematic symbol (b) Equivalent model.

OTRA amplifies the difference of input currents (Ip and In) and its output voltage (Vo) is expressed as [12]:

$$V_o = R_m\left(\mathrm{I_p} - \mathrm{I_n}\right) \tag{1}$$

here, Rm is transresistance gain of OTRA. In ideal case, Rm approaches infinity and Vp& Vn should be zero, that is two input terminals are at virtual ground. Moreover, Vomust not depend upon current drawn from output terminal (Io). Very high value of Rm leads to saturation of OTRA (output attaining positive saturation voltage (VDD) or negative saturation voltage (VSS)), when used in open loop configuration. For OTRA to be used for linear applications, it must be used in negative feedback configuration. Moreover, input and output impendences of OTRA is low resulting in circuits that are insensitive to stray capacitances making OTRA appropriate for high frequency applications [5, 8].

In literature OTRA has been implemented using CFOA (AD844) [9]. Figure 2 shows this CFOA based implementation of OTRA. This study proposes three more implementation of OTRA using commercially available ICs such as OPAMP, CCII+ and OTA. An oscillator has been implemented using these proposed architectures and simulation and experimental results have been presented in this work.

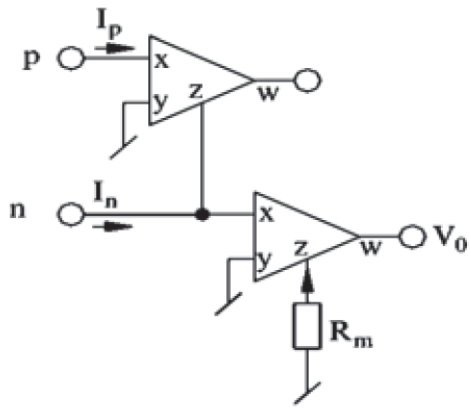

Figure 2. CFOA based implementation (adapted from 2004 Springer [9]).

VARIOUS IMPLEMENTATIONS OF OTRA USING BASIC BUILDING BLOCKS

A.Otra Using Opamp (Proposed Otra-i)

An operational amplifier (OPAMP) is a device whose output voltage is the multiplication of its internal gain and differential voltage applied at its input terminals. Output voltage of OPAMP is given as [10]:

$$V_o = R_m\left(\mathrm{I_p} - \mathrm{I_n}\right) \tag{2}$$

where, A is the open loop gain of OPAMP.

Various OPAMP ICs like LM741, CA3130, LM339, LM258 etc. are commercially available. Since, open loop gain of OPAMP is very high, for linear applications it has to be used in negative feedback mode. An implementation of OTRA using OPAMPs has been developed (proposed OTRA-I) and is shown in Figure 3.

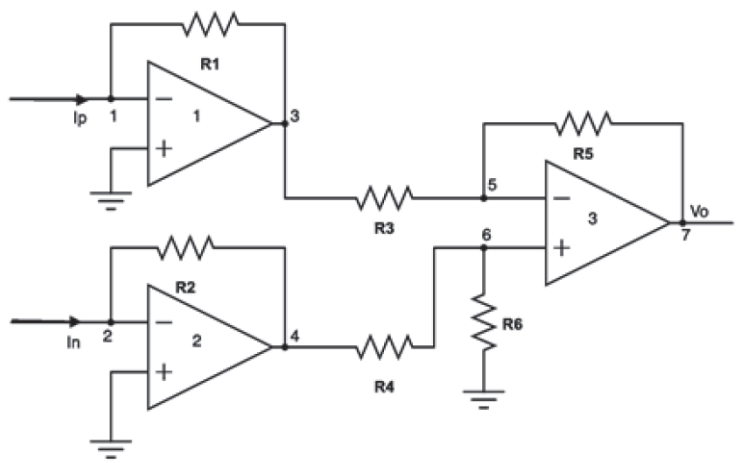

Figure 3. Proposed implementation of OTRA using OPAMP (proposed OTRA-I).

In this circuit, OPAMPs 1 and 2 acts as current to voltage converter. OPAMP 3 along with resistors R3, R4, R5 and R6 acts as differential amplifier. The OPAMPs used in the design have negative feedback, thus ensuring virtual short at their input terminals. This confirms virtual ground at the two input terminals of proposed OTRA and is expressed as:

$$V_o = R_m\left(\mathrm{I_p} - \mathrm{I_n}\right) \tag{3}$$

Applying KCL at different nodes of the proposed design, output voltage (V7) can be derived as:

$$\mathrm{V_0} = (I_p \times \mathrm{R_1})\left(\frac{\mathrm{R_5}}{\mathrm{R_3}}\right) - (I_n \times R_2)\left(\frac{\mathrm{R_6}}{\mathrm{R_4}+\mathrm{R_6}}\right)\left(\frac{\mathrm{R_3}+\mathrm{R_5}}{\mathrm{R_3}}\right) \tag{4}$$

In case, R1 is kept equal to R2, R3 is kept equal to R4 and R5 is kept equal to R6, Eq. (4) can be simplified to:

$$\mathrm{V_0} = \frac{\mathrm{R_1}\times R_5}{\mathrm{R_3}}\left(\mathrm{I_p} - \mathrm{I_n}\right) \tag{5}$$

Comparing Eq. (5) with Eq. (1), it can be analysed that:

$$V_o = R_m\left(\mathrm{I_p} - \mathrm{I_n}\right) \tag{6}$$

where, Rm = $\frac{\mathrm{R_1}\times\mathrm{R_5}}{\mathrm{R_3}}$, represents the transresistance gain of the implemented OTRA (proposed OTRA-I).

From Figure 3, input resistance of proposed OTRA (Rin), at two input terminals is given as:

$$R_{in,p(n)} = \frac{V_{p(n)}}{I_{p(n)}} \tag{7}$$

here, $R_{in,p}$ refers to input resistance at p terminal an $R_{in,p}$ refers to input resistance at n terminal. From Eqs. (3) and (7), it can be observed that $R_{in,p}(n) \approx 0$.Output impedance (R_{out}), of the implemented OTRA, in design of Figure 3 can be derived as:

$$R_{out} \approx R_{out(opamp3)} = Very\ low \tag{8}$$

From Eqs. (3) to (8) it can be analysed that the proposed design implements a near ideal OTRA using OPAMPs, with the constraint that transresistance gain (Rm) of the implemented OTRA is dependent on resistive ratio $\left(\frac{R_1 \times R_5}{R_3}\right)$ Thus to achieve high values of Rm, high values of R1 and R5 have to be chosen.

B.Otra Using Operational Transconductanceamplifier (Proposed Otra-ii)

Operational transconductance amplifier (OTA) is a voltage controlled current source that provides current proportional to the difference of voltages applied at its input terminals. The main advantage of OTA lies in the fact that its transconductance can be controlled through a biasing current. OTA has high input impedance and can be used with and without negative feedback [2]. IC of OTA (CA3080) is not very costly and is easily available in laboratories

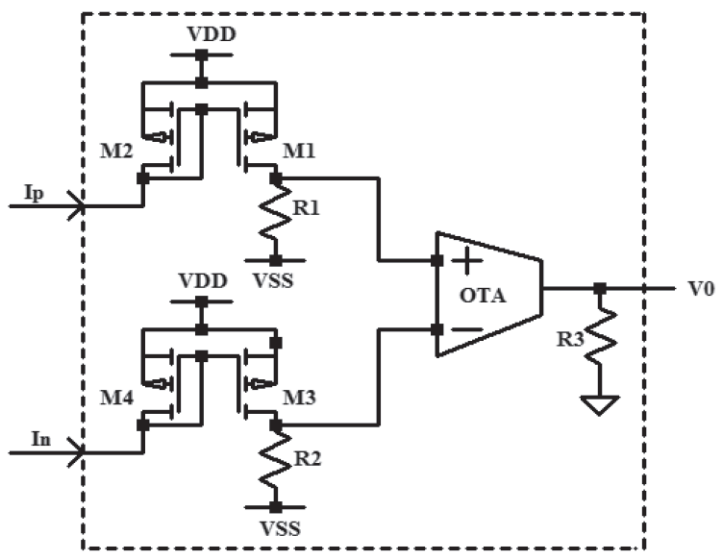

Figure 4. Proposed implementation of OTRA using OTA (proposed OTRA-II).

Output current of OTA, in terms of its input voltages, is given as:

$$I_{out} = Gm\ (V_{in+} - V_{in-}) \tag{9}$$

here, G_m is the transcoductance of OTA and its high values can be easily obtained with ICs available in market. CA3080 offers G_m in the range of 6-13mS. It can be varied directly by changing the device biasing current (I_B).

Proposed implementation of OTRA (proposed OTRA-II) using OTA is shown in Figure 4. In this circuit, to achieve low impedance at input terminals of OTRA, current mirrors have been used. Two current mirrors (one at each input terminal) have been implemented using MOSFETs M1-M4 and resistors R1 and R2. These current

mirrors not only provide the required low input resistance but also convert the input currents into voltage form, essential for OTA. To convert output current of OTA to voltage a resistor (R3) is used in the circuit. Small value of R3 will ensure small output resistance of the device.
Analysis of the circuit shown in Figure 4, shows that output voltage obtained from the proposed OTRA-II can be given as:

$$V_0 = (I_p R_2 - I_n R_1) \times (G_m \times R_3) \quad (10)$$

here, Gm is the transconductance of OTA used in the design.
In Eq. (10), if R_1 is taken equal to R_2 then this equation reduces to:

$$V_0 = (I_p - I_n) \times R_1 \times (G_m \times R_3) \quad (11)$$

Comparing Eq. (11) with Eq. (1), it can be analyzed that:

$$V_o = R_m (I_p - I_n) \quad (12)$$

where, $R_m = R_1 \times G_m \times R_3$, represents the transresistance gain of the implemented OTRA.

In Figure 4, diode connected MOSFETs M2 and M4 produces a nearly constant voltage at the two input terminals of proposed OTRA-II. To obtain virtual ground at these input terminals, the drain voltages of MOSFETs M2 and M4 have to be fixed at 0V. This can be done by adjusting V_{DD} suitably. It has been empirically calculated that in the proposed design if V_{DD} is kept equal to 1.3V, an approximately 0V is achieved at the input terminals. This can be expressed mathematically as:

$$V_p \cong V_n \cong 0 \quad (13)$$

Input resistance of proposed OTRA (Rin), at two input terminals is equal to the input resistance of current mirror at the respective terminals. This resistance is equal to few ohms and mathematically is given as:

$$R_{in,p(n)} = \frac{1}{g_{m4(2)}} \quad (14)$$

here, gm is transconductance of the corresponding MOSFET.

Output impedance (R_{out}), of the implemented OTRA in design of Figure 4 can be derived as:

$$R_{out} \approx R_{out(OTA)} \| R_3 \cong R_3 \quad (15)$$

From Eqs. (12) to (15) it can be analyzed that proposed OTRA-II implements a near ideal OTRA using OTA and some of the basic ICs available in lab. In this design, the transresistance gain (R_m) of the implemented OTRA depends directly on resistances used and transconductance of OTAs ($R_1 \times G_m \times R_3$). Thus, high values of R_m can be easily achieved by taking their large values. However in this design, R_1 and R_2 are fixed with V_{DD} to achieve virtual ground and low values of R_3 are preferred to obtain low value of output resistance. Thereby, transresistance of this OTRA is varied by changing Gm of OTA. In proposed OTRA-II, input resistance of implemented OTRA depends upon the input resistance of current mirror used at the input terminals. Moreover, to achieve virtual ground at the input terminals, value of V_{DD} has to be calculated through simulations or experimentally.

C. Otra Using Current Conveyor (Proposed Otra-iii)

In new era of current mode circuits, current conveyors are gaining a lot of popularity in designing of analog and mixed mode signal processing devices. Secon d generation current conveyor (CCII+) is most often used to design linear and non-linear circuits. It has 2 input terminals (x and y) and 1 output terminal (z).

Terminal characteristics of CCII+ are given as [2]:

$$i_y = 0; \qquad v_x = v_y; \qquad i_z = i_x \tag{16}$$

In CCII+, x and y terminal exhibit virtual short. No current flows in y terminal. Current at x is copied at high impedance output terminal (z).

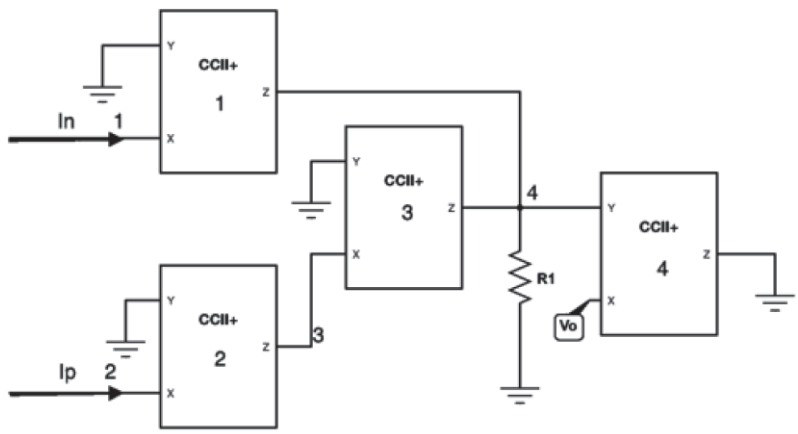

Figure 5. Proposed implementation of OTRA using CCII+ (proposed OTRA-III).

Figure 5 shows the proposed structure of OTRA using CCII+ (proposed OTRA-III). In this circuit, CCII+(2) is used to reverse the polarity of I_p current. Using port equations of CCII+, given by Eq. (16), V_0 of Figure 5 can be represented as:

$$V_O = (I_p - I_n) \times R_1 \tag{17}$$

Comparison with Eq. (1) gives that:

$$V_O = (I_p - I_n) \times R_m \tag{18}$$

here, Rm = R1, represents the transresistance of implemented OTRA.

From Figure 5, it can be observed that virtual ground is achieved at input terminals of the proposed OTRA. This is obtained as in CCII+, Vx = Vy, and in Figure 5, Vy(1,2) = 0. This is expressed as:

$$V_p \cong V_n \cong V_y(1\ ,\ 2) = 0 \tag{19}$$

Input resistance of proposed OTRA-III can be obtained by analysing the input resistance of CCII+ at x terminal and can be given as:

$$R_{in,p(n)} = R_{in,x(1,2)} \cong \text{Very small} \tag{20}$$

Output impedance (Rout), of proposed OTRA-III shown in design of Figure 5 can be derived as:

$$R_{out} = R_{in,x(4)} = \text{Very low} \quad (21)$$

From Equations (17) to (21) it can be analyzed that proposed OTRA-III implements an OTRA, whose transresistance gain (R_m) is given by resistor R1, used to design the structure. To achieve high values of R_m, high value of this resistor has to be used. In this design, very low values of input and output resistances are obtained, as these resistances are equal to resistance looking from x terminal of CCII+. Furthermore, virtual ground is achieved in the design very conveniently, just by connecting the y terminals of CCII+(1) and CCII+(2) to ground. However in this design, implementation of OTRA by CCII+ requires 4 blocks of CCII+.

In the 3 proposed designs of OTRA, first one is based on OPAMP, OTRA-II is based on OTA and OTRA-III is based on CCII+. OPAMP being a cheap and easily available component, proposed OTRA-I is the easiest to implement in the lab. In this design, high values of Rm can be obtained by choosing small values of R3, without affecting the input or output resistances of the implemented OTRA. OTRA is a device that is preferred by circuit designers due to its high bandwidth and slew rate. However in proposed OTRA-I, implementation via OPAMP (a voltage mode component) degrades its bandwidth and slew rate parameters. All the designs proposed in this paper, majorly depend on the value of the resistances used in circuit, to change the transresistance gain of the implemented OTRA. The exception is proposed OTRA-II, in this design the gain can be altered by varying the biasing current and thereby G_m of the OTA used. This feature of OTRA-II design offers the flexibility of electronic tuning in the implemented OTRA. However in OTRA-II design, it is difficult to obtain virtual ground at input terminals and input resistance depends upon the g_m of the MOSFET used to implement the current mirror required at the input port. Proposed OTRA-III requires 4 CCII+ blocks for its designing. However, this design offers high values of bandwidth and slew rate. Furthermore, it provides virtual ground at input terminals and low resistance at input and output ports.

IMPLEMENTATION OF OTRA BASED OSCILLATOR USING VARIOUS PROPOSED DESIGNS

Oscillators are an important electronic device that plays a major role in designing of signal processing, measurement and telecommunications systems. It is also used a fundamental block in several electronic instruments and power conversion control circuits [11]. Typically in a wide array of circuit systems, oscillators are designed using OPAMPs and passive components. However, the finite gain bandwidth product of an op-amp decreases the oscillator circuit performance. To overcome this problem, oscillators based on OTRAs have been investigated in literature. One such oscillator is shown in Figure 6 [11].

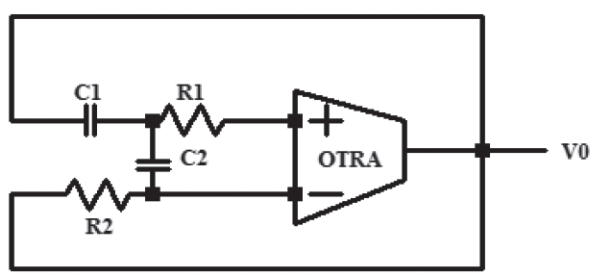

Figure 6. OTRA based oscillator

Considering OTRA to be ideal, nodal analysis of Figure 6 yields the characteristic equation of this OTRA based oscillator as:

$$S^2 C_1C_2 + S (G_1C_2 + G_1C_1 - G_2C_1) + G_1G_2 = 0 \quad (22)$$

From Eq. (22), the condition and frequency of oscillation (ω0) for the oscillator circuit shown in Figure 6 can be derived as:

$$\frac{G_2}{G_1} - 1 \geq \frac{C_2}{C_1} \tag{23}$$

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \tag{24}$$

This is a minimum RC oscillator and its condition of oscillation and frequency of oscillation are dependent on each other. This can be easily analyzed from Eqs. (23) and (24).

SIMULATION AND EXPERIMENTAL RESULTS

Simulation results for various proposed OTRA structures have been presented in this section. The simulations have been carried out in LTSPICE XVII using standard SPICE models of OPAMP (LM741), OTA (CA3080) and CCII+ (AD844). The values of different components that have been considered for performing simulations are tabulated in Table 1.

Dc Analysis

DC analysis has been carried out to observe the changes obtained in output voltage of proposed OTRAs with variations in differential input current (Ip-In). To verify the variations in Rm of the proposed structure with the parameters mentioned in section 3, this DC analysis has been plotted with different values of the defining parameter. Figure 7 shows these results for proposed OTRA-I.

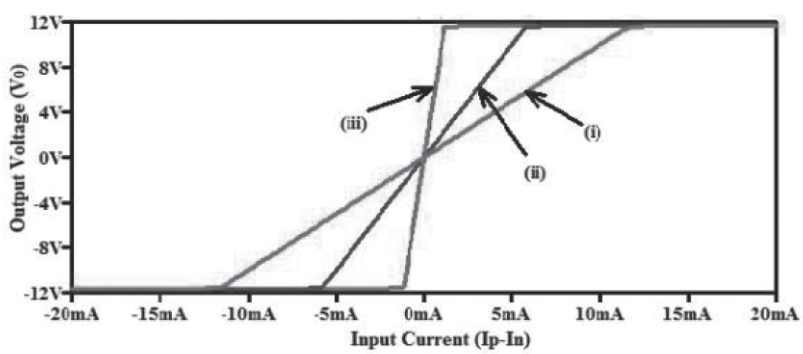

Figure 7. DC analysis for proposed OTRA-I for different values of R3 (i) R3 = 100Ω (ii) R3 = 50Ω (iii) R3 = 10Ω.

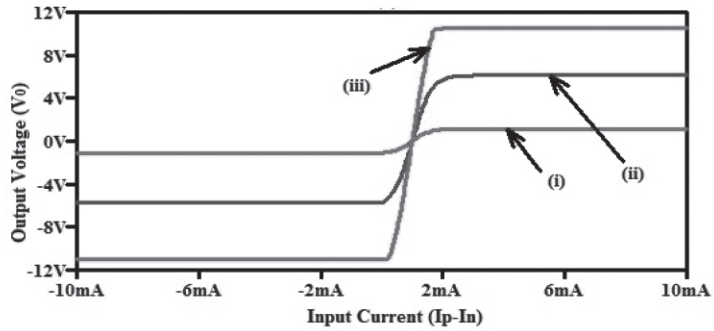

Figure 8. DC analysis for proposed OTRA-II for different values of IB (i) IB = 1mA (ii) IB = 5mA (iii) IB = 10mA

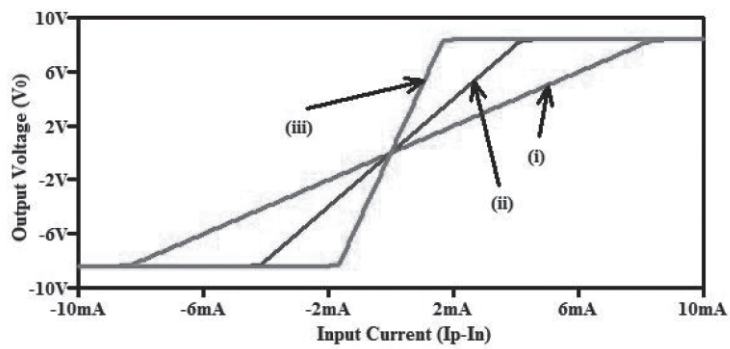

Figure 9. DC analysis for proposed OTRA-I for different values of R1 (i) R1 = 1KΩ (ii) R1 = 2KΩ (iii) R1 = 5KΩ.

In this figure, R3 of proposed OTRA-I is varied from 10Ω to 100Ω. It can be observed from the curves in the figure that as R3 decreases Rm of the proposed OTRA-I increases. This is due to the inverse relation of Rm on R3 in the OTRA structure. Variations obtained in Rm due to different values of R3 have been summarized in Table 2. The DC analysis results for proposed OTRA-II and proposed OTRA-III have been plotted in Figure 8 and Figure 9 respectively. These curves have been plotted by varying biasing current of OTA (IB) in proposed OTRA-II and by varying resistance R1 of proposed OTRA-III. The results show the direct dependency of proposed OTRAs transconductance on these parameters. From Figure 8 it can be seen that with increase in biasing current not only transconductance increases but operating range also increases linearly. All the simulation values obtained have been summarized in Table 2.

Table 1. Design parameters of the components used during simulations of proposed OTRA structures.

OTRA Design	**Parameter**	**Value**	**Designed oscillator parameters**	**Value**
Proposed OTRA -I	R1, R2, R4	100Ω	R1	30KΩ
	R3	50Ω	R2	10KΩ
	R5, R6	1kΩ	C1, C2	1uF
Proposed OTRA -II	R1, R2	100Ω	R1	200Ω
	R3	1kΩ	R2	100Ω
			C1, C2	100nF
Proposed OTRA-III	R1	2kΩ	R1	300Ω
			R2	100Ω
			C1, C2	500pF

Table 2. Simulation results for different proposed OTRA structures.

	Proposed OTRA -I		**Proposed OTRA -II**		**Proposed OTRA -II**	
Transresistance (Rm)	R3= 100Ω	0.999KΩ	I_B = 1mA	1.93KΩ	R1= 1KΩ	0.999KΩ
	R3 = 50Ω	1.99KΩ	I_B = 5mA	6.18KΩ	R1=2KΩ	1.99KΩ
	R3=10Ω	9.99KΩ	I_B= 10mA	14.81KΩ	R1=5KΩ	4.985KΩ
Rm (dB)	66.02dB		79.69dB		59.99dB	
Rin	< 1Ω		22.98Ω		496.23Ω	
Rout	1KΩ		0.99KΩ		0.05KΩ	
BW	44.6KHz		5.18MHz		14.46MHz	
SR^{+*}	0.475V/µs		127.42V/µs		474.62V/µs	
SR^{-*}	0.475V/µs		134.8V/µs		452.34V/µs	
Oscillation Frequency	73.83 KHz		2MHz		1.82MHz	

*To calculate SR a load capacitance (CL) of 10pf has been used.

Ac Analysis

In this subsection, frequency behaviour of different OTRA structures has been observed and described in detail. Figure 10 plots this response for all the three proposed OTRA configurations. From this figure it can be analyzed that gain of OTRA-II (designed using OTA) is maximum while bandwidth of OTRA-III (designed using CCII+) is maximum. Moreover, it is observed that the bandwidth of OTRA-I, based on OPAMP is minimum. This is expected behaviour of a voltage mode device. The different values obtained from this response have been summarized in Table 2.

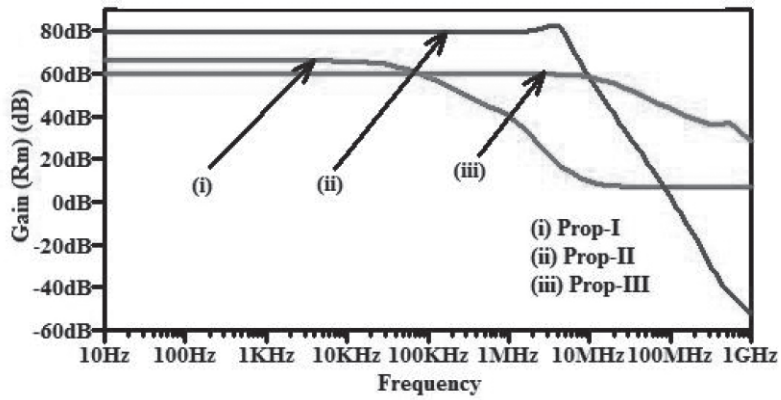

Figure 10. Frequency responses for (i) proposed OTRA-I (ii) proposed OTRA-II (iii)proposed OTRA-III.

Variation of input resistance (Rin) and output resistance (Rout) for these proposed devices has been analyzed and shown in Figure 11 and Figure 12 respectively. These figures show that Rin is minimum for OTRA-I and Rout for OTRA-III is minimum. Their respective simulated values have been mentioned in Table 2.

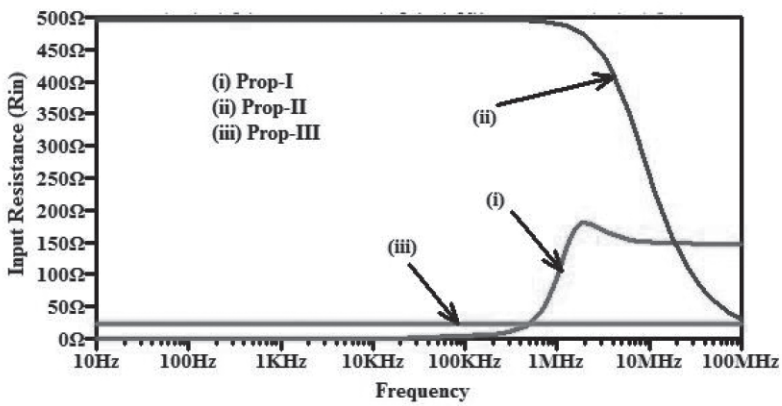

Figure 11. Variation of input resistance (Rin) with frequency for (i) proposed OTRA-I (ii) proposed OTRA-II (iii) proposed OTRA-III.

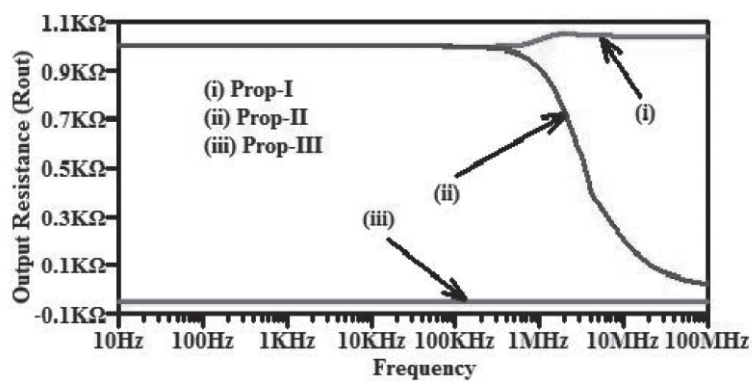

Figure 12. Variation of output resistance (Rout) with frequency for (i) proposed OTRA-I (ii) proposed OTRA-II (iii) proposed OTRA-III.

Transient Analysis

To observe the behavior of proposed OTRAs with a square pulse, their transient responses have been studied. In case of proposed OTRA-I, a square pulse of 5 KHz frequency and 10mA amplitude is applied at input terminal and for rest OTRAs the pulse applied has been of 500KHz. The response obtained in these configurations has been shown in Figure 13.

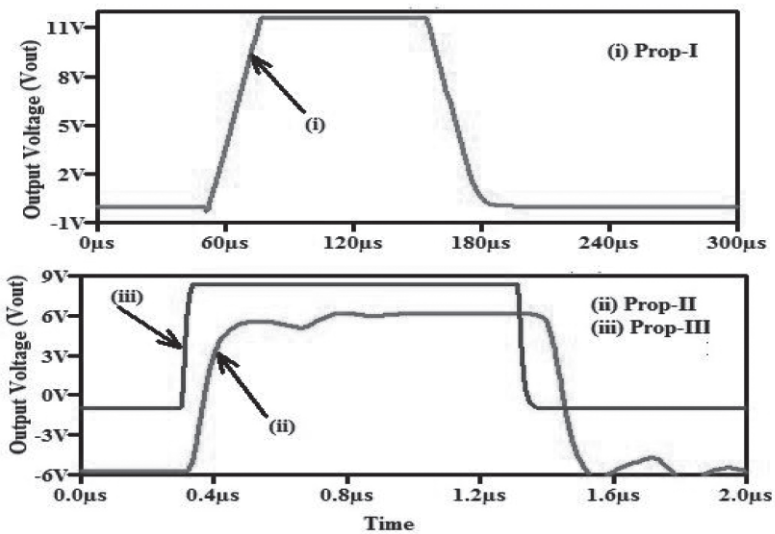

Figure 13. Transient response of proposed OTRAs with application of a square pulse (i) proposed OTRA-I (ii) proposed OTRA-II (iii) proposed OTRA-III.

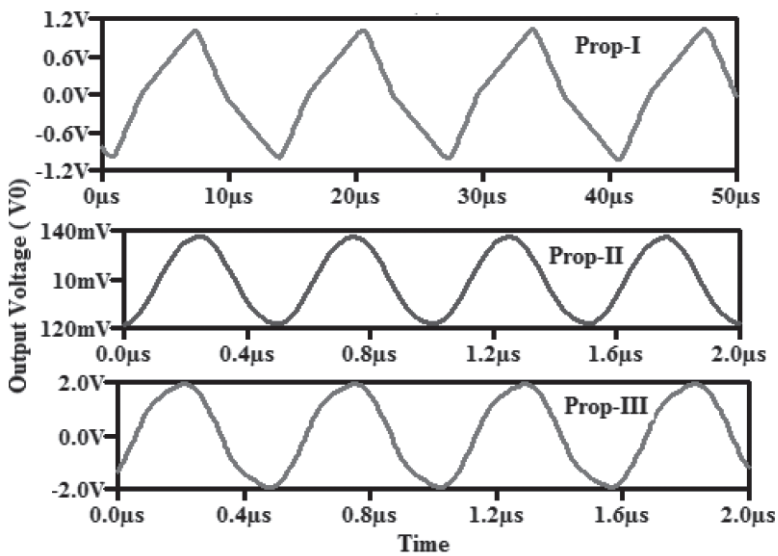

Figure 14. Response obtained from oscillators designed using (i) proposed OTRA-I (ii) proposed OTRA-II (iii) proposed OTRA-III

Implemented Oscillator Response

Oscillator shown in Figure 6 has been implemented using various OTRA proposed structures. The values of parameters used for designing these oscillators have been tabulated in Table 1. These parameters have been chosen considering the condition given in Eq. (23). The components used to design oscillator based on OTRA-I are the largest and those for designing oscillator based on OTRA-II are the smallest. This is due to the difference in their bandwidth and frequency of oscillation being inversely related to these parameter values (as per Eq. (24)). The response obtained from oscillators designed using various proposed OTRAs has been shown in Figure 14. The oscillation frequencies produced by them are mentioned in Table 2

EXPERIMENTAL RESULTS.

The prototypes of the oscillators discussed above have been implemented on bread board using LM741 IC for proposed OTRA-I, CA3080 IC for proposed OTRA-II and AD844 IC for proposed OTRA-III. Similar parameters as mentioned in Table 1, have been used to obtain oscillating output at bread board, with the difference that R1 has been taken as variable resistor. This potentiometer helps in tuning of R1 to achieve required gain of the circuit for obtaining sustained oscillations. The photograph of the oscillation outputs received from these circuits have been shown in Figure 15 for all the 3 circuits.

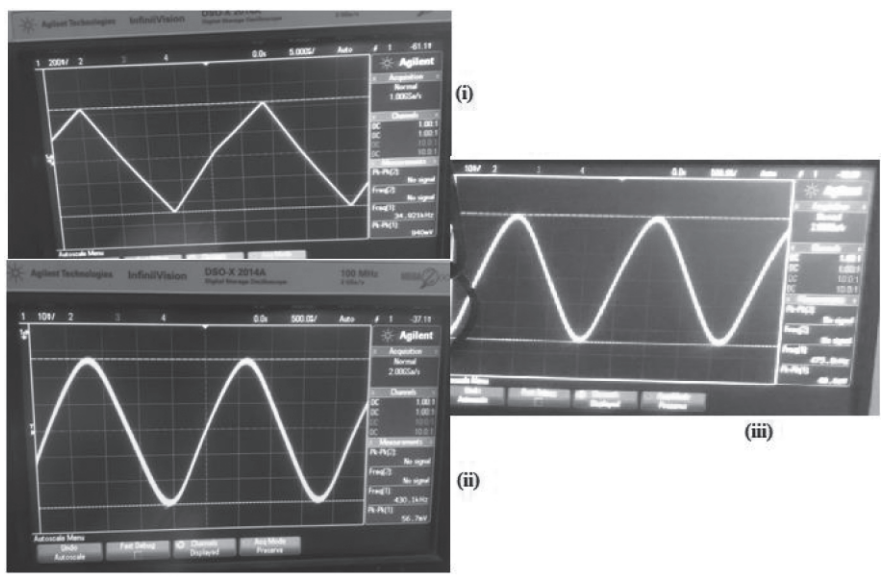

Figure15. Photograph of the oscillation outputs received from experimental circuits of oscillator designed using (i) proposed OTRA-I (ii) proposed OTRA-II (iii) proposed OTRA-III
These oscillator outputs confirm the usability of the designed circuits in practical environment

CONCLUSION

This paper presents 3 alternative ways of implementing OTRA using discrete circuit elements. In this work, OTRA has been implemented using OPAMP, OTA and Current Conveyor. These blocks have been chosen for the work in the paper as commercial ICs of these components are easily available. The designed OTRA structures have been simulated using LTSPICE and implemented on bread board using the ICs available in the lab. Further, oscillator circuit has been designed using these proposed OTRA structures and analyzed for proper functioning via simulations and practically using bread board to confirm the usability of the proposed designs in practical environment. The simulation results confirm to the voltage and current behavior described by the mathematical equations of OTRA. It has been observed that proposed OTRA-I, is the simplest to design but it operates with lower bandwidth and slew rate.In proposed OTRA-II the transresistance gain can be tuned electronically by varying the biasing current and OTRA-III offers the highest values of bandwidth and slew rate. The experimental results of designed oscillators from the proposed OTRA structures validate their usability in practical environment.

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