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Comparative Analysis in Terms of Power and Delay of the Different Sense Amplifier Topologies

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ABSTRACT

To read the data from the memory in each of the devices is crucial. In the modern-day VLSI, world need high-speed devices to satisfy the demand for application such as the Internet of Things (IoT) and System on Chip (Soc). We have implemented the different types of existing sense amplifiers to investigate the working and application point of view. Every sense amplifier has its own advantage. Each of the sense amplifiers is focusing basically on the charging and discharging of Bit Line (BL), Bit Line Bar (BLB) in case of Voltage sense and Data Line (DL), Data Line Bar (DLB) in case of current sense. The waveform of the Voltage sense and current sense clearly shown. Performance comparison based on Sensing Delay, Power, and Supply variation at UMC 65nm CMOS technology node using CADENCE Virtuoso tool.

Keywords: Current sense; Voltagesense; Memory cell; CMOS; Hybrid sense; Bit lines; Pre-charge; amplifier.

INTRODUCTION

A memory chip, which is one of the most important components of a very large scale integration (VLSI) system is a matrix of locations (Evert Seevinck, van Beers, & Ontrop, 1991). Each of which is able to store one bit. Memory chips occupy the enormous area on a system on achip (SoC) (E Seevinck, 1990). In spite of low power, high-performance memory is also a major concern (Anh-Tuan, Zhi-Hui, Kiat-Seng, & Briefs, 2008). Sense Amplifier is an important circuit which senses and amplifies the small voltage signal from bit lines to an appropriate logic level "1"(Kristovski, Pogrebnoy, Analog, & Processing, 2000). Sense amplifiers can be categorized into voltage mode and current Mode sense amplifiers (Zhang, Wang, Zhu, & Zhang, 2017). Voltage sense amplifiers are connected to bit lines of the SRAM cell columns and hence depend on bit lines capacitance (Patel, Neale, Wright, Sachdev, & Papers, 2019). As the memory device's density increases, the inescapable parasitic capacitance also increases (Liu, Cai, Yuan, Hei, & Briefs, 2016). This originates from the constriction in accomplishing a higher sensing speed need. Larger the bit lines capacitance, larger the time constant RC which leads to larger delay (Arora, Gundu, & Hashmi, 2016). Current mode sense amplifiers give assurance to this bottleneck (Kawahara et al., 1992). Bit lines are connected to inputs of current sense amplifiers and discharging of bit lines causes decreases in current which helps in determining the output voltage level (Abu-Rahma et al., 2011). Current sense amplifiers are widely used to reduce power and sensing delay as it amplifies the small differential signal from Bit lines and Data line Bar (DLB) quickly (Hemaprabha & Vivek, 2015; Kumar et al., 2011; Rabaey, Chandrakasan, & Nikolić, 2003) . Bit lines connected to inputs of current sense amplifiers cause' extremely high input impedance at the input, leads decoupling of Bit lines from output (Dutta & Mondal, 2020; Sinangil & Chandrakasan, 2014; Toli{\'c}, 2019; Weste & Harris, 2015) . Various voltage and current sense amplifiers are reported so for having low power, high-speed merits. In this work, we broadly studied the operation of various existing voltage, current and hybrid sense amplifiers, and analysed their weakness (Chotten & Richa, 2019; Xie et al., 2019; Yoon et al., 2020) . Figure 1 shows the basic architecture of a column of the memory array. In this paper we have discussed different topologies of the senseamplifier designs having different delays and power consumption.

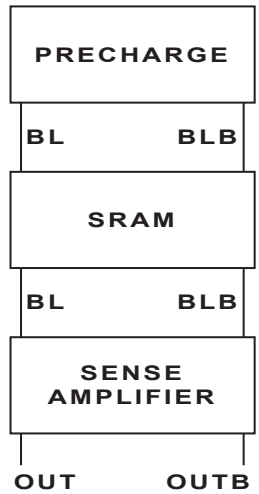

Figure 1. Essential Blocks Need to Sense Data Stored in Cell

This paper contributed the following points.
1) Description of different sense amplifier topologies.
2) Delay Comparison of different sense amplifier.
3) Power Consumption comparison of Different sense amplifier topologies.
4) Variation of Delay and Power Consumption with Supply Voltage

All the results were obtained in a 65nm UMC CMOS technology at room temperature using CADENCE VIRTUOSO for 1 volt supply voltage. The flow of paper is organized as follows: In the earlier part of the introduction the basic functions of the conventional sensing concept are explained, then the later part consists of the description of both topologies. In section II contributes to the state of the art of existing sense amplifiers and there CMOS circuit's functions are described. The Working of CMOS circuit diagram of the basic sense operation and circuit diagram of both possible cases of the sense amplifier is described in section III. Section IV describes the simulated results of the different circuit and output waveform at 65nm CMOS UMC technology node. Finally, in section V the conclusion is given.

EXISTING CIRCUITS OF SENSE AMPLIFIER

Voltage Latch Sense Amplifier

Figure 2 shows conventional Voltage latch sense amplifier (VLSA) circuit which senses the small voltage difference between BL and BL bar via P3 and P4 transistors by keeping sense enable (Sae) signal at logic Low. When Sae is at logic High, P1, P2, N1, N2 forms a cross-coupled inverter that amplifies the small voltage difference on Q and QB. Transistor N3 provides a discharging path to either of Q or QB leads to a full CMOS logic level at output OUT and OUTB. Bit and Bit bar lines connected directly to VLSA, hence increase the parasitic capacitance. Increased parasitic capacitance leads to more delay as sense amplifier take more time to discharge this increased parasitic capacitance.

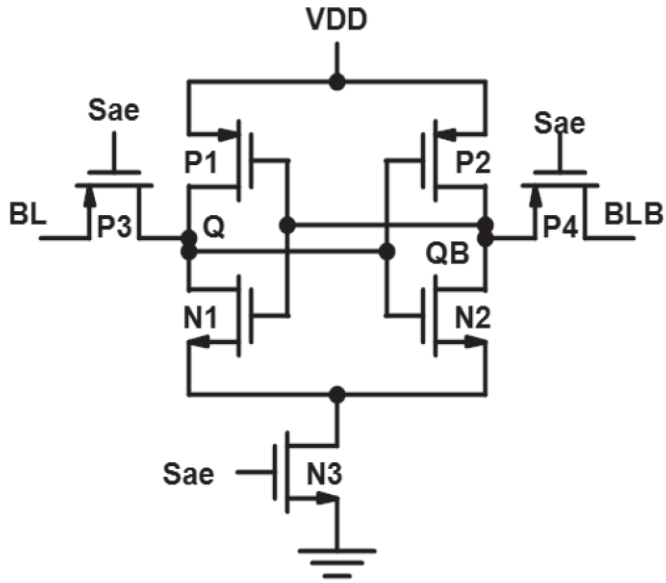

Figure 2. CMOS circuit of Voltage Latch Sense Amplifier [13]

Conventional Voltage Sense Amplifier

Figure 3 shows the conventional voltage sense amplifier which constructed using only 5 transistor and one inverter at the output. In this circuit gate of P1 and P2 are connected to the drain of N1 while the gate transistor N1 and N2 are driven by the Bi lines (I.e. BL and BLB).

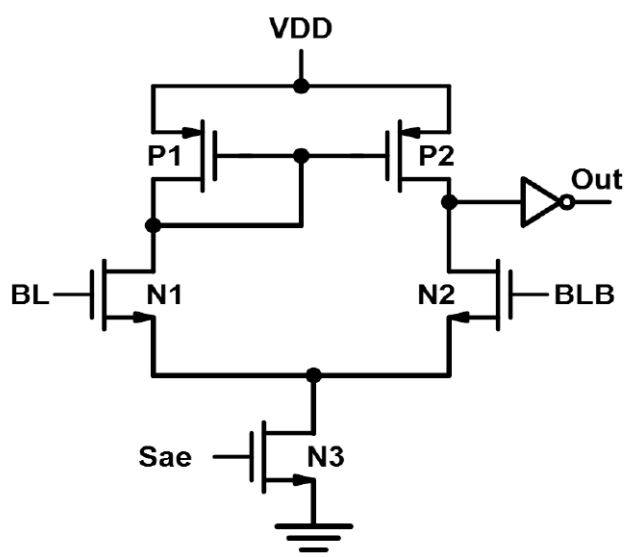

Figure 3. CMOS circuit of Voltage Sense Amplifier [1]

According to the Sae signal tail transistor make the decision weather ”1” or ”0” is stored in the cell.

Current Latch Sense Amplifier

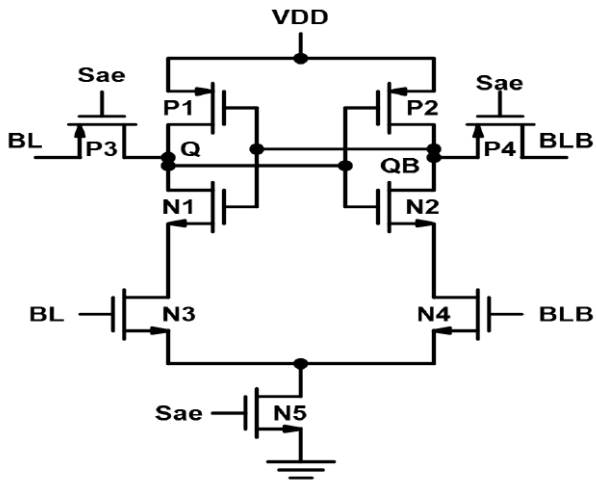

Figure 4. CMOS circuit of Current Latch Sense Amplifier [5]

Figure 4 shows the Current Latch Sense Amplifier consists of 9 transistors. In the circuit two extra transistors, N3 and N4 incorporated when compared with the Voltage Latch Sense amplifier. Gate of these transistors N3 and N4 are connected to BL and BLB respectively. According to the Sae signal tail transistor N5 take the decision what logic ”1” or ”0” is stored in the memory cell.

Conventional Current Sense Amplifier

Nowadays, several attempts at designing current-mode sense amplifiers have been published. Figure 5 shows the convention current sense amplifier proposed by Seevink in1990. This CSA consists of only four equal-sized PMOS transistors below the cell and connected between BL and BLB. In many cases it can fit in the column pitch, avoiding the need for column-select devices, thus again reducing propagation delay. The sensing delay is not affected by the BL capacitance since no differential capacitor discharging is needed to sense the cell data.

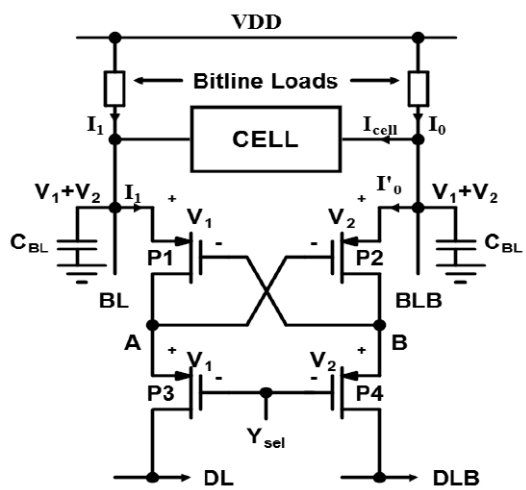

Figure 5. CMOS circuit of Current Sense Amplifier [2]

Hybrid Current Mode Sense Amplifier

Due to virtual short circuit VBL is not equal to VBL bar in practical cases. In deep sub-micron technology this effect becomes significant and causes I0 to be three times larger than I1. This will lead to less utilization.

$$\% \text{ utilization} = \Delta I / \text{Total Current} = (I1 - I0')/ (I0+I1)$$
$$\Delta I << I \text{ cell}.$$

More effective sense amplifiers are reported so far in order to achieve high speed and low power needs. Sense amplifier presented in Figure 6 consists of 4 PMOS transistors for pre-charging and holding of Bit lines. P3, P4 pre charges and P1, P2 holds the Bit lines at VDD, not source bit line currents. P1 and P2 are kept small-sized in order to make it not strong enough to keep Bit lines at VDD and hence during reading operation one of the Bit lines drops. P5 and P6 connect Bit lines to Data lines during the sense stage of sense Amplifier. P11 transistor is an equalization transistor. It helps to attain the same logic at the output and output bar before the Read cycle. During Read cycle column select (CS bar) signal, Sae, EQ bar and Read bar signal turns high. But P1 and P2 are still on to hold BL's and DL's at VDD. As EQ bar is at logic high leads to a cross-coupled configuration that senses small current difference of DL'S and give CMOS logic at the output. To check Read effectiveness % utilization is used

$$\% \text{ utilization} = \Delta I/ \text{Total current} = (\Delta I) / (I1+I0+I\text{discharge})$$
$$I \text{ cell} > I0, \quad I1 = \text{very large and } I \text{ discharge} = I \text{ cell} - I0.$$

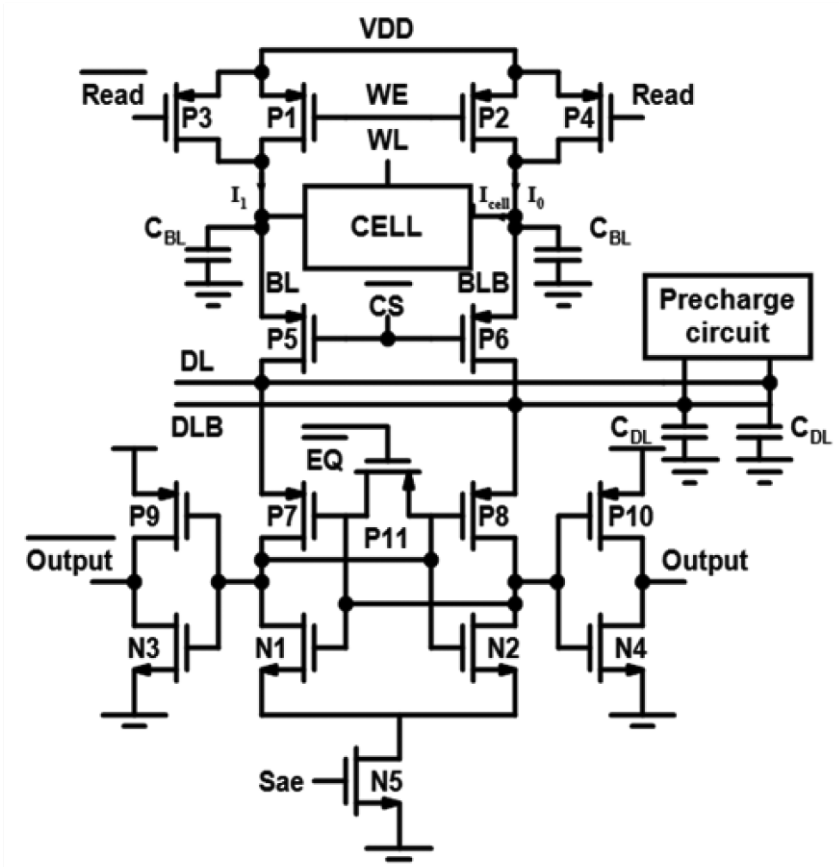

Figure 6. CMOS circuit of Current Mode Sense Amplifier [3]

Improved Hybrid Current Mode Sense Amplifier

In order to make Figure 6 circuit works at lower supply voltage, a modified circuit has been reported as shown in Figure 7. Resizing of transistors and adding two more transistors leads to a strong circuit that works at lower supply voltages. P11 and P12 transistors pre-charges node E and F to the same logic i.e. VDD when the Pull bar is at logic Low.

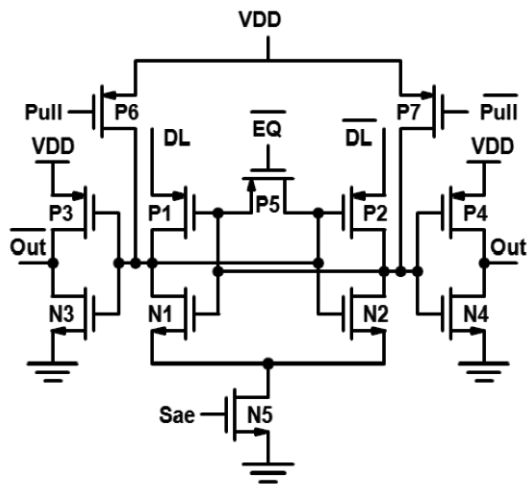

Figure 7. CMOS circuit of Improved Current Mode Sense Amplifier [3]

Hybrid Latch-Type Sense Amplifier

Figure 8 presents a recently reported Hybrid sense Amplifier (HYSA). In the pre charging phase of Sense Amplifier Sae is kept at logic Low causes pre charging of Q/QB and Z/ZB nodes with small voltage difference. In the second phase Sae is kept at logic high that turns off P3, P4, P5, P6 and turns on N3. Turning N3 on leads to amplify the small voltage difference at Q and QB through cross-coupled configuration (P1, P2, N1, and N2). Memory arrays consist of an array of Bit cells connected to bit lines and the word lines. High word line activates SRAM Memory Cell and stored bit in SRAM transfers to and from bit lines. Sense Amplifier senses the transferred bit from SRAM and amplifies it to a recognizable logic level. Bit lines are pre charged by pre-charging circuits. During pre-charging, pre-charge and WL should be at logic Low leads to logic High at Bit lines as shown in Figure 9. High at Word line activates SRAM leads to discharging of one of the Bit line capacitance as shown in Figure 9. Figure 9 clearly explain the step to retrieve data stored in SRAM cell, weather data”0” is stored or data”1” is stored.

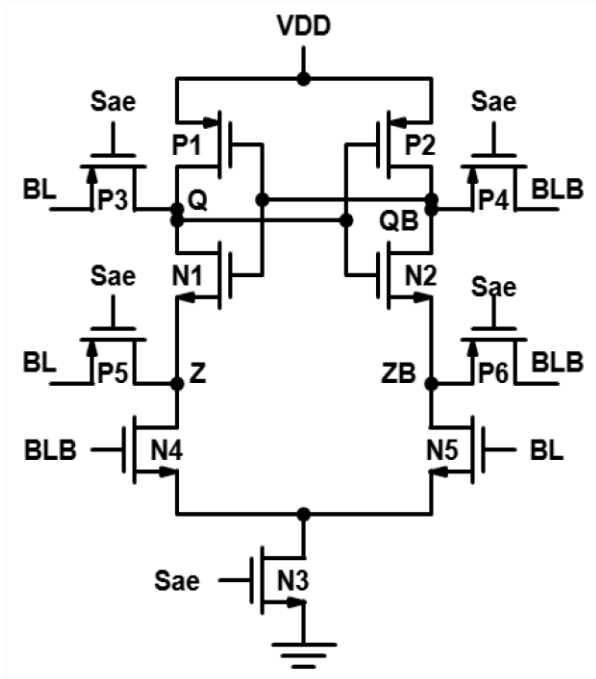

Figure 8. CMOS circuit of Improved Current Mode Sense Amplifier [6]

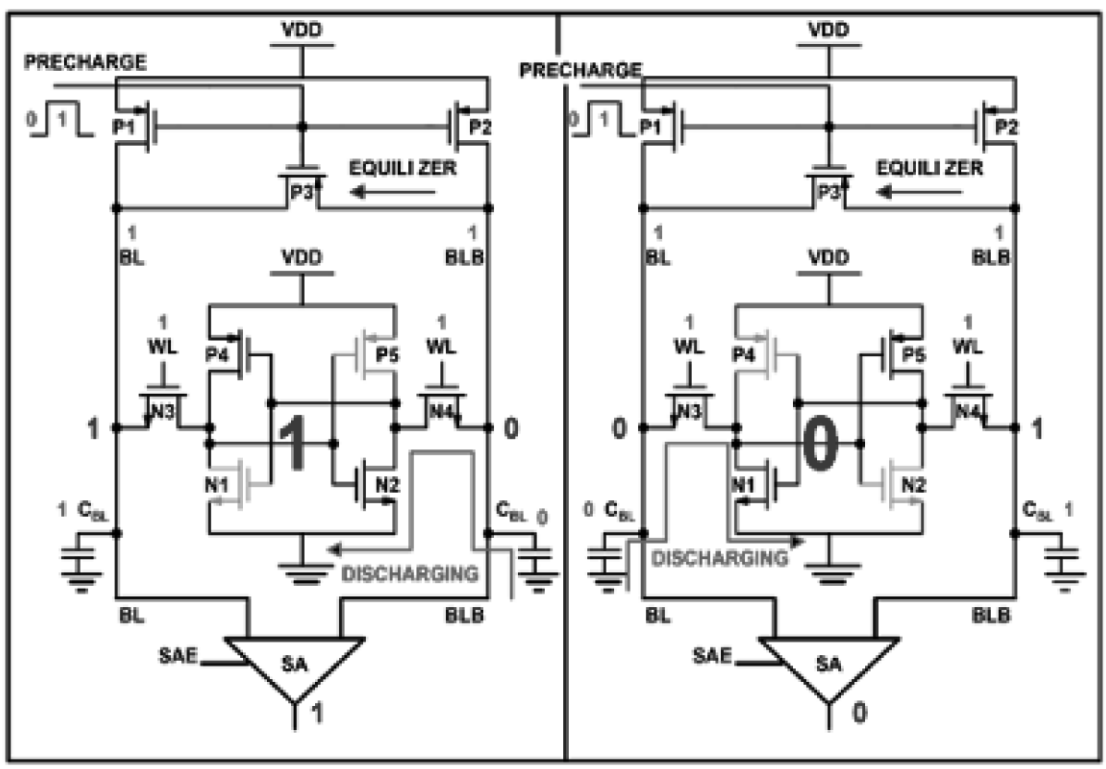

Figure 9. Process of reading "1" and "0" from the cell by Sense Amplifier.

EXPERIMENTAL RESULTS AND ANALYSIS

Figure 10 depicts the bit line and bit line bar condition when data ”0” was stored in the cell and it is read by the voltage sense amplifier. Here Bit line is discharging so we can say”0” was stored. Figure 11 shows waveform of the Current sense amplifier in which there are four signal are to be taken care BL, BLB, DL, and DLB. Where DL is Data Line and DLB is Data Line Bar. According to the condition of their lines out to be decided weather”0” was stored or”1” was stored.

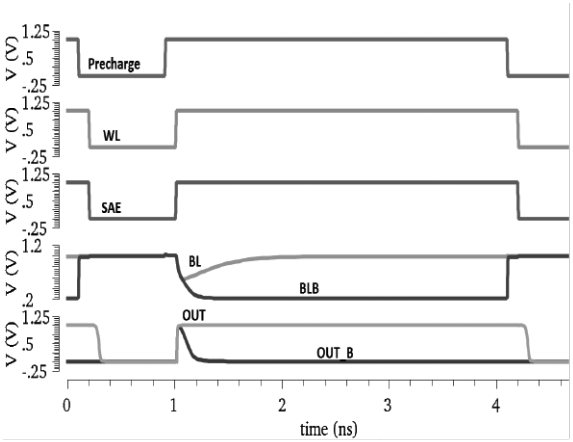

Figure 10. Output Waveform of the Voltage Sense Amplifier

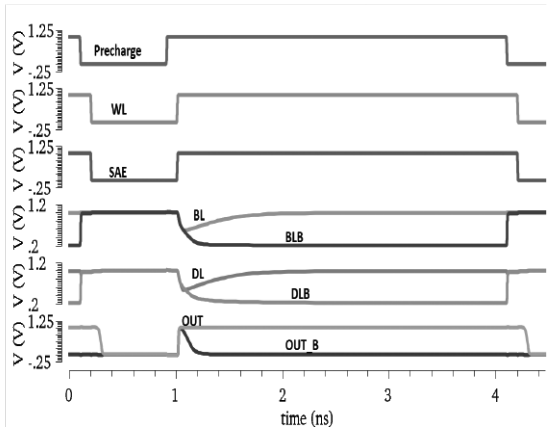

Figure 11. Output Waveform of the Current Sense Amplifier

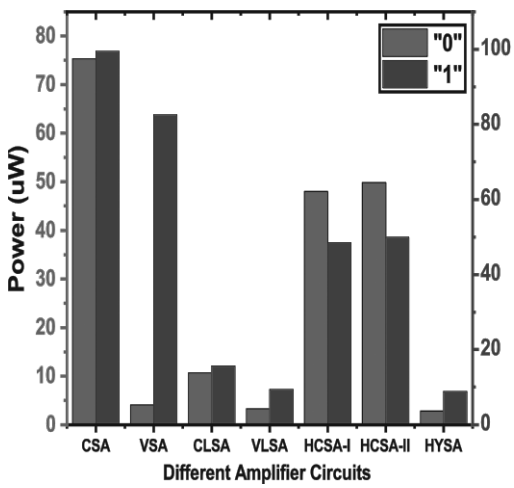

Figure 12. Power Plot of the Different Sense Amplifiers.

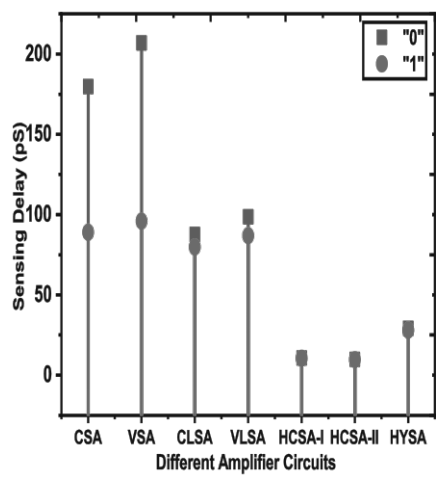

Figure 13. Delay Plot of the Different Sense amplifiers.

Figure 12 clearly shows the Power consumed by the different sense amplifiers in the data retrieving process. Bar chart showing both reading data”0” and reading data”1” while in both the cases power is different. There are two Y-axis is indicated one for ”1” and other for ”0” and X-axis show different sense amplifier topologies. Figure 13 shows the sensing Delay variation of the different sense amplifier topologies while reading the data stored in the cell. When read”1” is occur delay comes lesser than read”0”.

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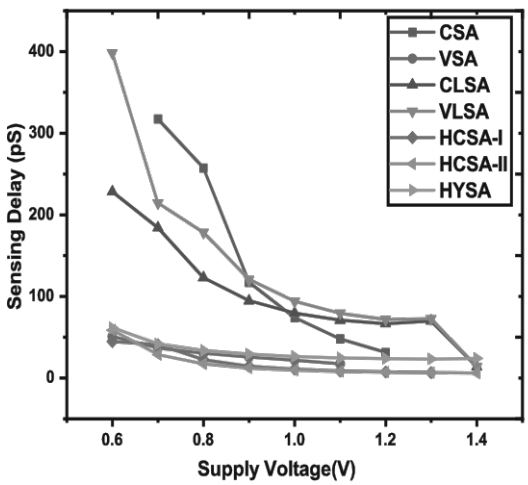

Figure 14. Supply vs. Delay Plot of the Different Sense Amplifier when reading 0

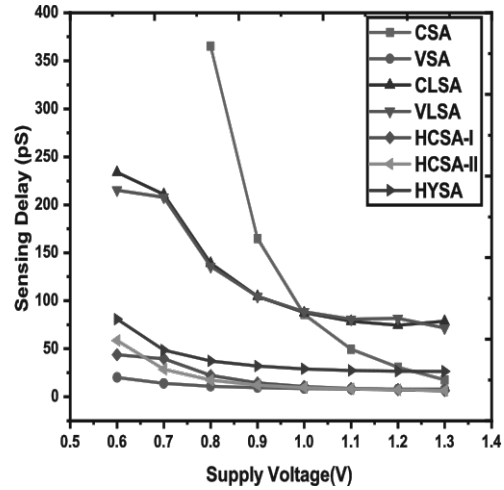

Figure 15. Supply vs. Delay Plot of the Different Sense Amplifier when reading 1

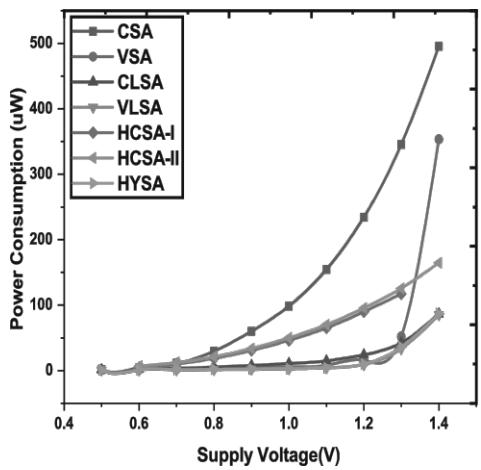

Figure 16. Supply vs. Power Plot of the Different Sense Amplifier when reading"0"

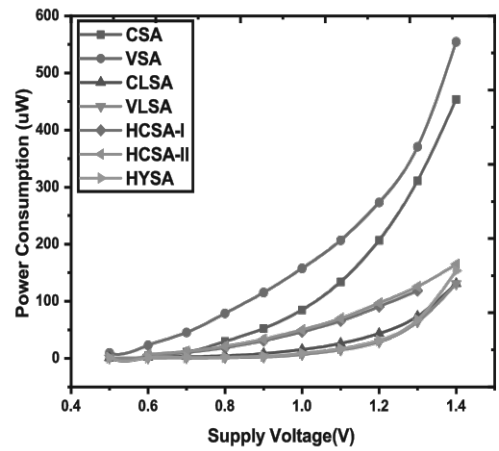

Figure 17. Supply vs. Power Plot of the Different Sense Amplifier when reading 1

We can see clearly in the Figure 13. Figure 14 shows the Variation of sensing delay of different sense amplifiers with respect to supply voltage. As we vary the supply voltage from 0.6 to 1.2, delay is decreasing while reading"0". Figure 15 shows the Variation of delay of different sense amplifiers with respect to supply voltage. As we vary the supply voltage from 0.8 to 1.2, delay is decreasing while reading"1".

Figure 16 shows the Variation of power consumed in different sense amplifiers with respect to supply voltage. As we vary the supply voltage from 0.6 to 1.4, power is increasing while reading"0".Figure 17 shows the Variation of power consumed in different sense amplifiers with respect to supply voltage. As we vary the supply voltage from 0.6 to 1.4, power is increasing while reading"1". Table 1 shows the size of the Load, Access, and Driver transistors used in the SRAM memory cell. Table 2 tabulates the numerous values of Power consumed and sensing delay the various sense amplifier topologies in different data condition "0" and "1".

Table 1. Size of SRAM Transistors

Load Transistors P1 & P2	W/L (nm) =100/60
Access Transistors N3 & N4	W/L (nm) =150/60
Driver Transistors N1 & N2	W/L (nm) =180/60

Table. Delay and Power of Different Sense Amplifiers

	Delay(pS)		**Power(μW)**		**PDP(fJ)**	
Read Data	**"0"**	**"1"**	**"0"**	**"1"**	**"0"**	**"1"**
CSA[2]	179.8	88.92	75.29	99.4	13.53	8.83
VSA[1]	207	95.92	4.03	82.5	0.83	7.91
CLSA[5]	87.63	79.8	10.68	15.6	0.93	1.24
VLSA[13]	98.76	86.86	3.27	9.4	0.32	0.81
HCSA-I[3]	10.77	10.57	48.01	48.42	0.517	0.511
HCSA-II[3]	9.82	9.63	49.81	49.91	0.49	0.48
HYSA[6]	29.09	28.02	2.77	8.82	0.08	0.24

CONCLUSION

The VSA, CSA, VLSA, CLSA, HCSA-I, HCSA-II, and HYSA topologies implemented and investigated. Sensing delay and power consumed is found out and compared. Effect of supply on sensing delay and power consumption also discussed in both of the data reading conditions. Result shows current sense amplifier has lower sensing delay than the Voltage Sense Amplifier. Power consumption in current sense amplifier is higher than the Voltage sense amplifier. PDP of the each sense amplifier has been calculated for better understanding of the power consumption. This paper successfully addressed the all four observation taken initially.

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