THD optimization in 15-level asymmetric reduced switch count multilevel PV inverter using optimization algorithms

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ABSTRACT

Philosophers and industries have focused on designing multilevel inverters, which use significantly fewer power switches and dc sources to achieve high power, low switching, and less harmonic output distortion for medium voltage applications. Even so, these multilevel inverters have some downsides like the use of many electronic components, electromagnetic interference (EMI), bulky driver circuit complexity, significant reverse recovery times, and voltage balancing issues. A modern asymmetrical multilevel inverter with fewer switches and drivers than standard topology is introduced in this article. The powerful analogy addresses traditional inverter topologies of a similar structure. The proposed MLI is relatively simple and easy to extend for many output levels. The proposed design of MLI is implemented for 15 level output with precise and high-quality near sinusoidal waveform using seven switches, three dc sources and three diodes and hence the volume, cost and driver circuit complexity is considerably reduced. The novelty in the proposed topology is that reduced ON state semiconductor switching devices. The output of the MLI is evaluated with the parameter of total harmonic distortion (THD). To minimize the THD, optimization algorithms such as GA, PSO, WOA and HHA were implemented at fundamental switching PWM control method. The comparative analysis of these algorithms on proposed inverter performance is integral for this research. The efficacy of this topology enhances the integration of renewable energy sources.

Keywords: THD, Asymmetric Inverter, MLI, Reduced Switch Inverter, Optimization, PV Inverter

I. INTRODUCTION

In the new industrial and academic research paradigm, multilevel inverters have evolved dramatically because of their ability to produce high-quality output at reduced costs. Philosophers have focused widely on reducing inverter costs by using near-total components. The main goal of a multilevel topology of the inverter is to incorporate the harmonic profile into the IEEE519 standard, which eliminates the need for heavy filters (McGrath BP., 2002**)**. Multiple targets such as minimum THD, low dv/dt stress, lower common-mode voltages are available to guarantee the use of electric motors. Electromagnetic interference (EMI) problems are less frequent on the multilevel inverter than conventional two and 3-level inverters. In general, researchers aimed at increasing the basic units in series or cascading of the basic unit to get more output voltage levels to improve the inverter's efficiency at lower THD. The inverter perceives its usefulness in PV fed UPS, propulsion systems, integration of green energy sources, aeroplanes, battery-powered vehicles etc. A simple control strategy is necessary to reduce the complexity of multilevel inverters. Therefore, the investigators focused on efficient topology architecture and modulation (Rodriguez J., 2002).

Diode clamping, capacitor clamping, and cascading-bridge inverters were standard multilevel topologies of inverters (M. N. Abdul Kadir., 2011). These topologies are widespread in renewable energy integration and electric hybrid vehicle (EHV) industries (Md. Rabiul Islam., 2019). Along with controlled switches, diode clamped MLIs require many diodes whose reverse recovery times increase during the transition period; similarly, the flying capacitor MLIs utilize several static capacitors whose voltage balance is a critical issue (ùCHIOP Adrian., 2012). The topology of the cascaded H-bridge (CHB) inverter is free from reverse recovery diodes and static capacitors. Therefore, the efficiency of CHB is more than diode clamped and capacitor clamped inverters. For typical high-power loads such as conveyors, pumping, fans, and milling, diode-clamped (DC) multilevel converters are used. The multilevel flying capacitor (FC) inverters are used on medium voltage drives and high-frequency bandwidth systems. Whereas cascaded H-bridge inverters were used applications such as reactive power control in the grid, renewable energy integration, active filters, UPS, magnetic resonance imaging, etc. Moreover, hybrid and electric trains for multilevel motor drives are a growing application (Malinowski Mariusz., 2011). The CHB inverter utilizes a simple, extremely efficient dynamic control scheme and needs fewer semiconductor switches to produce the desired output voltage level. The literature reports two types of operations for CHB inverters, namely symmetrical and asymmetrical configurations (Alishah R.S., 2014). The symmetric inverter has similar dc voltage sources, whereas the asymmetric inverter has unequal dc voltage sources. Asymmetrical multilevel inverters with reduced switch count can produce more levels of output. Two methods for determining the magnitude of dc voltage inputs are used in CHB asymmetric

multilevel inverter, binary and trinary configurations. Compared to binary structure, by merely varying the magnitude of dc sources, the Trinary configuration will produce more levels from the same power switches and sources (Nagaraj Vinoth Kumar., 2017). The key factors deciding the price and complexity of the MLI are simple to control methods, reduced switches, dc sources, and control circuits.

In recent years, various configurations of symmetric and asymmetric multilevel inverters were explored with a reduced number of switches. Different symmetrically structured topologies were presented (Vanaja, D.S, 2021). Two types of algorithms were described for symmetric and asymmetric inverter topologies (Farhadi Kangarlu, M., 2012). However, this configuration uses bi-directional switches, which is the main drawback of this system, so many IGBTs are required. A basic cell structure for symmetrical topology was introduced (Babaei, E., 2015), including three dc sources and five switches for seven levels. The basic cell is cascaded to achieve higher output levels, and an H-bridge is connected to this output in cascade for polarity reversal. More dc sources, switches, power diodes, transistors and control circuits are the key drawback in the symmetrical configuration. These complications multiply under the topologies under which two-way switches in the voltage perspective are used (Ebrahimi, J., 2012; Farhadi Kangarlu, M., 2012). Various reduced switch topologies have been reported in (Alishah R.S., 2014; Ebrahimi, J., 2012; Kamaldeep Boora1., 2017; Madan Kumar Das., 2017) to reach high levels of the peak voltage. A basic cell structure with bidirectional switches is presented in (Alishah, R. S., 2015), and this basic cell is cascaded for required output levels. Many of the reduced switch multilevel inverter configurations have primary circuit as level generation part and auxiliary circuit as polarity reversal part (Alishah, R. S., 2016; Rahim, N.A., 2011; Ounejjar, Y., 2011; Najafi, E., 2012). Few of these are only support symmetrical structures with similar dc voltage sources (Ounejjar, Y., 2011; Najafi, E., 2012). A packed U-cells centred asymmetrical MLI that cannot work in symmetrical source conditions is proposed (Ounejjar, Y., 2011). Some reduced switch inverter structures utilize bidirectional switches in their primary circuit (Rahim, N.A., 2011; Kangarlu, M.F., 2013; Piyush L. Kamani., 2020, Shunmugham Vanaja D., 2021). The reduced switch MLIs particularly in renewable energy applications, including photovoltaic systems, have immense potential to enhance the efficiency and reduce the harmonics of grid-connected systems (Y.Sai.Bhargav., 2019). There have recently been several researchers that recommend reduced MLI switch topologies for a PV grid system (Rahim, N.A., 2010; Jana, K.C., 2016). A 7-level grid-connected converter with significantly fewer IGBTs and a DC source with capacitor clamping were identified in 3 equal parts (Rahim, N.A., 2011). Fortunately, the capacitor voltage balance is not precise. For grid-connected PV applications, a generalized multilevel inverter with reduced switch count has been reported (Rahim, N.A., 2010; Ramachandran., 2018). The voltage balancing is clearly discussed among the dc-link voltages of several dc links. Conversely, only these inverters are configured for symmetrical PV voltages and require more switches. No researcher reported the asymmetric MLI with reduced switch configuration for the PV application. This paper proposed an asymmetric MLI structure with minimum switch count by removing bidirectional switches, clamping diodes and capacitors in its design. In addition, the proposed converter has no effect of diode reverse recovery times, capacitor voltage balancing and uses a simple gate driver circuit due to the absence of bidirectional switches. To mitigate switching losses, a low switching frequency control method is used for the proposed inverter, and swarm intelligence-based optimization methods are used to find a viable solution to the transcendental equations for determining the inverter's optimal switching angles.

Problem statement is proposed in section 2. The suggested MLI design and its operating modes are described in section 3, pulse width modulation control and mathematical analysis of transcendental equations is presented is section 4, switching angle optimization using swarm intelligence-based optimization is reported in section 5, results and discussions are presented in section 6. Finally, the conclusions are described in section 7.

II. PROBLEM STATEMENT

The investigation and technological developments of MLIs are essential to improve the power quality of the PV system. The nonlinear properties of the three-level inverters limit their use in PV applications since they do not meet the grid codes. Hence, an LC filter must be placed at the output of three-level inverters to minimize the harmonic content and improve the quality of waveforms per the grid standards. The LC filters cannot reduce the stress on the power switches of the inverter, due to which the efficiency, stability, and reliability of the system are degraded. These problems associated with the three-level inverter will be addressed by designing modular multilevel inverters (MMI) with reduced components. These inverters can be most applicable to medium and high-power applications even though the switching control method is a significant concern for pulse generation for MMIs. The use of high-frequency switching control still creates voltage stress on the power switches, which further affects the power quality of the output of the inverter. However, switch reduction, harmonic reduction, and grid integration are three concerns observed in traditional multilevel inverters and their modulation schemes.

2.1 Reduction in power switches

With the increase in levels, the number of power switches also increases in conventional multilevel inverters, which increases the components of the gate driver and control circuit. Hence the complexity of triggering power switches increases, which affects the inverter's reliability.

2.2 Switching control technique

The switching control method employed for the multilevel inverter is another critical concern for enhancing the power quality at the output. Usually, the high frequency switching modulation techniques causes more power losses and thereby reduce

the inverter efficiency. The total harmonic distortion is reduced at the inverter output by implementing high switching frequency control, but the switching losses get increased during the switching transitions.

III. PROPOSED ASYMMETRIC INVERTER

This research suggested a novel design topology of 15-level asymmetric inverter suitable to fluctuating input voltages such as SPV systems. The basic cell configuration of the suggested model is given in figure 1. It has a single voltage source in series with a power switch connected across the bypass diode. During the switch 'S' is turned ON, the source voltage 'V' appears at the load, then $V_{dc\text{-}out}$ becomes source voltage 'V', and while the switch 'S' is turned OFF then the source voltage is isolated from the load; hence $V_{dc\text{-}out}$ equals to '0'.

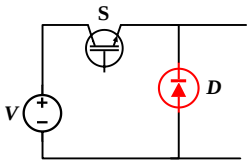


Figure 1. Basic cell Structure

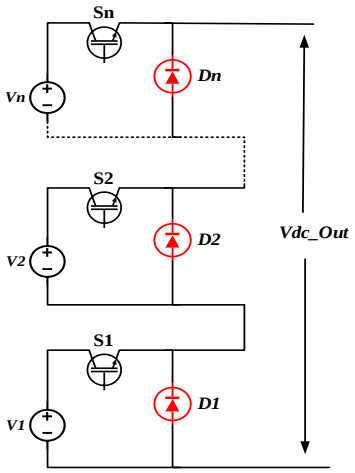


Figure 2. 'n' cell cascaded primary circuit

Basic cell structures are cascaded, as shown in figure 2 for 'n' cell structure of the suggested configuration of the inverter, known as the primary circuit. However, this 'n' cell configuration can generate a multilevel output, only with a positive polarity. The bidirectional output of the inverter can be obtained with polarity reversal by connecting an H-bridge auxiliary circuit at the output of the primary circuit, as shown in figure 3.

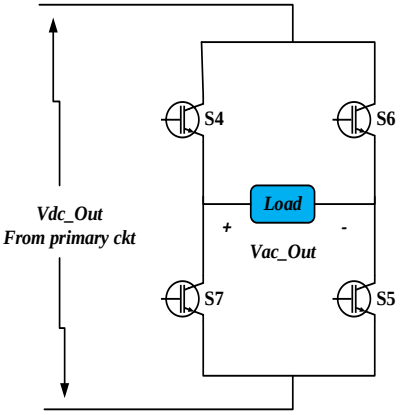


Figure 3. Auxiliary Circuit

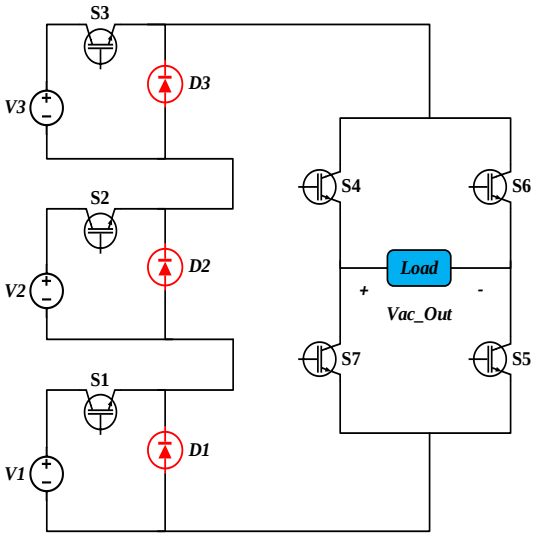


Figure 4. 15-level Asymmetric Inverter

The proposed inverter structure consists of a primary circuit cascaded with 3-basic cell structures and interconnected across the auxiliary circuit, which uses 3-dc sources, 7-controlled switches (IGBTs) and 3-diodes. The proposed topology and switching path choices are configured so that IGBTs or diodes can never dead short circuit with the dc sources. Combining the primary and auxiliary circuits achieves the complete cycle of both +ve and -ve polarity of output. Using a polarity generator (auxiliary circuit) like the H-bridge module, this structure synthesizes 15 output voltage levels with 7-positive, 7-negative and a zero level. The topology of proposed multilevel inverter for 15-level output is shown in figure 4. The voltage rating of numerous dc sources depends on the voltage rating of output levels. The dc source reduced voltage rating specifies V_{dc} step voltage at the output. Different potential dc voltage sources combinations are shown in table 1.

Table 1. Choice of DC sources for suggested asymmetric topology.

Method of Selection	Choice of DC Sources	No of Steps	No of Levels	Max. O/p Voltage

Equal Magnitude	$V_1=V_2=V_3=V_{dc}$	4	7	$3V_{dc}$
Unequal Magnitude	$V_1=V_{dc}, V_2=V_3=2V_{dc}$	6	11	$5V_{dc}$
Binary Approach	$V_1=V_{dc}, V_2=2V_{dc}, V_3=4V_{dc}$	8	15	$7V_{dc}$

The binary approach method is considered for this study among the above three choices of dc source selection, since multilevel inverters work with high efficiency at low switching and conduction losses as the number of output voltage levels are significantly high with minimum number of sources and switching devices. Therefore, the choice of voltages for 15-level output is as follows,

$$V_1= V_{dc}$$
$$V_2= 2V_{dc}$$
$$V_3= 4V_{dc}$$

This approach also offers asymmetrical operation to multilevel inverter ideal for fluctuating PV voltages due to variable solar irradiance. The switching sequence for different levels of output step voltages is given in table 2 from +7Vdc to -7Vdc, including '0' voltage level.

Table 2. Asymmetric switching sequences and output voltage levels of presented 15-level inverter.

ON Switches	Power flow path	Output voltage level
S_1, S_2, S_3, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow V_1^-$	$+7V_{dc}$
S_2, S_3, S_4 & S_5	$V_2^+ \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow D_1 \rightarrow V_2^-$	$+6V_{dc}$
S_1, S_3, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow V_1^-$	$+5V_{dc}$
S_3, S_4 & S_5	$V_3^+ \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow D_1 \rightarrow D_2 \rightarrow V_3^-$	$+4V_{dc}$
S_1, S_2, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow D_3 \rightarrow S_4 \rightarrow$Load $\rightarrow S_5 \rightarrow V_1^-$	$+3V_{dc}$
S_2, S_4 & S_5	$V_2^+ \rightarrow S_2 \rightarrow D_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow D_1 \rightarrow V_2^-$	$+2V_{dc}$
S_1, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow D_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow V_1^-$	$+V_{dc}$
S_4 & S_6 (or) S_5 & S_7	$S_4 \rightarrow$ Load $\rightarrow S_6 \rightarrow S_4$ (or) $S_5 \rightarrow$ Load $\rightarrow S_7 \rightarrow S_5$	0
S_1, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow D_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow V_1^-$	$-V_{dc}$
S_2, S_6 & S_7	$V_2^+ \rightarrow S_2 \rightarrow D_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow D_1 \rightarrow V_2^-$	$-2V_{dc}$
S_1, S_2, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow D_3 \rightarrow S_6 \rightarrow$Load $\rightarrow S_7 \rightarrow V_1^-$	$-3V_{dc}$
S_3, S_6 & S_7	$V_3^+ \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow D_1 \rightarrow D_2 \rightarrow V_3^-$	$-4V_{dc}$
S_1, S_3, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow V_1^-$	$-5V_{dc}$
S_2, S_3, S_6 & S_7	$V_2^+ \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow D_1 \rightarrow V_2^-$	$-6V_{dc}$
S_1, S_2, S_3, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow V_1^-$	$-7V_{dc}$

The switches S_4 and S_5 in the auxiliary circuit conduct continuously for 7-levels of +ve half cycle of output voltage, and switches S_6 & S_7 conducts continuously for 7-levels of -ve half cycle of output. The '0' output level is obtained by either short circuit of load with switches S_4 & S_6 is ON or S_5 & S_7 is ON. Thus, the fifteen-level output voltage is obtained from the proposed converter by operating the primary and axillary circuits according to the switching conditions described in table 2.

IV. COMPARISON WITH SIMILAR TOPOLOGIES

The main aim of using a reduced switch multilevel inverter is to raise output voltage levels by using the fewest possible electronic components. Thus, many distinctions are made from switch count, control circuits and DC sources between the proposed topology and the standard cascaded inverters of similar type. Furthermore, the maximum voltage blocked by the power switches is often compared to the other topologies.

The comparison between the number of dc sources, switches, diodes, and capacitors required for various topologies cited in this article with suggested topology is shown in figure 5, and a comparison for the device ratio concerning the number of levels is presented in figure 6. This distinction demonstrates that the suggested topology uses fewer devices in its design. The comparison for various asymmetric MLIs for N-level output is given table 3.

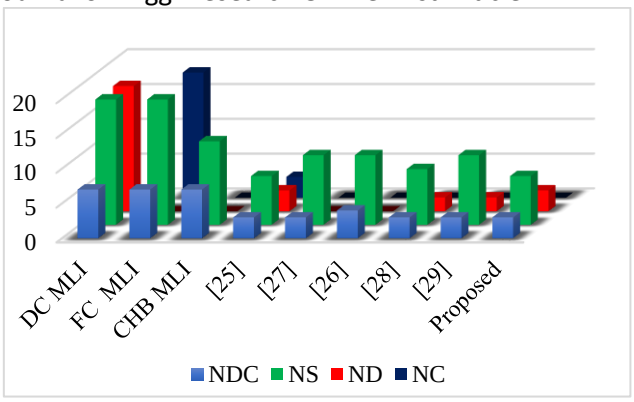


Figure 5. Comparison between the existing 15-level asymmetric topologies and proposed 15-level inverters.

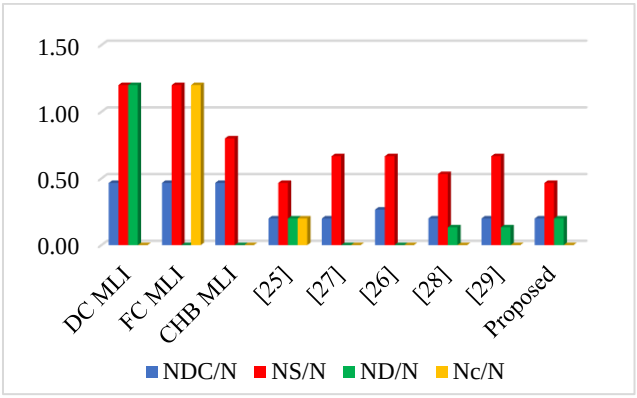
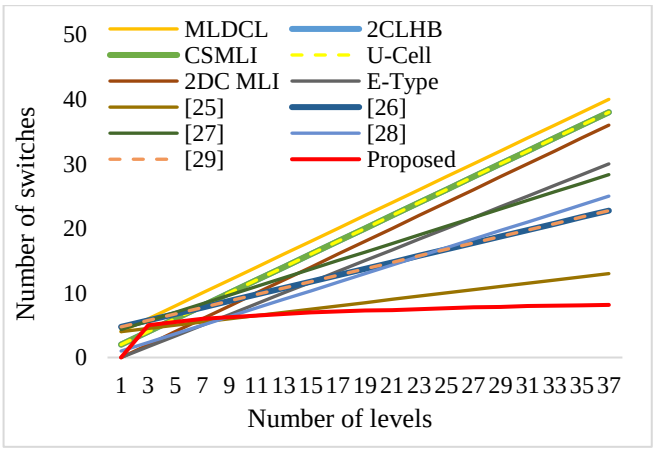


Figure 6. DC Sources, Switches, Diodes & Capacitor ratio comparison for 15-level asymmetric inverters.

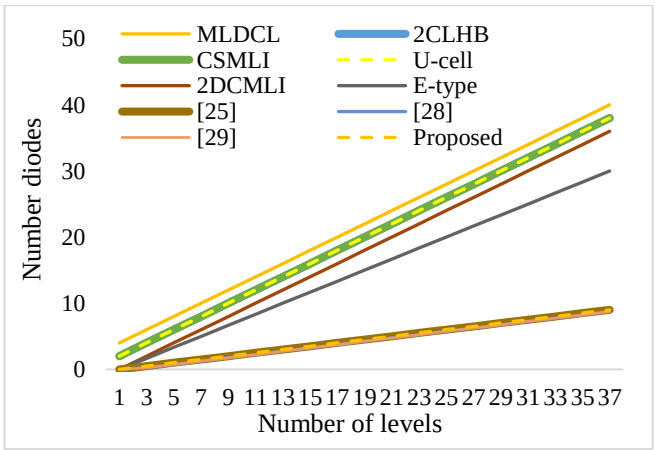
Table 3. Comparison of various asymmetric MLIs with proposed MLI for N-levels

Type of Inverter	No of Switches	No of Diodes	No of DC sources	TSV (xVdc)
NPC	2(N-1)	N+1	(N-1)/2	2(N-1)
FC	2(N-1)	2(N-1)	N-1	2(N-1)
CHB	2(N-1)	2(N-1)	(N-1)/2	2(N-1)
MLDCL	N+3	N+3	(N-1)/2	3(N-1)
2CLHB	N+1	N+1	(N-1)/2	2(N-1)
CSMLI	N+1	N+1	(N-1)/2	2(N-1)
U-Cell	N+1	N+1	(N-1)/2	2(N-1)
2DCMLI	N-1	N-3	(N-1)/3	(N-1)/3
E-Type	5(N-1)/6	5(N-1)/6	(N-1)/6	10(N-1)6
[25]	(N-1)/4+4	(N-1)/4	(N-1)/4	(N-1)/2
[26]	(2N+1)/4+4	0	(N+1)/4	(2N+1)/2
[27]	(2N-1)/3+4	0	(N-1)/4	(N-1)/2
[28]	(N+1)/6	(N-2)/4	(N-1)/4	(N-2)/2
[29]	(2N-1)/4+4	(N-2)/4	(N-1)/3	(N-1)/2
Proposed	(N-1)/4+4	(N-1)/6	(N-1)/4	(N-1)/4

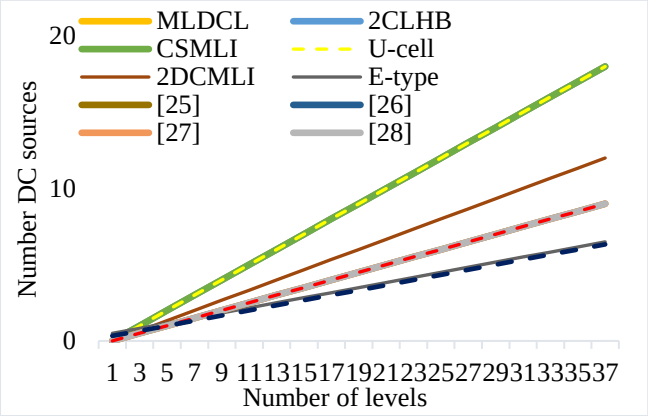
Where, N_{DC} = Number of dc voltage sources
N_S = Number of power switches
N_D = Number of power diodes
N_C = Number of capacitors
N = Number of voltage levels



(a)



(b)



(c)

Figure 7. Comparison between the design components of various MLIs
(a) Required number of switches Vs number of levels
(b) Required number of diodes Vs number of levels
(c) Required number of dc sources Vs number of levels

The above figure 7 compares the devices required for the design of various multilevel inverters with the proposed multilevel inverter for different levels of output voltage.

V. CONTROL METHODOLOGY OF PROPOSED MLI

5.1 Fundamental Switching Frequency Control (FSFC)

Fundamental switching frequency control is one of the best PWM control methods for multilevel converters. FSFC control can be achieved based on Selective Harmonic Elimination (SHEPWM). The key features of SHEPWM are compared with other switching methods and is given in table 4.

Table 4. Comparison between switching control methods with SHEPWM

Method of switching	SVPM	SVPWM	SHEPWM
Utilization of dc sources	0~0.866	0~1	0~1.12
Frequency of switching	Medium	High	Low
Complexity	Low	High	High
Implementation	Online	Online	Offline

Generally, the waveform of multilevel inverter output is expressed using Fourier series expansion. The generalized expression for Fourier series expansion is given as:

$$V(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n\omega t) \quad (1)$$

Here, V_n = n^{th} harmonic voltage magnitude. Due to the odd symmetry of the quarter wave, the even-order harmonics in the output of the inverter becomes zero. Therefore the expression for V_n becomes,

$$V_n = \begin{cases} \frac{4V_{dc}}{n\pi} \sum_{i=1}^{k} cos(n\alpha_i) \, ; for\ odd\ values\ of\ 'n' \\ 0; \ for\ even\ values\ of\ 'n' \end{cases} \quad (2)$$

Where, α_i is the switching angles of i^{th} harmonic and is between 0^0-90^0 (i.e. $0 < \alpha_i < \frac{\pi}{2}$).

SHEPWM aims to suppress lower order harmonics, whereas harmonic filters removed remaining harmonics. This research developed a 15-level asymmetric inverter with a fundamental switching frequency control scheme to conceal the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th} harmonic voltages. The application of 15-level output will reduce the size of the harmonic filters as the prominent harmonics from 5^{th} to 19^{th} harmonics are controlled.

$$\left.\begin{aligned}
\frac{4V_{dc}}{\pi}\left[\cos\alpha_1+\cos\alpha_2+\cdots\ldots+\cos\alpha_7\right] &= V_1\\
\frac{4V_{dc}}{5\pi}\left[\cos5\alpha_1+\cos5\alpha_2+\cdots\ldots+\cos5\alpha_7\right] &= V_5\\
\frac{4V_{dc}}{7\pi}\left[\cos7\alpha_1+\cos7\alpha_2+\cdots\ldots+\cos7\alpha_7\right] &= V_7\\
\frac{4V_{dc}}{11\pi}\left[\cos11\alpha_1+\cos11\alpha_2+\cdots\ldots+\cos11\alpha_7\right] &= V_{11}\\
\frac{4V_{dc}}{13\pi}\left[\cos13\alpha_1+\cos13\alpha_2+\cdots\ldots+\cos13\alpha_7\right] &= V_{13}\\
\frac{4V_{dc}}{17\pi}\left[\cos17\alpha_1+\cos17\alpha_2+\cdots\ldots+\cos17\alpha_7\right] &= V_{17}\\
\frac{4V_{dc}}{19\pi}\left[\cos19\alpha_1+\cos19\alpha_2+\cdots\ldots+\cos19\alpha_7\right] &= V_{19}
\end{aligned}\right\} \quad (3)$$

Where, V_5, V_7, V_{11}, V_{13}, V_{17}, V_{19} are the harmonic voltages required to suppress to reduce the THD of output voltage. Therefore, these are equated to zero and the resulting equation can be represented in equation (5). The fundamental voltage component in equation (3) is equated to modulation index corresponding PWM scheme, which can be written as:

$$M = \frac{V_1}{V_{1\max}} \quad (4)$$

Where, V_{1max} = Peak fundamental voltage

$$V_{1max} = \frac{4kV_{dc}}{\pi}$$

V_1 = Actual fundamental voltage
k = Degree of freedom = $(L-1)/2$
L= No of output voltage levels

By combining (3) and (4) the above conditions can be written as follows.

$$\left.\begin{aligned}
\frac{4V_{dc}}{\pi}\left[\cos\alpha_1+\cos\alpha_2+\cos\alpha_3+\cos\alpha_4+\cos\alpha_5+\cos\alpha_6+\cos\alpha_7\right] &= f_1(\alpha) = M\\
\frac{4V_{dc}}{5\pi}\left[\cos5\alpha_1+\cos5\alpha_2+\cos5\alpha_3+\cos5\alpha_4+\cos5\alpha_5+\cos5\alpha_6+\cos5\alpha_7\right] &= f_2(\alpha) = 0\\
\frac{4V_{dc}}{7\pi}\left[\cos7\alpha_1+\cos7\alpha_2+\cos7\alpha_3+\cos7\alpha_4+\cos7\alpha_5+\cos7\alpha_6+\cos7\alpha_7\right] &= f_3(\alpha) = 0\\
\frac{4V_{dc}}{11\pi}\left[\cos11\alpha_1+\cos11\alpha_2+\cos11\alpha_3+\cos11\alpha_4+\cos11\alpha_5+\cos11\alpha_6+\cos11\alpha_7\right] &= f_4(\alpha) = 0\\
\frac{4V_{dc}}{13\pi}\left[\cos13\alpha_1+\cos13\alpha_2+\cos11\alpha_3+\cos13\alpha_4+\cos13\alpha_5+\cos13\alpha_6+\cos13\alpha_7\right] &= f_5(\alpha) = 0\\
\frac{4V_{dc}}{17\pi}\left[\cos17\alpha_1+\cos17\alpha_2+\cos17\alpha_3+\cos17\alpha_4+\cos17\alpha_5+\cos17\alpha_6+\cos17\alpha_7\right] &= f_6(\alpha) = 0\\
\frac{4V_{dc}}{19\pi}\left[\cos19\alpha_1+\cos19\alpha_2+\cos19\alpha_3+\cos19\alpha_4+\cos19\alpha_5+\cos19\alpha_6+\cos19\alpha_7\right] &= f_7(\alpha) = 0
\end{aligned}\right\} \quad (5)$$

The switching angles must not violate the constraints,

$$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2} \quad (6)$$

The set of nonlinear equations in (5) can be solved using constraint (6) to obtain the switching angles required for the fifteen-level inverter. These equations can be solved using a fundamental switching frequency control method and optimization methods to optimize the inverter's switching angles. Any optimization strategy requires developing a fitness function related to the variables to be evaluated. The primary objectives are,

- To obtain the base voltage value equivalent to any preset or expected value.
- To suppress or reduce a few harmonics of lower order.

The inverter's switching angles influence the output harmonic voltages. The generalized harmonic voltage fitness function (FF) consists of the following form to achieve the above objectives:

$$OF = min_{\alpha_k}\left\{\left(100 * \frac{V_1^* - V_1}{V_1^*}\right)^4 + \sum_{K=2}^{N} \frac{1}{h_k}\left(50 * \frac{V_{h_k}}{V_1}\right)^2\right\} \quad (7)$$

To minimize the 5th, 7th, 11th, 13th, 17th, 19th harmonics the above objective function can be taken as

$$OF = 100 * \frac{(V_{1d} - V_1)^4}{V_{1d}^4} + \left(\frac{50}{V_1}\right)^2 * \left(\frac{V_5^2}{5} + \frac{V_7^2}{7} + \frac{V_{11}^2}{11} + \frac{V_{13}^2}{13} + \frac{V_{17}^2}{17} + \frac{V_{19}^2}{19}\right) \quad (8)$$

This research aims to minimize the above objective function to reduce the THD. The transcendental equations in (5), satisfying the constraint function (6) with fitness function (8), can be solved by using nature-inspired optimization algorithms for minimum THD and optimal switching angles of the proposed multilevel inverter.

The control methodology for obtaining switching angles for the proposed fifteen level asymmetric inverter is shown in figure 8. The transcendental equations were solved based on the dc-link voltage required, which is the reference voltage for setting a modulation index, and lookup tables will generate the optimized switching angles with a selected optimization algorithm for the solver.

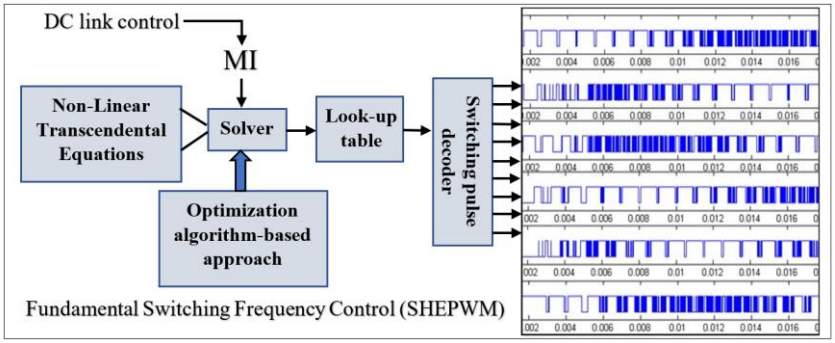


Figure 8. Control Methodology of Proposed MLI

5.2 Optimization Algorithms

Optimization has been the most inspiring technique for many design applications, showing significant progress of computing systems. These optimization schemes can define optimal requirements and optimize operations and high production efficiency. Formulating the objective function/stiffness function for a minimum problem occurs in chosen optimization strategies. In recent years, metaheuristic algorithms have been mainly used to solve many of the nonlinear equations of all classical optimization approaches to provide effective solutions for real-time implementations. The following are some essential and feasible optimization schemes used for solving the nonlinear transcendental equation (5) and the algorithms and approaches to the SHEPWM problem.

A) Genetic Algorithm

Computerized search methods are the genetic algorithms (GAs) based on natural selection and genetics. These algorithms are beneficial for probably large search areas. They are navigated relatively quickly to search for suitable combinations of the solution set, which could require a very long period for other techniques.

Genetic algorithms are based on the population size of pre-selected candidates. The implementation of genetic algorithms takes place following phases.

1. ***Initialization:*** The initial population set of any candidate solutions has been created by random means of the following equation across the whole search space, close to the centre of every switching boundary. For each solution set, the number of populations was calculated as 20.

$$\alpha_{ij}^{IP} = \alpha_{ij} + \left[\alpha_{ij}^{L} \pm rand_j\left\{\frac{\left(\alpha_{ij}^{U} - \alpha_{ij}^{L}\right)}{2}\right\}\right] \quad (9)$$

Where, α_{ij}^{IP} represents initial population matrix, α_{ij}^{L} initial guess of solutions from $\alpha_1 to\ \alpha_7$

2. ***Evaluation:*** The fitness values of the candidate solutions will be determined using the pre-formulated objective function shown in the equation when the population set for each switching angle is initialized or the offspring populations are established.

$$F_{OBJ}(\alpha) = \frac{1}{1 + F(\alpha)} \quad (10)$$

Where,

$$F(\alpha) = modf_1(\alpha) + modf_2(\alpha) + modf_3(\alpha) + \cdots$$

3. ***Selection:*** Several higher fitness values have been chosen to produce offspring, thus applying the most suitable survival strategy for the candidates' solutions. *This* was done by calculating the cumulative probability using the fitness value of each population with the random number (0,1) provided by the selection of the roulettes.
4. ***Crossover or Recombination:*** The combination of two or more parental solutions blends to generate multiple (e.g., offspring) solutions. Each solution is converted into 11-bit binary, parental pairs have been randomly picked for crossover solutions; a 'r' random number is generated for each pair in the random variant of (0,1) so that "r" is equal to a pre-determined crossover probability (here, 0,6), to decide whether it should be perforated. A random number of (1,10) were produced to choose a convergence point when it was found. A single point crossover has been used here.
5. ***Mutation:*** By recombining two or more parental chromosomes, local yet random mutations alter a solution to boost the solution. Here too, for and descendant, a random number 'r' between (0,1) is generated in which the 'r' contrasts with the predetermined mutation probability (here 0,1). A random number was generated between (1.10) when the mutation was deemed appropriate to select the point of mutation and this specific bit was complemented.
6. ***Replacement:*** Selecting, recombining, and mutating the parental population of the first generation was used to replace the parents of the second generation.
7. ***Termination:*** Until a given termination condition was met, steps 2-6 were repeated.

B) Particle Swarm Optimization

Kennedy and Eberhart suggested PSO in 1995, and it defines Swarms' sociological behaviour. Each particle's PSO vectors are 1 x N and the vector of each particle. The best individual location in an identified particle is the local best, and the best position in the whole swarm is the global best. PSO is ideally suited to solving complex problems due to its low computation effort and quick computer coding. Initial values such as other traditional iterative methods are not required for PSO (Albert Alexander., 2015; Dishore S.V., 2020, D. G. Kumar., 2021). In the following steps, the PSO mechanism can be articulated:

Step 1: Initialize the parameters of particle vectors X_i, V_i, P_{best}, G_{best}, and inertia weight of the particle C_0. Choose a number of generations as 100, size of the population as 40, cognitive parameter C1 as 0.5 and social parameter C2 as 1.25.

Step 2: Test the conditions for $0 < (C_1 + C_2) < 2$ and $(C_1 + C_2)/2 < C_0 < 1$, The system would then be guaranteed to converge to a stable equilibrium position if the two conditions were met. If false, go to Step 1.

Step 3*:* The particles' new position and velocity vectors were determined using the following equation.

$$v_l^i(t+1) = w(t).v_l^i(t) + C_{ind}.rand1,(p_l^i - x_l^i(t) + C_{soc}.rand2.(G^i - x_l^i(t)) \quad (11)$$

Then the new position is defined as,

$$x_l^i(t+1) = x_l^i(t) + v_l^i(t+1) \quad (12)$$

Step 4: Evaluate the objective function of the particles using

$$\text{OF} = min_{\alpha_k}\left\{\left(100 * \frac{V_1^* - V_1}{V_1^*}\right)^4 + \sum_{K=2}^{N}\frac{1}{h_k}\left(50 * \frac{V_{h_k}}{V_1}\right)^2\right\} \quad (13)$$

Step 5: Check for the constraint on fitness function as

$$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2} \quad (14)$$

Step 6: check for P(xi) < P(Pi), if not then i = i + 1 go to step3.

Step 7: Update the particle's best local position if the best local position is better than before. Thus Pi = Xi replaces the local best position.

Step 8: Pg = min (P neighbor).

Step 9: Terminate the process if the optimal switching angles are achieved.

C) Whale Optimization Algorithm

WOA is a population-based algorithm developed in 2016 by Mirjalili & Lewis. This algorithm simulates humpback whales' social behaviour.

WOA, like other population-based algorithms, uses a random solution (people) and three rules to update and develop candidate solutions in each stage that encircle the prey, spiral update position, and search for prey (D. G. Kumar., 2021).

a) Exploitation Phase: Bubble net attacking

The algorithm comprises two steps; the first step concerns the exploitation phase with encircling pray and the spiral position updating. The second step is the exploration phase called searching pray. There are two approaches for modelling the behaviour of humpback whales in the Bubble Sea, which is called mathematical exploitation.

(1) Encircling Prey: After discovering the position of the prey, they encircle them. Therefore, the WOA algorithm implies that the current leading candidate solution is the optimal target, assuming that the appropriate solution is not located in the search area. The other search agents then seek to switch their location to the better search agents. The following equations describe this behaviour:

$$\vec{X}(t+1) = \overrightarrow{X^*}(t) - \vec{A}.\vec{D} \quad (15)$$

$$\vec{D} = \left|\vec{C}.\overrightarrow{X^*}(t) - \vec{X}(t)\right| \quad (16)$$

Where $\overrightarrow{X^*}(t)$ is the previous best location for the whale in iteration t. $\overrightarrow{X}(t+1)$ is the current location of the whale, $\vec{D}$ is a vector distance between pray and whale, and | | indicates absolute value. The coefficients C and A are calculated as follows:

$$\vec{A} = 2.\ \vec{a}.\vec{r} + \vec{a} \quad (17)$$

$$\vec{C} = 2.\ \vec{r} \quad (18)$$

The value of $\vec{a}$ is decreased to apply shrinking in equation (3); therefore, the range of oscillation of $\vec{A}$ is also decremented by $\vec{a}$. The $\vec{A}$ value could be lies in $(-a, a)$ interval, where a value is reduced by iterations from 2 to 0. By choosing random values of $\vec{A}$ between $(-1, 1)$, any search agent may decide the new position somewhere between the agent's original location and the existing best agent location.

(2) Spiral position Updating: The interval between the whale and the prey is estimated at (X, Y), and the prey is positioned at (X*, Y*). In this case, a spiral approximation between the whale's location and the prey is generated to track the humpback whales' loop movement as follows:

$$\vec{X}(t+1) = e^{bk}.\cos(2\pi k).\overrightarrow{D^*} - \overrightarrow{X^*}(t) \quad (19)$$

$$\overrightarrow{D^*} = \left|\overrightarrow{X^*}(t) - \vec{X}(t)\right| \quad (20)$$

Where b is the logarithmic spiral's scalar quantity and k is a random number in the range [-1, 1]. This behaviour influences the role of whales in the WOA while optimizing. The shrinking circular pattern and the spiral pattern have a 50 percent chance of being chosen, and the following are the elements of each:

$$\vec{X}(t+1) = \begin{cases} \overrightarrow{X^*}(t) - \vec{A}.\vec{D} & \text{if } p < 0.5 \\ e^{bk}.\cos(2\pi k).\overrightarrow{D^*} - \overrightarrow{X^*}(t) & \text{if } p > 0.5 \end{cases} \quad (21)$$

Where p is an arbitrary number in the range (0, 1).

b) Exploration Phase: Searching Pray

In the exploration phase of the search process for the presa, a particular method based on the vector $\vec{A}$ variances may be used. The whales deliberately search at random to find their food based on the location of one another. As a result, WOA forces the search agents to move away from the local whale by using the vector $\vec{A}$ with random values greater or smaller than 1. Instead of the best search agent being reorganized during the discovery period, the search agent's position is random.

$$\vec{X}(t+1) = \overrightarrow{X_{rand}} - \vec{A}.\vec{D} \quad (22)$$

$$\vec{D} = \left|\vec{C}.\overrightarrow{X_{rand}} - \vec{X}\right| \quad (23)$$

D) Harris Hawks Algorithm

The Harris Hawk optimizer is a novel population-based, nature-inspired optimization model. The main inspiration for HHA named surprise pounce is the cooperative behaviour and chasing style of Harris' hawks in the wild. Many hawks work together to pounce on prey from different directions in this clever tactic. Harris hawks can reveal a variety of chase patterns depending on the situation's complexity and the prey's escaping patterns. For optimum MLI switching angles using SHEPWM, Harris hawk's knowledge while hunting pray is mathematically formulated.

Step1-Exploration Phase: Harris hawks stick up arbitrarily, sit in certain areas, follow and track the prey. The leader hawks are focused on the location of the communities and their prey. This is defined as a mathematical equation for distance (q) switch between hawks and prey, as follows:

$$X(t+1) = \begin{cases} X_{rand}(i) - r_1 X_{rand}(t) - 2r_2 X(t) & q \geq 0.5 \\ X_r(t) - X_m(t) - r_3(LB + r_4(UB - LB)) & q < 0.5 \end{cases} \quad (24)$$

Where,

r_1, r_2, r_3, r_4 *and* q are the random values in the range between 0 and 1. $X(t+1)$ is the position update vector of the Hawk for the $(i+1)^{th}$ iteration, $X_r(t)$ is the position of the pray and $X(t)$ is position vector of the Hawk at the i^{th} iteration. U_B & L_B are the Upper & Lower bounds, respectively and $X_{rand}(t)$, $X_m(t)$ are the random populations.

Each hawk has an average position as:

$$X_{i+1}(t) = \frac{1}{N}\sum_{i=1}^{N} X_i(t) \quad (25)$$

Where,

$X_i(t)$ = Hawks current position.

$X_{i+1}(t)$ = Updating position vector.

N= Number of Hawks.

Step2 - The hawks attempt to identify and reach the prey during the exploration phase. As a result, the energy (E) of the prey is significantly modified and provided by

$$Escaping\ Energy, E = 2E_0\left(1 - \frac{t}{T}\right) \quad (26)$$

Where T is the maximum iteration number, t is the current iteration, and the initial energy (E_0) varies at random from (-1 to 1) during each iteration. $E \geq 1$ indicates that the prey is tired and that hawks are looking for prey in a new location. $E < 1$ also indicates that the prey is tired and that its attack is intensified by fast striking.

Step3 - Exploitation phase: The switching tactics will begin to focus on the prey at this stage. The prey still tends to escape from the hawks, and it is seen that the potential to escape the prey is 'r'. If r<0.5 the prey can escape safely; if r≥0.5 it would be unable to escape. Even so, the hawks target the prey and win or lose in a soft or hard siege. The hard siege takes place as the prey escape if (r≥0.5) and $|E|$< 0.5. If (r≥0.5) and $|E|$≥0.5 then there will be a soft siege. 'r' is a chance for the prey to escape here. It can be modelled in the following mathematical form in steps 4 to 7.

Step4 - Soft siege: The prey here (switching angle for proposed problem) has potential and is trying to escape by sprouting and is smoothly modelled around the hawks.

$$X(t+1) = \Delta X(t) - E|JX_\alpha(t) - X(t)| \quad (27)$$

$$\Delta X(t) = X_\alpha(t) - X(t) \quad (28)$$

J=2(1−r5) is the prey jumps at random.

ΔX(t) is the difference in the position of the vector in successive iterations to r5, which is a random number inside the (0,1) range.

Step5 - Hard siege: The prey in this situation is completely tired and barely surrounded by the hawks and surprise. The locations will be updated by (28)

$$X(t+1) = X_\alpha(t) - E|\Delta X(t)| \quad (29)$$

Step6 - Soft siege with continued rapid dives: The prey still has the energy and is attempting to get away from it, which can be summarized as total and r<0.5, with a soft siege needed to begin until the hawks begin to pounce. This move is more intelligent than in the past. The Levy flight (LF) concept has been applied to progressive rapid dives of hawks for the soft siege, and the next move is calculated by the hawks using the following equation:

$$Y = X_\alpha(t) - E|JX_\alpha(t) - X(t)| \quad (30)$$

Although they have attempted several times, the hawks are comparing each movement with the previous dive to figure out whether it was a successful dive. The animal is treated irregularly, briefly, and rapidly if diving is unsuccessful. We presume that the hawks dive in the following rules based on LF patterns:

$$Z = Y + S * LF(D) \quad (31)$$

D is the dimension of the problem, S is the random vector 1 to D, and LF is the levy flight function to follow:

$$LF(x) = 0.01 * \frac{u*\sigma}{|v|^{\frac{1}{\beta}}} \quad (32)$$

$$\sigma = \left(\frac{\Gamma(1+\beta)*sin\left(\frac{\pi\beta}{2}\right)}{\Gamma\left(\frac{1+\beta}{2}\right)*\beta*2^{\left(\frac{\beta-1}{2}\right)}} \right)^{\frac{1}{\beta}} \quad (33)$$

Where u and v are unintended values (0, 1) and β are expected to be 1.5. Therefore, in the soft siege phase the last upgrade rule of the hawk position is:

$$X(t+1) = \begin{cases} Y & if\ F(Y) < F(X(t)) \\ Z & if\ F(Z) < F(X(t)) \end{cases} \quad (34)$$

Where Y and Z are calculated using (32) and (33).

Step7 - In this case, a hard siege of relentless quick dives: and r<0.5 are lost and exhausted. The hawks then use a hard siege, in which they keep their distance from the prey to kill it. The updating rule in this case is:

$$X(t+1) = \begin{cases} Y & if\ F(Y) < F(X(t)) \\ Z & if\ F(Z) < F(X(t)) \end{cases} \quad (35)$$

$$Y = X_\alpha(t) - E|JX_\alpha(t) - X_m(t)| \quad (36)$$

$$Z = Y + S * LF(D) \quad (37)$$

For the latest iteration, Y and Z at (38) and (39) are the next positions before the prey is killed, i.e. the optimal solution is achieved.

VI. RESULTS & DISCUSSIONS

The proposed 15-level asymmetric multilevel inverter is simulated on MATLAB Simulink using GA, PSO, WOA, and HHO with the SHE PWM switching control technique. The proposed asymmetrical structure's input DC sources are 37V, and the obtained peak value (Vpeak) is 259 V. The proposed inverter's switching frequency is 50Hz, the harmonic frequency is 1kHz, and the Nyquist frequency of total harmonics is 5kHz. To get a current magnitude of 10A at 259V peak and to obtain the current waveform like a near sinusoid, the load values are chosen as, R = 26.8 Ω and L = 9.9 mH. For a modulation index of 0.9, the switching angles are calculated. The output voltage of the proposed symmetric multilevel inverter is shown in figure.18. The proposed structure generates a 15-level output voltage when the DC sources are in the ratio of 1:2:4 as shown in Table 1. Table 5 shows the THD obtained from the proposed asymmetric multilevel inverter (15-level) for Harmonic and Nyquist frequencies.

The fitness function is evaluated using four algorithms such as GA, PSO, WOA and HHA. The number of iterations taken for converge solution of the fitness function is given in table 5. It is observed for the results that, the HHA algorithm converged in less number of iterations (75 iterations) compared to other algorithms and the corresponding THD is also obtained as 5.51% at Nyquist frequency, 2.55% at harmonic frequency which is minimum compared to the THDs obtained with other algorithms proposed. The comparison between the convergences characteristics of four algorithms was presented in figure 9.

Table 5. Optimal switching angles resulted from different optimization algorithms for proposed multilevel inverter.

Algorithm	α_1	α_2	α_3	α_4	α_5	α_6	α_7
GA	5.6^0	10.9^0	18.6^0	26.5^0	34.8^0	44.6^0	61.2^0
PSO	3.9^0	12.1^0	20.9^0	29.9^0	38.1^0	48.7^0	61.1^0
WOA	4.3^0	11.89^0	20.6^0	28.6^0	40.6^0	48.5^0	63.6^0
HHA	3.9^0	11.4^0	19.5^0	28.9^0	39.2^0	50.5^0	62.6^0

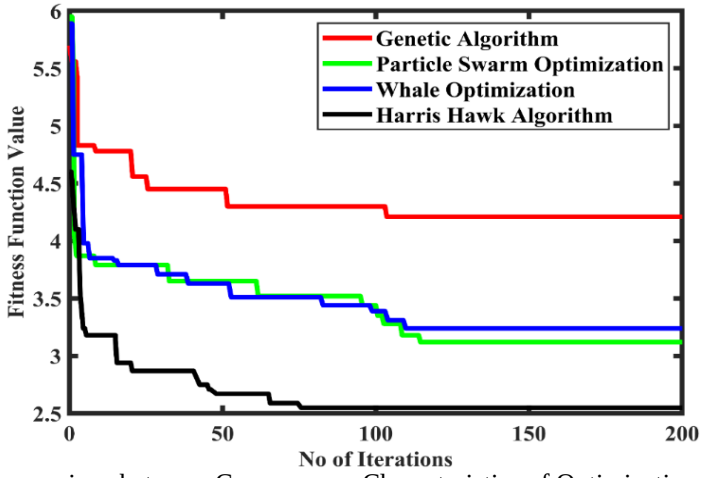


Figure 9. Comparison between Convergence Characteristics of Optimization Algorithms

The gating pulses for the prosed asymmetric inverter is generated using the methodology given in figure 8. Switch S_1 is the high-frequency switch, and switch S_3 is the low-frequency switch in the primary circuit. The corresponding switching pulses at 0.9 modulation index is shown in figure 10. Gating pulses of the auxiliary circuit is given in figure 11. The auxiliary circuit is an H-bridge in nature, and it can be used for polarity reversal at the output voltage.

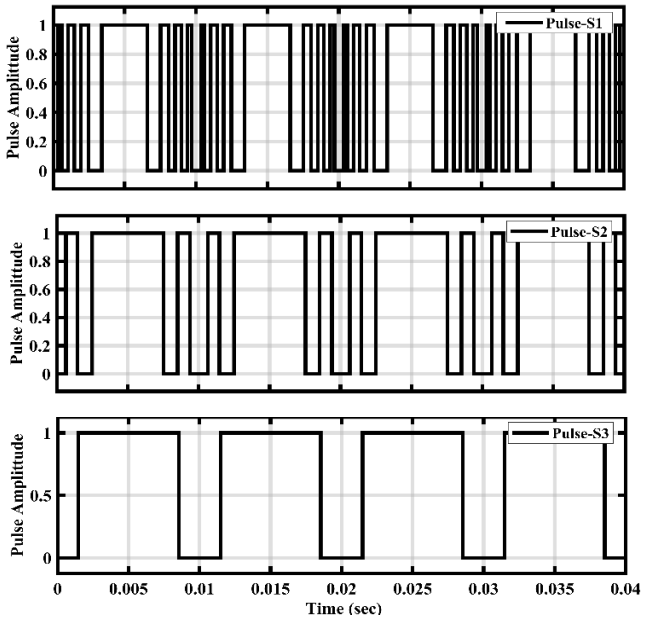


Figure 10. Gating pulses for the primary circuit

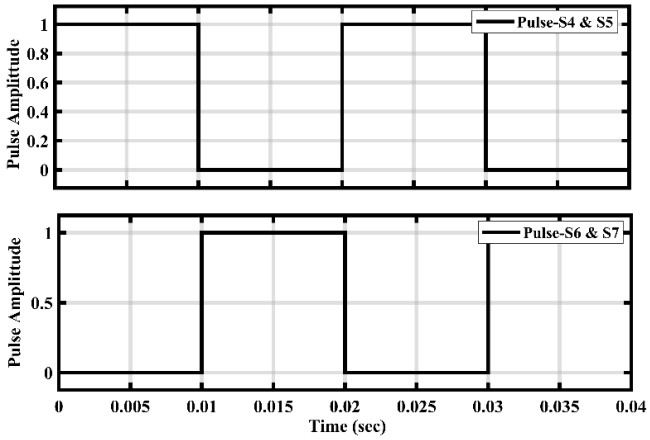


Figure 11. Gating pulses for the auxiliary circuit

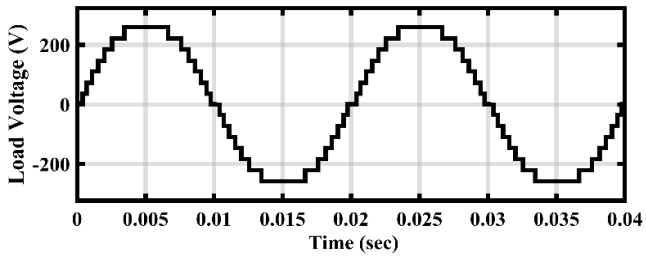


Figure 12.15-level load voltage waveform of suggested inverter

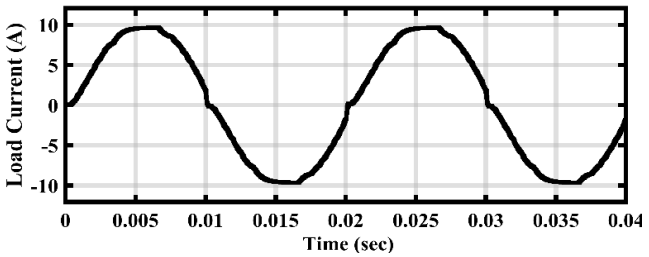


Figure 13. Load current waveform of the suggested inverter

The suggested topology's load voltage and load current are simulated and presented in figure 12 and figure 13, respectively. The load current is almost fine-tuned without any harmonic filters to resemble a near sinusoidal waveshape.

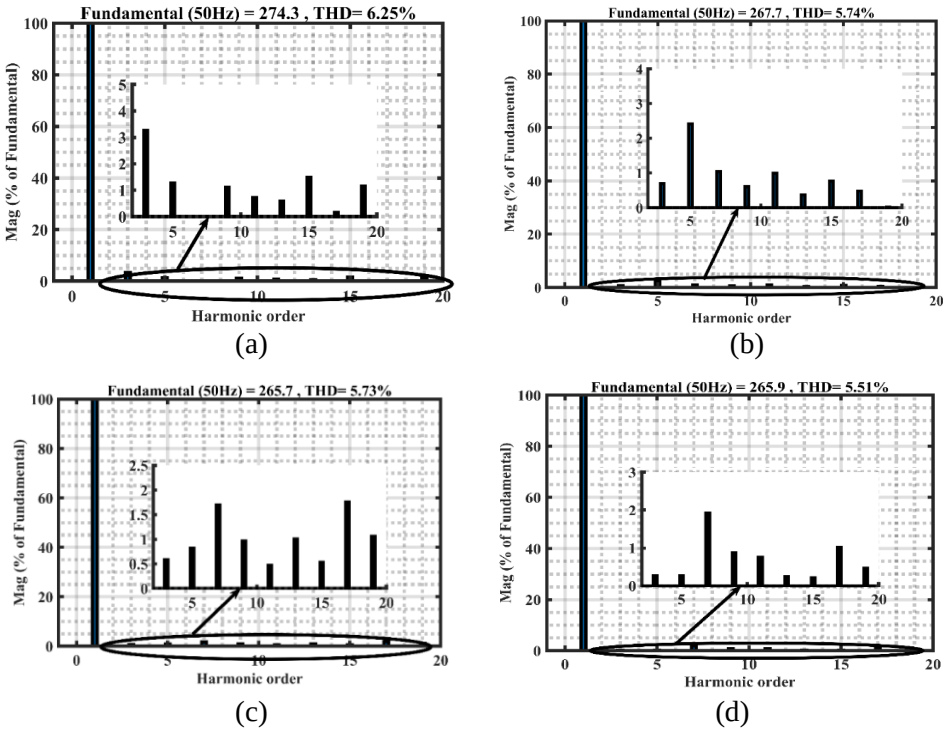


Figure 14. Voltage Harmonic Distortion (a) GA (b) PSO (c) WOA (d) HHA

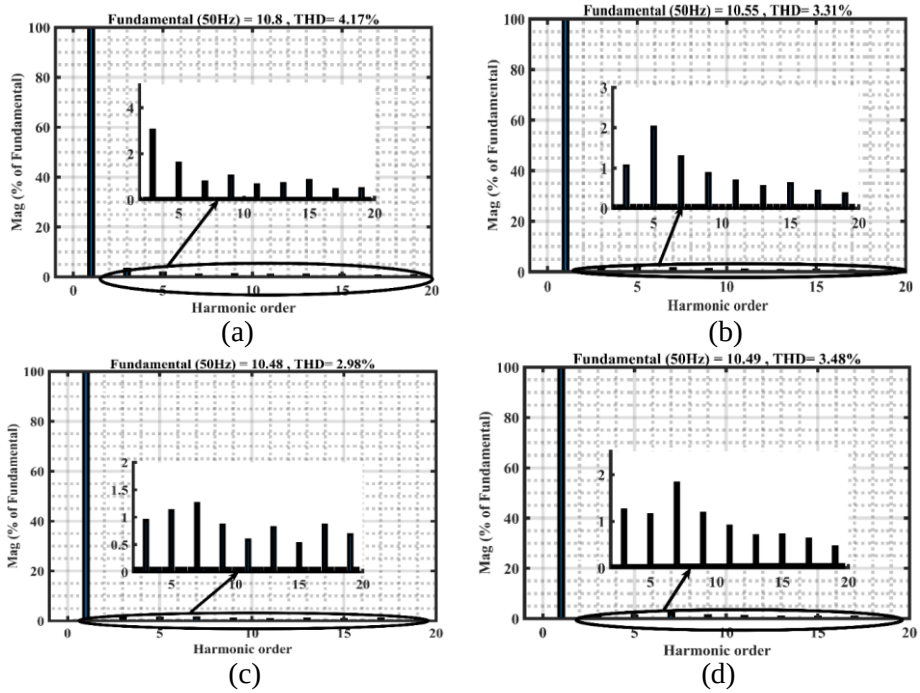


Figure 15. Current Harmonic Distortion (a) GA (b) PSO (c) WOA (d) HHA

The optimization algorithms of GA, PSO, WOA and HHA algorithms are applied for the control algorithm of switching angle optimization for the formulated objective function given in equation (8) for optimizing Total Harmonic Distortion (THD). The optimal switching angles obtained from these optimization algorithms are given in table 5. From table 6 it is confirmed that the Harris Hack Algorithm offers the best solution at a minimum number of iterations (75-iterations) compared to other algorithms of GA, PSO and WOA. Also, the THD analysis was considered at both Nyquist frequencies (generally 5kHz) and at Harmonic frequency (considered for 1kHz for eliminating up to 19th harmonic). The THD plots for voltage and current harmonics using different optimizing algorithms were presented in figure 14 and figure 15, respectively.

Table 6. Performance analysis of proposed inverter with different optimization algorithms

Algorithm	No of Iterations	% (THD)v	% (THD)i	% (THD)v	% (THD)i	V_{PEAK} (V)	V_{RMS} (V)	I_{PEAK} (A)	I_{RMS} (A)
		At Nyquist Frequency (5kHz)		At Harmonic Frequency (2kHz)					
GA	103	6.25	4.17	4.21	3.95	247.3	193.9	10.8	7.636
PSO	114	5.74	3.31	3.12	3.02	267.7	189.3	10.55	7.463
WOA	109	5.73	2.98	3.24	2.68	265.7	187.9	10.48	7.409
HHA	75	5.51	3.48	2.55	3.16	265.9	188	10.49	7.419

The magnitude of harmonic voltages from 3rd harmonic to 19th harmonics using different optimization algorithms were evaluated, and a comparison of these harmonic magnitudes was presented in figure 16. Lower dominant harmonics such as 3rd and 5th harmonics are optimized to very low values, about 0.27% and 0.26% using harris hawk optimization algorithm compared to other algorithms. Hence, the harris hawk optimizer is the better choice for the proposed multilevel objective function solution since it gives the THD of 5.51% at Nyquist frequency and 2.55 % at the harmonic frequency.

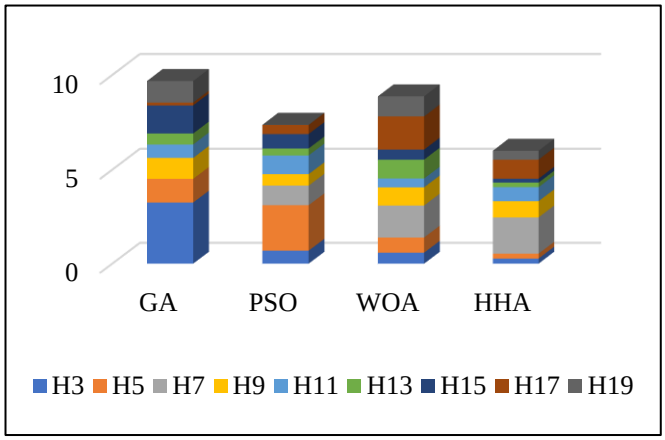


Figure 16. Comparison of Voltage Harmonic Distortion

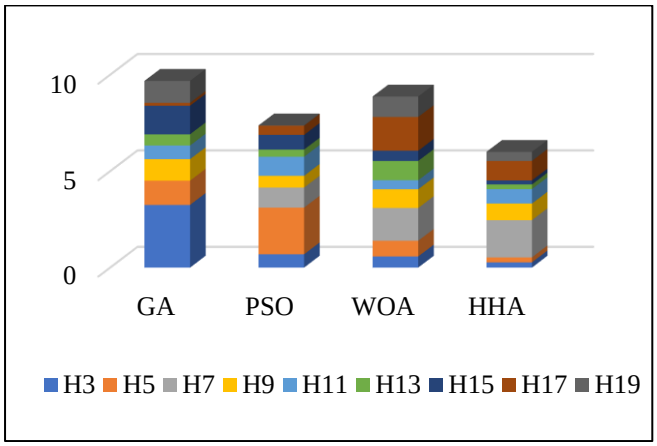


Figure 17. Comparison of Current Harmonic Distortion

The magnitude of current harmonics from 3rd harmonic to 19th harmonics using different optimization algorithms were evaluated and comparison these harmonic magnitudes were in figure 17. Lower dominant harmonics such as 3rd and 5th harmonics are optimized to very low values about 0.94% and 1.12% using whale optimization algorithms compared to other algorithms. Hence, the whale optimizer is the better choice for the proposed multilevel objective function solution while considering the current harmonics are the parameter in analysis, since it gives the THD of 2.98% at Nyquist 2.68 % at harmonic frequency.

VII. CONCLUSIONS

This article demonstrated an Asymmetric multilevel inverter that is most suited for solar PV applications. A SHEPWM using optimization algorithms was implemented using four different algorithms: GA, PSO, WOA and HHA. The main goal of using the optimization algorithms is to optimize the switching angles of the suggested topology further to optimize the THD of output. The THD obtained from these algorithms is comparatively low as per IEEE-519 standard. The proposed inverter performs well with a low THD of 5.51% at Nyquist frequency and 2.55% at harmonic frequency compared to GA, PSO and WOA. Also, the current THD using HHA is 3.48% at Nyquist frequency and 3.16% at the harmonic frequency. As per the IEEE-519 standard, the converter with THD below 5% is recommended for power system applications. As a result, according to IEEE-519 standards, the proposed inverter's performance in terms of voltage and current THD is satisfactory.

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