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Comparative power quality analysis of conventional and proposed enhanced SRF SOGI-FLL control based DSTATCOM

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ABSTRACT

This paper expresses about comparative power quality analysis in between conventional and proposed control techniques of DSTATCOM under different loading conditions. The goal of DSTATCOM is to reduce power quality problems that occur due to an unbalanced load, nonlinear load, power electronics based load, and polluted grid. The performances of DSTATCOM are different in the different control techniques. Three conventional and one proposed control techniques have been employed in the DSTATCOM. Synchronous reference frame (SRF), sliding mode control (SMC), and ADALINE based LMS control are the conventional techniques, while enhanced SRF SOGI-FLL is the proposed technique. The control techniques of DSTATCOM have been compared in terms of load balancing, power factor enhancement, DC link voltage regulation, and minimization of harmonics. These control techniques extract reference current for the PWM which generates switching pulses for the DSTATCOM. The complete H-bridge DSTATCOM system along with these control techniques have been implemented in MATLAB /Simulink platform, and, after execution, superior power quality features of proposed control technique have been investigated.

Keywords: DSTATCOM; power quality; SRF; SMC; VSC; SOGI.

INTRODUCTION

With the frequent employment of power electronics gadgets, AC distribution systems are suffering various power quality crisis (Srinivas et al., 2011; Singh et al., 2015). Major portions of loads which are used in industrial, commercial, and residential purpose are made up of power electronics based (Kumar et al., 2014).These types of loads are called as nonlinear load. Some of the examples of non-linear loads are fans, pumps, computers, and induction motors (Singh et al., 2011; Arya et al., 2016). These loads are also lagging power factor loads. There are two types of power quality problem: voltage quality and current quality (Singh et al., 2015). DSTATCOM is used to mitigate current quality problems in the distribution systems (Zaveri et al., 2012). Different topologies of three-phase four-wire based DSTATCOM have been proposed in the literature (Patnaik et al., 2013; Singh et al., 2011). Each topology has its own inherent benefits. Multilevel converters presented in the literature (Zaveri et al., 2012)

have low loss, reduced size of filter, and higher efficiency than the conventional two-level voltage source converter. Hence, in this paper, H-bridge based multilevel converter has been adopted for the DSTATCOM. H-Bridge converters not only decrease the lower order harmonics, but also have a suitable safety during the operation (Patnaik et al., 2013). Process of DSTATCOM is mostly depending on its control performance applied for reference current extraction and DC voltage regulation (Chauhan et al., 2014; Zainuri et al., 2016). In the last few decades, several researchers have emphasized to construct the proficient and vigorous control of DSTATCOM. To provide the control of DSTATCOM, many strategies have been presented in the literature such as SRF theory (Kumar et al., 2014; Singh et al., 2011), IRP theory (Zaveri et al., 2012), interpretations and modifications of IRP theory (IEEE Std. 519,2014), PB theory (Singh et al., 2015), SC theory (Singh et al., 2015), sliding mode control (Sekhar et al., 2016), ADALINE (Qasim et.al 2014; Bhattacharya et al.,2011), SOGI-MCCF(Chittora et al., 2018), and Adaptive filter (Srinivas et al., 2017). The major drawbacks of PLL in SRF technique are its digital implementation in circuits, large calculation time, being less proficient for correcting voltage distortion, voltage frequency deviation, and so on (Golestan et al., 2017). The foremost problem of sliding mode control (SMC) technique is to design the sliding surface in dynamic system. It has been seen that if surface design is not proper in dynamic circumstance, it will result in unsatisfactory performance. Hence in this work, conventional PLL of SRF has been replaced by SOGI-FLL and developed a novel control philosophy of enhanced SRF SOGI-FLL for the DSTATCOM. SOGI-FLL synchronizes the frequency and phase angle of the grid with power inverter in less time (Hao et al., 2017). This paper also compared the power quality performances of enhanced SRF SOGI-FLL with the other techniques used in the literature. The paper has been separated in divisions. First division illustrates the Introduction of the work in which literature survey and novelty of the work has been included. In division 2, circuit configuration of the three-phase four-wire H-bridge based DSTATCOM system has been presented. In division 3, various conventional control schemes with their mathematical modeling have been elaborated. In segment 4, the discussions about proposed enhance SRF SOGI-FLL control scheme have been mentioned. Part 5 deals with the results in which performances of DSTATCOM under various loading conditions have been discussed. At last, section 6 concludes the paper.

H-BRIDGE DSTATCOM

Figure 1illustrates the circuit arrangement of three-phase H-bridge DSTATCOM attached to the distribution system. The point on the distribution system at which H-bridge DSTATCOM is bonded is known as point of common coupling (PCC). I_{sa},I_{sb}, and I_{sc} represent current from the three phase AC mains. I_{La},I_{Lb},I_{Lc} represent current from the load side. The parameters $R_s$and L_s are the resistance and inductance of the AC mains. I_c and $V_c$denote the injected current and voltage, respectively, by the DSTATCOM. $V_{dc}$is the interior voltage of DC connect capacitor of voltage source inverter. The r ipple filter represented as R_f and $C_f$is fixed at PCC and shunted with the load. The 12 no. of IGBT/diode based switches from three H-bridges VSI (Patnaik et al., 2013). Control algorithms have conventional techniques such as SRF, SMC, and ADALINE LMS as well as proposed enhance SRF SOGI-FLL technique. The purpose of hysteresis current controller is to afford switching signal for VSI valves.

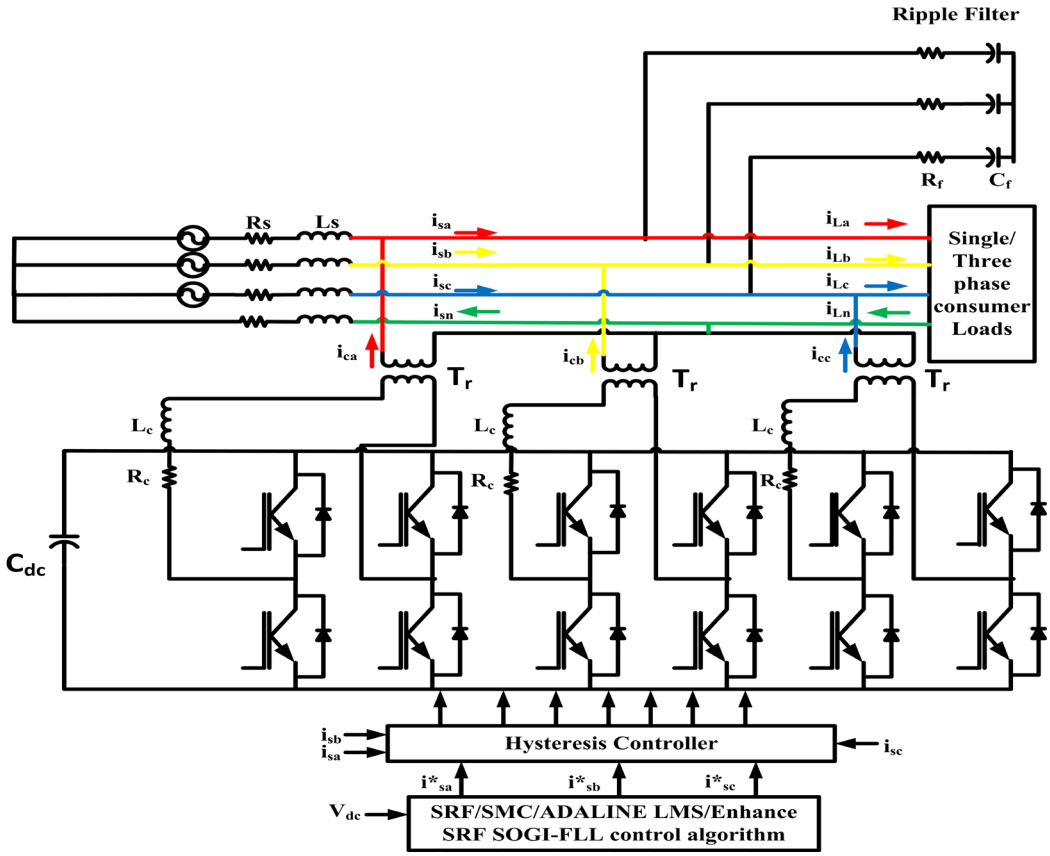

Figure 1. Test system based on three-phase H-bridge DSTATCOM.

CONTROL PERFORMANCES

To generate the switching signals for the VSI switches of H-bridge DSTATCOM, control performances such as SRF, SMC, ADALINELMS, and proposed enhance SRF SOGI-FLL technique have been adopted. The discussions about the above control performances are below.

SYNCHRONOUS REFERENCE FRAME THEORY

SRF generates the three-phase reference source current signal which is compared with the actual three-phase source current. PWM generator gives pulses from three-phase error source current signal. The input signals for the SRF are three-phase PCC voltage, three-phase load current (sensed from distribution system), and DC link voltage (sensed from VSI). Firstly, three-phase stationary signal is translated into corresponding synchronously rotating d-q-o signal by Clarke transformation, and then low pass filter is employed for extorting ripples. The PCC voltage signals are passed by three-phase PLL in order to generate sine and cosine signals for Clarke transformation and inverse Clarke transformation (Singh et al., 2015). On DC bus, PI controller produces I_{loss} component. On AC bus, PI controller produces I_{QDSTAT} component.

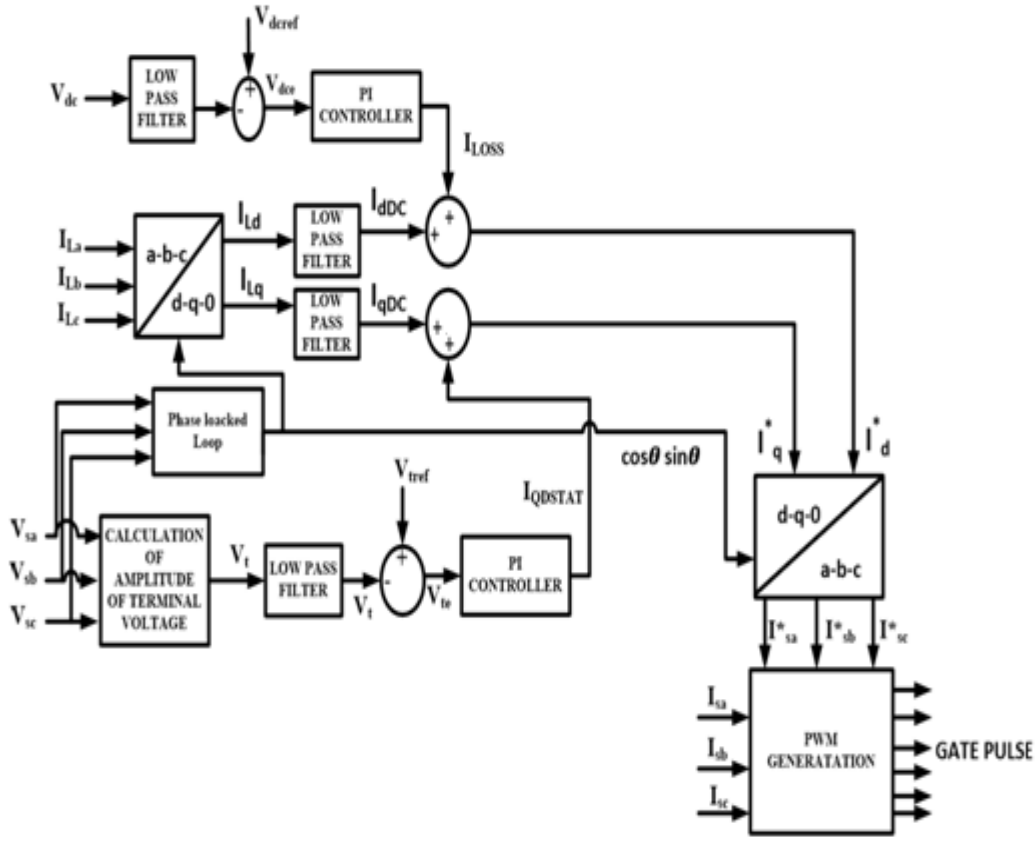

Figure 2. Building block of synchronous reference frame.

The reference d-q current is given by

$$I_d^* = I_{dDC} + I_{loss}$$

$$I_q^* = I_{qDC} + I_{QDSTAT} \quad (1)$$

The inverse Clarke transformation converts reference (d-q-0) current into reference (a-b-c) current. The detail discussion on synchronous reference frame has been depicted in Figure 2.

SLIDING MODE CONTROL

Sliding mode controller provides the vigorous control in transient states and the quick active reaction in overshoot and undershoots of DC-link voltage of VSI during load variation/transient state (Sekhar et al., 2016). Figure 3 demonstrates the block diagram of sliding surface design.

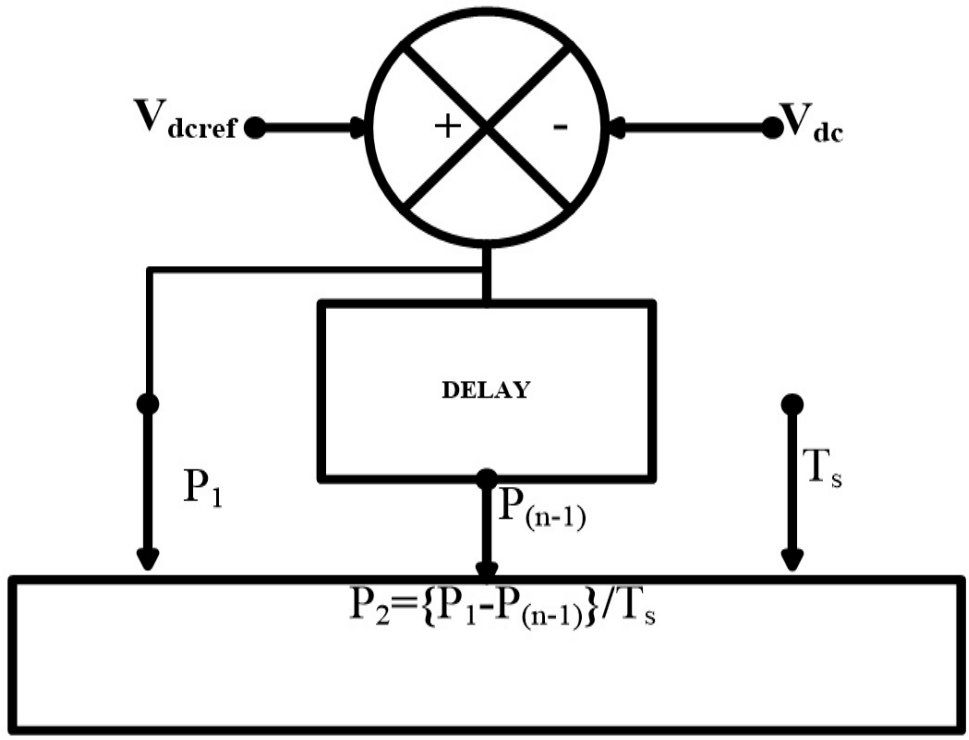

Figure 3. Block diagram of sliding regime.

Calculation of In-phase current is I_{saref}.

Actual DC voltage =V_{dc}.

Reference DC voltage =V_{dcref}.

Step 1 is sliding Surface Design (Sekhar et al., 2016)

The LPF filtered actual V_{dc}, and this is compared with reference DC voltage

$$P_1 = V_{dcref} - V_{dc} \tag{2}$$

P_1=Error signal of reference and actual DC voltage
Step 2 is clauses of the sliding regime
Taking the derivative of Equation (2),

$$P_2 = \dot{P_1} = \frac{1}{T_S}\left(P_1 - P_{(n-1)}\right) \tag{3}$$

P_2=State variable and the derivative of error
Step 3 is control law (Figure 4).

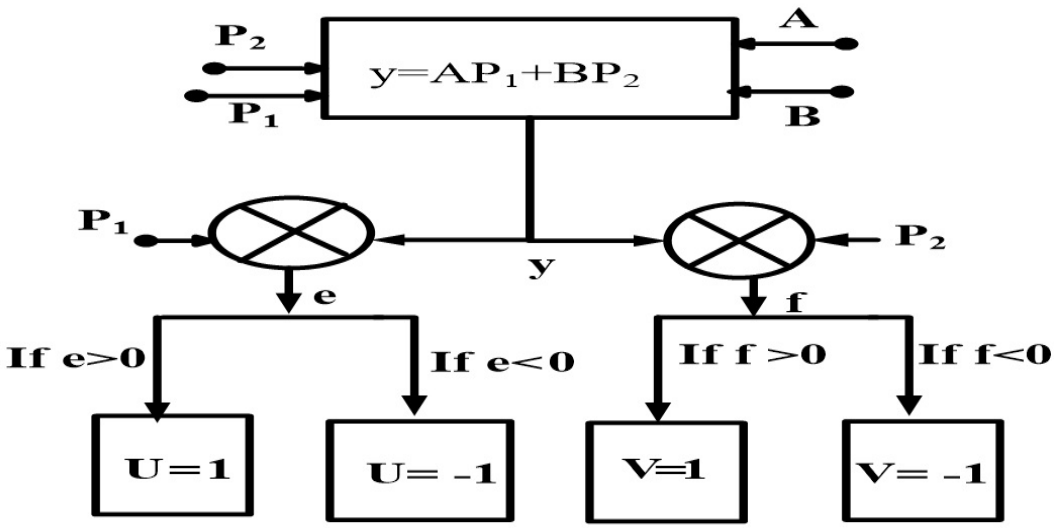

Figure 4. Block diagram of control law.

Now, the switching constraints u and v are selected with the help of slope of DC link voltage error

$$u = \begin{cases} +1, & y_{P1} > 0 \\ -1, & y_{P1} < 0 \end{cases} \tag{4}$$

$$v = \begin{cases} +1, & y_{P2} > 0 \\ -1, & y_{P2} < 0 \end{cases} \tag{5}$$

Now, the reference DC currents are

$$I_{dcref} = CP_1 u + DP_2 v \tag{6}$$

$$y = AP_1 + BP_2 \tag{7}$$

where y= switching hyper plane function.

A, B, C, and D are the SMC constants.

Instantaneous amplitude of PCC voltage is as follows:

$$V_t = \sqrt{2\frac{\{V_a^2 + V_b^2 + V_c^2\}}{3}} \tag{8}$$

In- phase component of unit templates is

$$U_{sap} = {}^{V_a}/_{V_t} \tag{9}$$

$$U_{sbp} = {V_b}/{V_t} \tag{10}$$

$$U_{scp} = {V_c}/{V_t} \tag{11}$$

Now, the quadrature component of unit templates is

$$U_{saq} = {\left(-U_{sbp} + U_{scp}\right)}/{\sqrt{3}} \tag{12}$$

$$U_{sbq} = {\left(U_{sap}\sqrt{3} + U_{sbp} - U_{scp}\right)}/{2} \tag{13}$$

$$U_{scq} = {\left(-U_{sap}\sqrt{3} + U_{sbp} - U_{scp}\right)}/{2} \tag{14}$$

Now, the reference In-phase component of active power of source current is

$$I^*_{sap} = I_{dcref} U_{sap} \tag{15}$$

$$I^*_{sbp} = I_{dcref} U_{sbp} \tag{16}$$

$$I^*_{scp} = I_{dcref} U_{scp} \tag{17}$$

The error in PCC voltage was evaluated as

$$V_{ace} = V^*_t - V_t \tag{18}$$

The PI controller creates output for keeping PCC voltage at reference value

$$I_{acref}(k) = I_{acref}(k-1) + K_{pa}\{V_{ace}(k) + V_{ace}(k-1)\} + K_{ia} V_{ace}(k) \tag{19}$$

Where

$V_{ace}(k)$ =Kth time voltage error,
$V_{ace}(k-1)$ = (K-1)th time voltage error,
K_{pa}= Proportional gain of PI controller, and K_{ia} =Integral gain of PI controller

Now, the reference quadrature-phase component of source current is

$$I^*_{saq} = I_{acref} U_{saq} \quad (20)$$

$$I^*_{sbq} = I_{acref} U_{sbq} \quad (21)$$

$$I^*_{scq} = I_{acref} U_{scq} \quad (22)$$

The total three-phase reference source current is the addition of In-phase and quadrature phase component as follows:

$$I^*_{Sa} = I^*_{Sap} + I^*_{Saq} \quad (23)$$

$$I^*_{Sb} = I^*_{Sbp} + I^*_{Sbq} \quad (24)$$

$$I^*_{Sc} = I^*_{Scp} + I^*_{Scq} \quad (25)$$

ADALINELMS CONTROL

Step 1. Calculation of in-phase and quadrature phase component of unit vector

$V_a, V_{b,} V_c$ are three-phase PCC voltages. First, it is sensed and filtered.

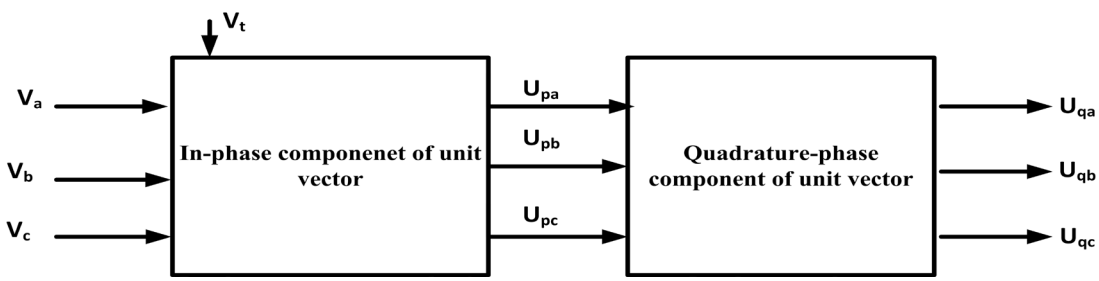

Figure 5. In-phase and q-phase of unit vector.

Amplitude of the terminal voltage V_t is obtained from Equation 8.
In-phase component of unit vector:

U_{ap}, U_{bp}, U_{cp} are obtained from Equations 9, 10,and11, respectively by putting the respective values of PCC voltages.

Quadrature component of Unit vector:
U_{aq}, U_{bq}, and $U_{cq}$are obtained from Equations 12, 13, and 14, respectively.

Step 2. Calculation of $Z_L(k)$ which is a part of d-axis component

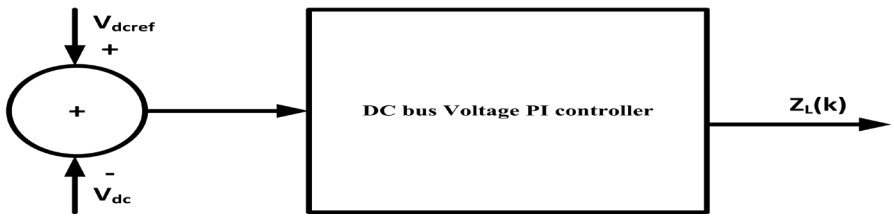

Figure 6. Calculation of $Z_L(k)$.

$$V_{dce}(k) = V_{dcref}(k) - V_{dc}(k) \tag{26}$$

$$Z_L(k) = Z_L + k_{pd}\{V_{dce}(k) - V_{dce}(k-1\} + k_{id}V_{dce}(k) \tag{27}$$

where$Z_L(k)$ is the part of the d-axis component of supply current. k_{pd}andk_{id} are the proportional and integral constants of DC bus voltage**.**

Step 3. Calculation of Z_{qv} which is the part of q-axis component

Voltage error of the AC voltage at the k[th] sampling instant is

$$V_{te}(k) = V_t(k) - V_{tr}(k) \tag{28}$$

$$Z_{qv}(k) = Z_{qv}(k-1) + k_{pa}\{V_{te}(k) - V_{te}(k-1) + k_{ia}V_{te}(k)\} \tag{29}$$

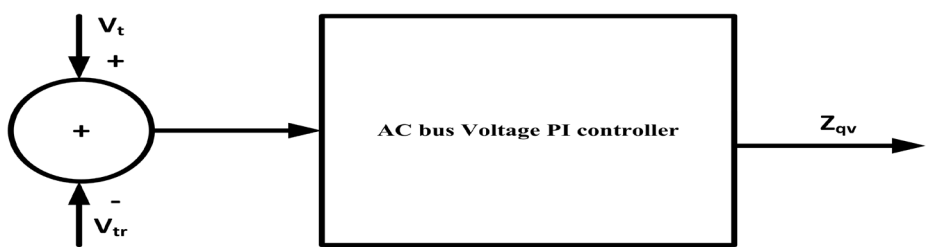

Figure 7. Calculation of Z_{qv} .

$k_{pa}$and k_{ia} are the proportional and integral constants of AC voltage controller

Step 4. Calculation of weight of the d-axis component of three-phase load current

Weight of the fundamental d-axis component (I_d) utilizes LMS control algorithm and its training through ADALINE neural network control algorithm (Singh et al., 2015):

$$Z_{ap}(\mathrm{k})=\{Z_{ap}(k-1)+\epsilon(I_{La}(k)-Z_{ap}(k-1)U_{ap}\}U_{ap}(k) \quad (30)$$

$$Z_{bp}(\mathrm{k})=\{Z_{bp}(k-1)+\epsilon(I_{Lb}(k)-Z_{bp}(k-1)U_{bp}\}U_{bp}(k) \quad (31)$$

$$Z_{cp}(\mathrm{k})=\{Z_{cp}(k-1)+\epsilon(I_{Lc}(k)-Z_{cp}(k-1)U_{cp}\}U_{cp}(k) \quad (32)$$

Z_{ap}, Z_{bp}, Z_{pc} are the weights of active power component of fundamental d-axis current.

Hence, the average weight of fundamental d-axis component of reference supply current is

$$Z_P(k) = (1 / 3)\,[Z_{ap}\,(k) + Z_{bp}\,(k) + Z_{cp}\,(k) + Z_L] \quad (33)$$

Z_L =Output of DC bus voltage controller, and ϵ=convergence factor (value taken 0.01)

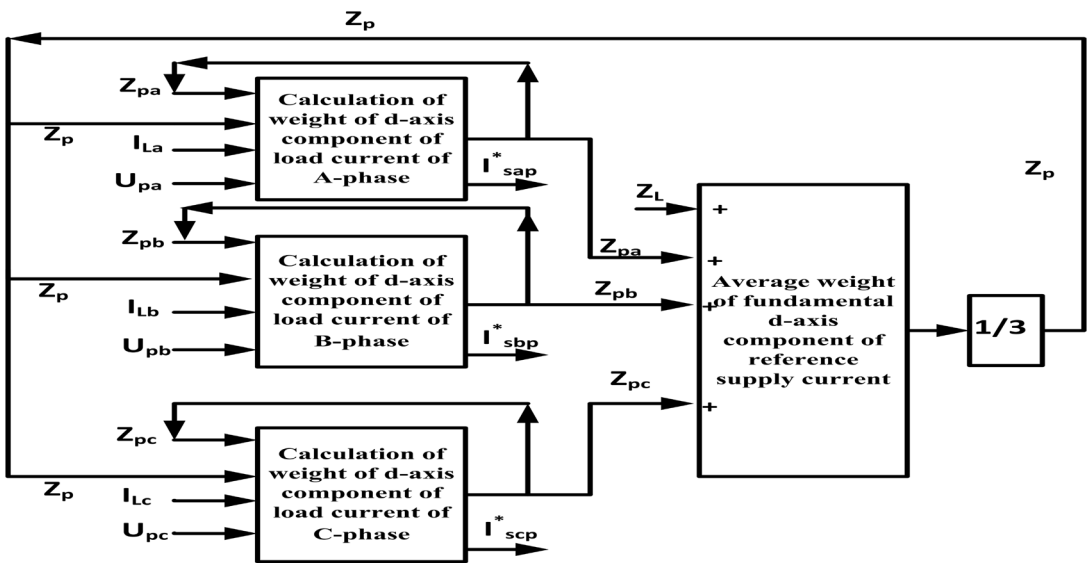

Figure 8. Calculation of $Z_p(k)$.

Fundamental reference d-axis (I_d) supply current

$$I^*_{sap} = Z_p U_{ap}, I^*_{sbp} = Z_p U_{bp}, I^*_{scp} = Z_p U_{cp} \quad (34)$$

Step 5. Calculation of Weights of Reactive Power Component of Load Current and Reference Supply Current of Reactive Component of Reference Supply Current is as Follows.

Estimation of weight of the fundamental q- axis component (Iq) utilizes LMS control algorithm and its training through ADALINE neural network control algorithm (Singh et al., 2015):

$$Z_{aq}(\mathrm{k})=\{Z_{aq}(k-1)+\epsilon(I_{La}(k)-Z_{aq}(k-1)U_{aq}\}U_{aq}(k) \tag{35}$$

$$Z_{bq}(\mathrm{k})=\{Z_{bq}(k-1)+\epsilon(I_{Lb}(k)-Z_{bq}(k-1)U_{bq}\}U_{bq}(k) \tag{36}$$

$$Z_{cq}(\mathrm{k})=\{Z_{cq}(k-1)+\epsilon(I_{Lc}(k)-Z_{cq}(k-1)U_{cq}\}U_{cq}(k) \tag{37}$$

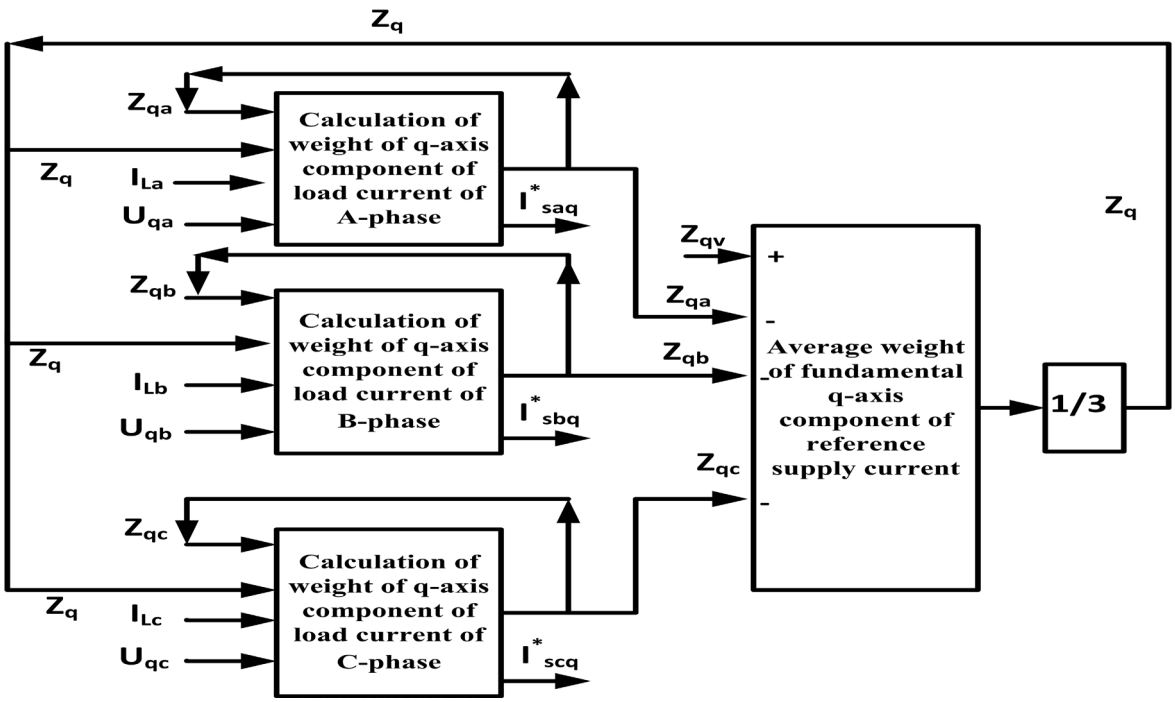

Figure 9. Calculation of $Z_q(k)$.

Z_{aq}, Z_{bq}, Z_{cq} are the weights of active power component of fundamental d-axis current. Hence, average weight of reference reactive power component of supply current is

$$Z_q(k) = [Z_{qv}(k) - \{Z_{qa}(k) + Z_{qb} + Z_{qc}(k)\}]/3 \tag{38}$$

Z_{qv} =Output of AC bus voltage controller

Fundamental reference q-axis (I_q) supply current is

$$I^*_{saq} = Z_q U_{aq}, I^*_{sbq} = Z_q U_{bq}\,, I^*_{scq} = Z_p U_{cq} \tag{39}$$

Step 6: Generation of PWM signals

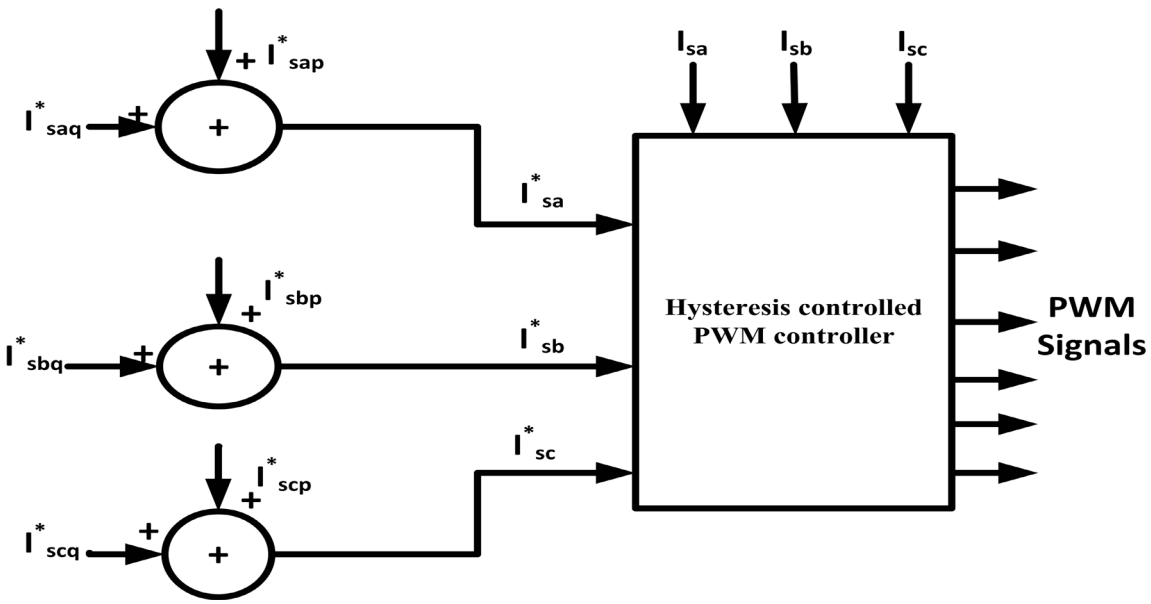

Figure 10. Generation of PWM signals.

The three-phase reference supply current is

$$I_{sa}^{*} = I_{sap}^{*} + I_{saq}^{*} \tag{40}$$

$$I_{sb}^{*} = I_{sbp}^{*} + I_{sbq}^{*} \tag{41}$$

$$I_{sc}^{*} = I_{scp}^{*} + I_{scq}^{*} \tag{42}$$

These calculated reference supply currents $(I_{sa}^{*}, I_{sb}^{*}, I_{sc}^{*})$ are compared with the sensed supply currents (I_{sa}, I_{sb}, I_{sc}) to achieve current error which produce gating signal pulses for VSI switches of DSTATCOM.

PROPOSED ENHANCED SRF SOGI-FLL

Here, SRF without PLL has been employed in the DSTATCOM. SOGI-FLL has been adopted for synchronizing the signal (Cespedes et al., 2014). In this novel control algorithm, conventional PLL has been replaced by the SOGI-FLL. SOGI-FLL has faster reaction, less computational time, and better response in eliminating power quality issues present in the nonideal grid (Hao et al., 2017; Arya et al., 2020).

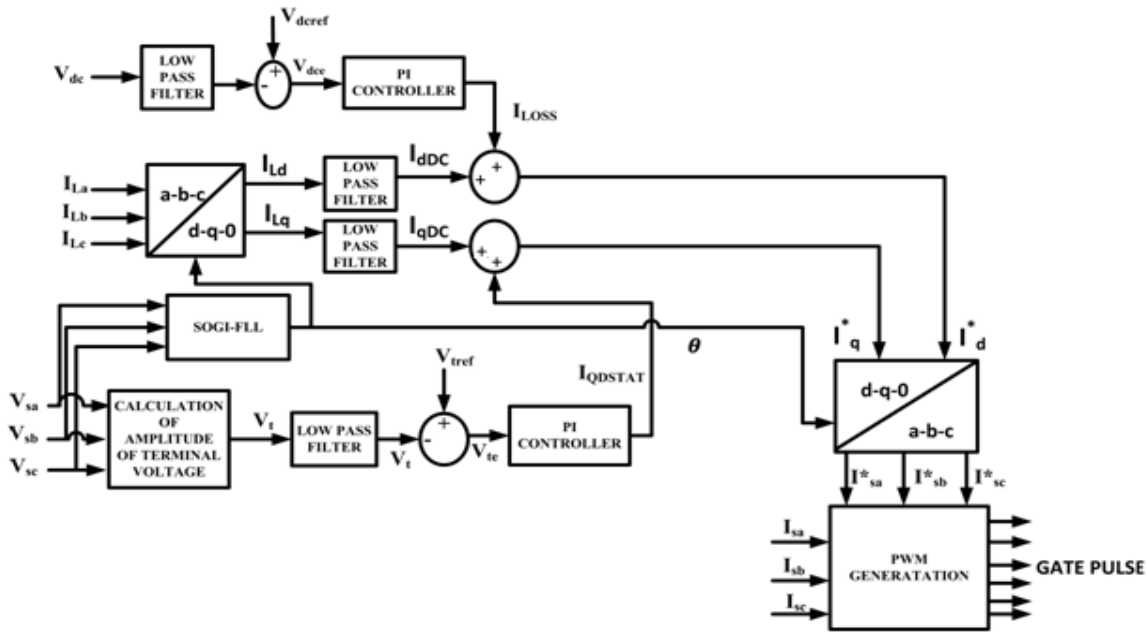

Figure 11. Enhanced SRF SOGI-FLL controller.

The SOGI-FLL methods have suitable steady-state and dynamic performance even if the system has varied its frequency and phase in a specified interval of time due to the impact of nonlinear load. In the below section, mathematical modeling of controller is designed.

MATHEMATICAL MODELING OF STANDARD SOGI-FLL

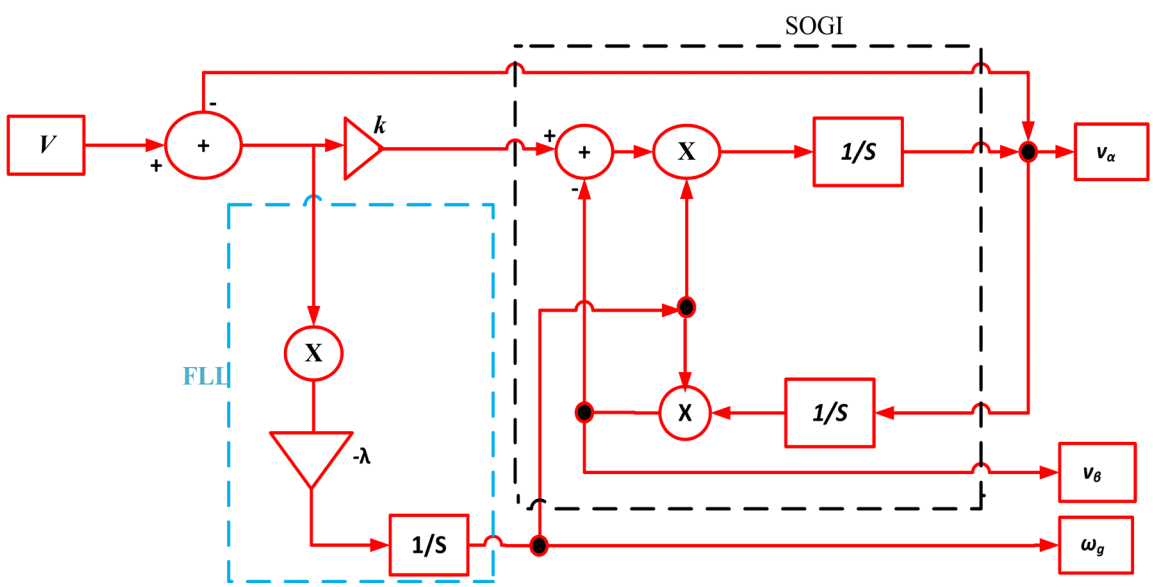

Figure 12. Standard SOGI-FLL.

Figure 12 shows the block diagram of SOGI-FLL. $v_\alpha$is the single phase input signal. $\widehat{v_\alpha}$and$\widehat{v_\beta}$ are the in-phase and quadrature-phase input signal of v_α , respectively. $\hat{v}$,ω_g, and θ are the amplitude, frequency, and phase angle of input signal. The output of SOGI-FLL is the phase angle θ which has been utilized in a-b-c to d-q-0 and d-q-0 to a-b-c transformation of figure 11. K and λ are the gain of SOGI and FLL, respectively. Output signals of the SOGI-FLL are represented by $v_\alpha(s)$ and $v_\beta(s)$

$$\widehat{v_\alpha}(s) = \frac{K\widehat{\omega_g}s}{s^2+K\widehat{\omega_g}s+\hat{\omega}_g^2 s} v(s) \tag{43}$$

$$\widehat{v_\beta}(s) = \frac{k\widehat{\omega_g^2}}{s^2+K\widehat{\omega_g}s+\hat{\omega}_g^2 s} v(s) \tag{44}$$

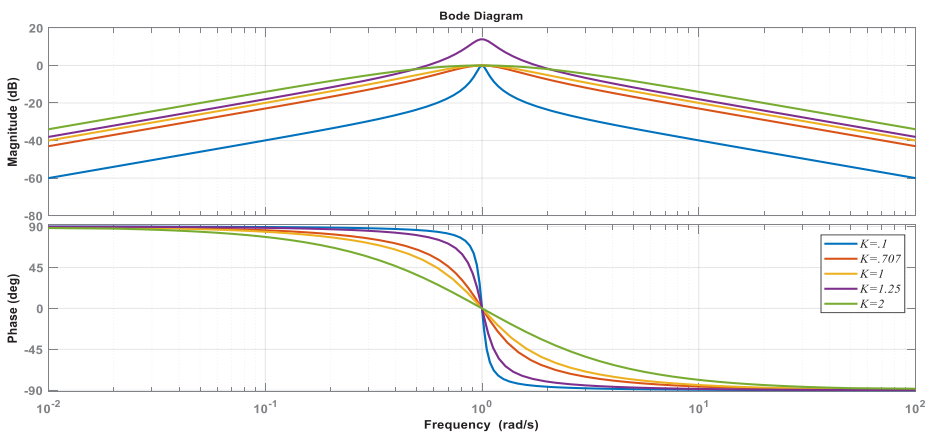

Figure 13. Frequency response of $v_\alpha(s)$.

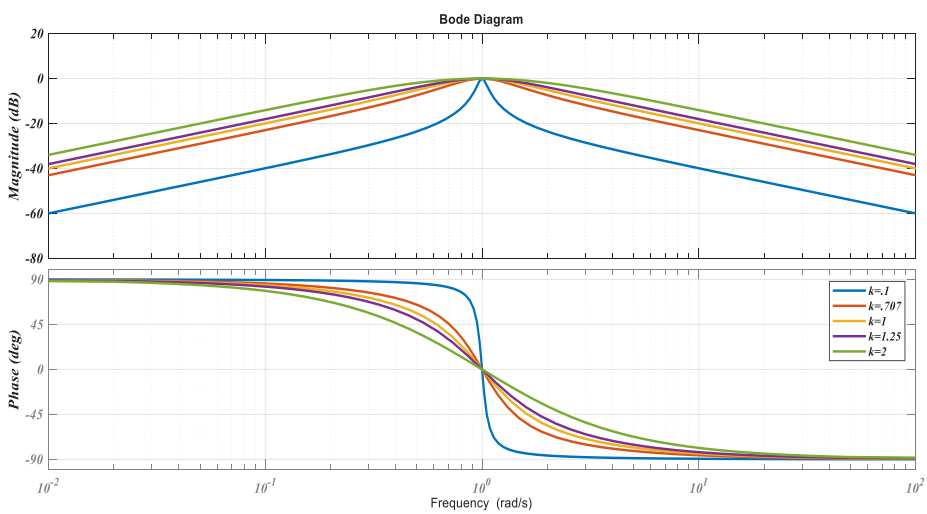

Figure 14. Frequency response of $v_\beta(s)$.

Figures 13 and 14 show the frequency response of $\widehat{v_\alpha}(s)$ and $\widehat{v_\beta}(s)$ for different values of k, respectively.

DYNAMICS OF SOGI-FLL

Initially taking the supply voltage V_s is free from harmonic distortion

$$v(t) = v_\alpha(t) = v\cos(\omega_g t + \varphi) \tag{45}$$

Take $\omega_g t + \varphi = \theta$.

Output of the SOGI for d-axis and q-axis becomes

$$\widehat{v_\alpha}(t) = \hat{V}\cos\hat{\theta} \tag{46}$$

$$\widehat{v_\beta}(t) = \hat{V}\sin\hat{\theta} \tag{47}$$

$\hat{v}$ and $\hat{\theta}$ are the amplitude and phase angle of input supply voltage, respectively. Assuming SOGI-FLL is in-quasi locked state, $\hat{v} \cong v$,$\hat{\theta} \cong \theta$. In the steady state, they are very close to v and θ, respectively. This is the basic linearization concept of FLL.

Differential equation obtained from figure

$$\dot{\widehat{v_\alpha}} = \widehat{\omega_g}[k(v_\alpha - \widehat{v_\alpha}) - \widehat{v_\beta}] \tag{48}$$

$$\dot{\widehat{v_\beta}} = \widehat{\omega_g}\widehat{v_\alpha} \tag{49}$$

$$\dot{\widehat{\omega_g}} = -\frac{\lambda}{v^2}(v_\alpha - \widehat{v_\alpha})\widehat{v_\beta} \tag{50}$$

Substituting the value of $v_\alpha$and $\widehat{v_\alpha}$,

$$\dot{\widehat{\omega_g}} = \frac{\lambda}{v^2}[v\cos\theta - \hat{v}\cos\hat{\theta}]\sin\hat{\theta} \tag{51}$$

$$= \frac{\lambda}{2v}[v\sin(\theta - \widehat{\theta}) + \hat{v}\sin\widehat{2\theta} - v\sin(\hat{\theta} + \theta) \tag{52}$$

Assume $\sin(\theta - \widehat{\theta}) \cong (\theta - \widehat{\theta}),\ \hat{v}\sin\widehat{2\theta} - v\sin(\hat{\theta} + \theta) \cong 0$

From the above assumption, the equation becomes

$$= \frac{\lambda}{2v}[v(\theta - \widehat{\theta}] \tag{53}$$

$$= \frac{\lambda}{2}[(\theta - \hat{\theta}] \tag{54}$$

Phase angle $\hat{\theta}$ determined from SOGI-FLL structure is

$$\hat{\theta} = \tan^{-1}\frac{v_\beta}{v_\alpha} \tag{55}$$

Differentiating w.r.t. time yields $\dot{\hat{\theta}} = \frac{v_\alpha \dot{\hat{v_\beta}} - \dot{\hat{v_\alpha}} v_\beta}{\hat{v_\alpha^2} + \hat{v_\beta^2}}$

$$\dot{\hat{\theta}} = \frac{v_\alpha \dot{\hat{v_\beta}} - \dot{\hat{v_\alpha}} v_\beta}{\hat{V}^2} \tag{56}$$

Consider $\hat{v_\alpha^2} + \hat{v_\beta^2} = \hat{V}^2$

Substitute the value of $v_\alpha$and v_β in Equation (56)

$\dot{\hat{\theta}} = \frac{(\hat{v}_\alpha^2 + \hat{v}_\beta^2)\hat{\omega_g} - k\hat{\omega_g}(v_\alpha - \hat{v_\alpha})\hat{v_\beta}}{\hat{V}^2}$

Consider $(v_\alpha - \hat{v_\alpha})\hat{v_\beta} = {-\dot{\hat{\omega_g}}\dot{\hat{V}^2}}/{\lambda}$

$$\dot{\hat{\omega_g}} = \omega_g + (\frac{k\hat{\omega}_g}{\lambda})\dot{\hat{\omega_g}} \tag{57}$$

Coefficient of $\frac{k\hat{\omega}_g}{\lambda}$i.e.$\dot{\hat{\omega_g}}$is grid frequency which is time dependent parameter. So, Laplace transform of Equation (57) is not possible. Hence, the linear model estimated coefficient of time dependent frequency is approximated to its nominal value

$$\dot{\hat{\omega_g}} = \omega_g + (\frac{k\hat{\omega}_n}{\lambda})\dot{\hat{\omega_g}} \tag{58}$$

Now, from the figure, estimated amplitude for supply voltage

$$\hat{V} = \sqrt{\hat{v}_\alpha^2 + \hat{v}_\beta^2} \tag{59}$$

Differentiating the above equation, w.r.t time yields

$$\dot{\hat{V}} = \frac{\hat{v_\alpha}\dot{\hat{v_\alpha}} + \hat{v_\beta}\dot{\hat{v_\beta}}}{\sqrt{v_\alpha^2 + \hat{v}_\beta^2}}$$

$$\dot{\hat{V}} = \frac{\hat{v_\alpha}\dot{\hat{v_\alpha}} + \hat{v_\beta}\dot{\hat{v_\beta}}}{\hat{V}} \tag{60}$$

Put the value of $\hat{v_\alpha}$ and $\hat{v_\beta}$ in Equation (60)

$$\dot{\hat{V}} = \frac{k\omega_g(v_\alpha - \hat{v}_\alpha)\hat{V}_\alpha}{\hat{V}}$$

$$\dot{\hat{V}} = \frac{k\omega_g[V\cos\theta - \hat{V}\cos\hat{\theta}]\hat{V}\cos\hat{\theta}}{\hat{V}} \tag{61}$$

$$= \frac{k\omega_g}{2}\{V\cos(\theta - \hat{\theta}) + \{V\cos(\theta + \hat{\theta}) - \hat{V}\cos(2\hat{\theta}) - \hat{V}\} \tag{62}$$

Consider $\cos(\theta - \hat{\theta}) = 1, V\cos(\theta + \widehat{\theta}) - \hat{V}\cos 2\hat{\theta} = 0$

$$\hat{V} \cong \frac{k\omega_g}{2}(V - \hat{V}) \tag{63}$$

Coefficient of $\frac{k}{2}$ i.e. ω_g is grid frequency which is time dependent parameter. So, Laplace transform of Equation (63) is not possible. the linear model estimated coefficient of time dependent frequency is approximated to its nominal value

$$\hat{V} \cong \frac{k\omega_n}{2}(V - \hat{V}) \tag{64}$$

Based on the above linearization model, approximated magnitudes of supply voltage, phase angle, and angular frequency are obtained as

$$\hat{V}(s) = \frac{{}^{k\omega_n}/_2}{s + {}^{k\omega_n}/_2}V(s) \tag{65}$$

$$\hat{\theta}(s) = \frac{({}^{k\omega_n}/_2)s + {}^{\lambda}/_2}{s^2 + ({}^{k\omega_n}/_2)s + {}^{\lambda}/_2}\theta(s) \tag{66}$$

$$\widehat{\omega_g}(s) = \frac{{}^{\lambda}/_2}{s^2 + ({}^{k\omega_n}/_2)s + {}^{\lambda}/_2}\omega_g(s) \tag{67}$$

MODELING OF TUNING PARAMETERS

Characteristics equation obtained from Equation (67)

$$= s^2 + ({}^{k\omega_n}/_2)s + {}^{\lambda}/_2 \tag{68}$$

The generalized form of characteristics equation for second-order system is

$$S^2 + 2\epsilon\omega_{n"}s + \omega_{n"}^2 \tag{69}$$

On comparing Equations (68) and (69)

$2\varepsilon\omega_{n''} = {k\omega_n}/{2}$, where ϵ=damping factor, $\omega_{n''}^2 = {\lambda}/{2}$, where $\omega_{n''}$=natural frequency, ω_n=nominal value of grid frequency.

Consequently, only two values k and λ i.e. SOGI gain and FLL gain are optimized to the best value so that the optimum tradeoff between settling time and overshoot will occur (Hao et al., 2017; Wen et al., 2016). From frequency response of in-phase and quadrature-phase supply voltage, it is quite clear that ϵ= 0.707(or $1/\sqrt{2}$) gives the best tradeoff between settling time and overshoot. So ϵ= 0.707(or $1/\sqrt{2}$) is considered. One can see that

$\omega_{n''}^2 = {\lambda}/{2}$, $\lambda = 2\omega_{n''}^2$

$$\omega_{n''} = {k\omega_n}/{4\varepsilon} \tag{70}$$

$$\lambda = \frac{k^2\omega_n^2}{8\epsilon^2} \tag{71}$$

Put $\epsilon = 1/\sqrt{2}$

$$\lambda = \frac{k^2\omega_n^2}{4} \tag{72}$$

From Equation (72), it is quite obvious that k and λ are in relation with each other. In this work, we have taken $k = 1/\sqrt{2}, \lambda = 12337$.

Table 1. SOGI Parameters.

Parameters	Value
SOGI gain, k	$1/\sqrt{2}$
FLL gain,λ	12337
Frequency	50Hz
Nominal angular frequencyω_n	$2\pi 50$rad/sec

RESULTS AND DISCUSSIONS

The three H-bridge inverter based DSTATCOM under synchronous reference frame, sliding mode control, ADALINE LMS, and proposed enhanced SRF SOGI FLL has been modeled in MATLAB/Simulink. MATLAB 2018a version has been employed to model the simulation with Ode23t solver. Simulation time of 1.6s has been considered for the dynamic result for all controllers. After execution, the following observations are analyzed.

Compensation Behavior of DSTATCOM Under Dynamic Load Condition from [0-0.4]s

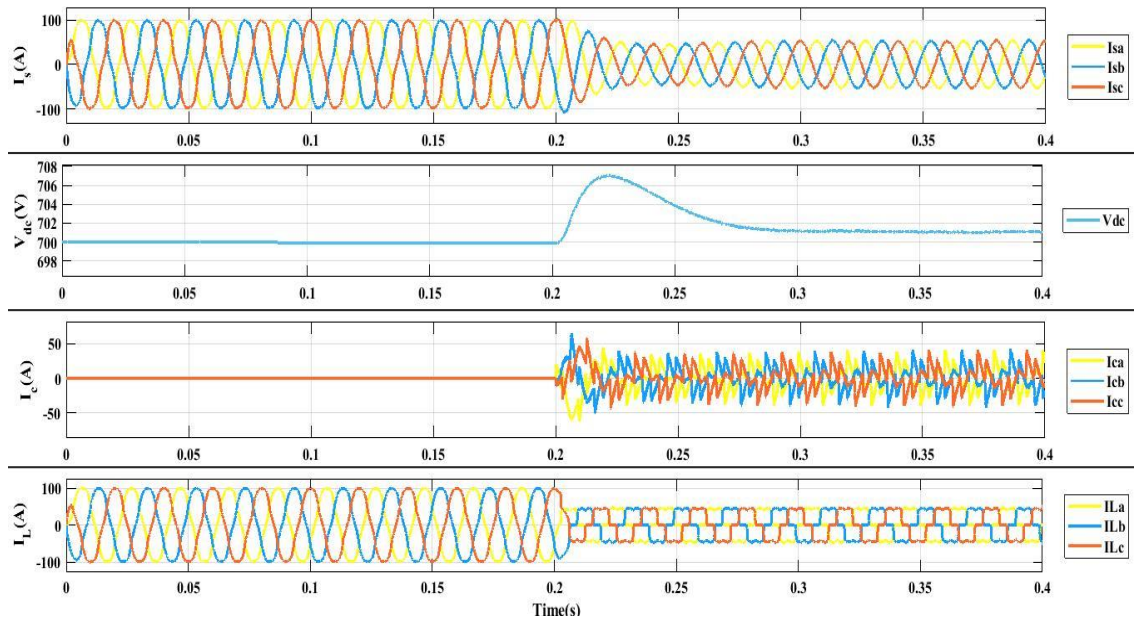

Figure 15. Performance of DSTATCOM under SRF controller.

Simulation results of DSTATCOM with the above four control techniques are certified using MATLAB/SIMULINK. The results have been observed under various loading conditions such as linear, nonlinear, unbalanced, and so on.

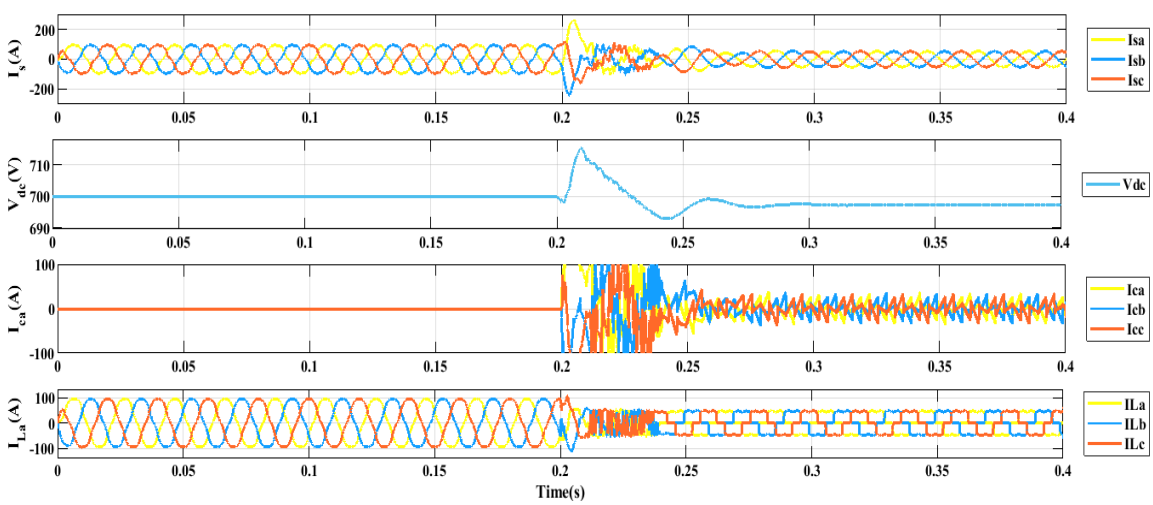

Figure 16. Performance of DSTATCOM under sliding mode controller.

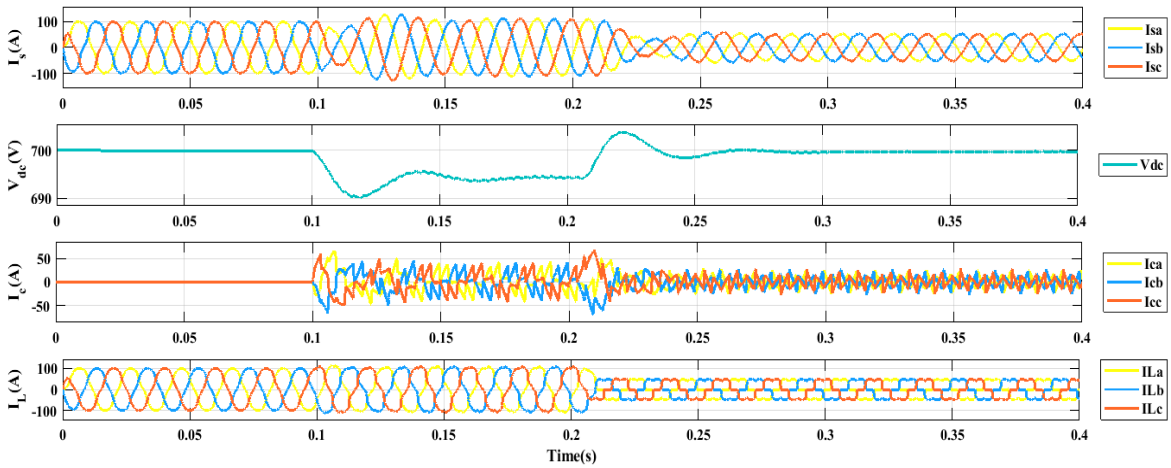

Figure 17. Performance of DSTATCOM under ADALINE LMS controller.

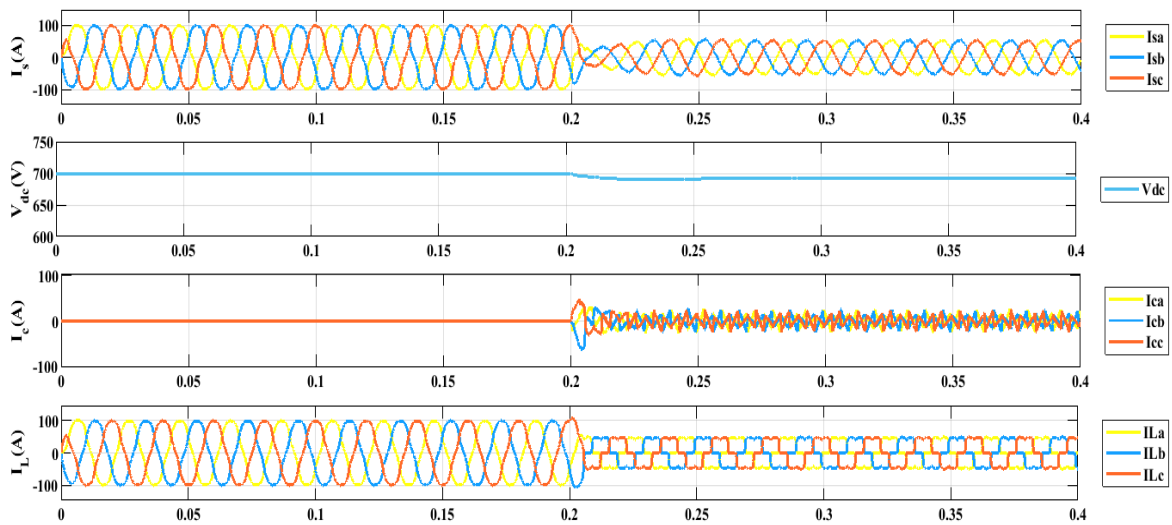

Figure 18. Performance of DSTATCOM under proposed enhanced SRF SOGI-FLL.

The DSTATCOM is in uncompensated mode during t = [0s - 0.2s] and, after, at t=0.2s, DSTATCOM comes into operation. Figs. 15 to 18 represent the performance evaluation of source current, DC capacitor voltage, DSTATCOM current, and load current by SRF, SMC, ADALINE LMS, and proposed enhanced SRF SOGI-FLL controller, respectively. In the above figures, when DSTATCOM is in operation, the waveforms of source current become sinusoidal. Load current I_L is nonsinusoidal throughout the period and contains the odd and even harmonics. Due to transient in the system, the DC voltage regulations of 700V have been achieved at different times for each controller. In SRF, SMC, ADALINE LMS, and proposed enhanced SRFSOGI-FLL controller, DC voltage regulation occurs at t=0.31s, 0.28s, 0.25s, and 0.21s, respectively. This indicates that DC voltage regulates fast in proposed enhanced SRF SOGI-FLL controller.

Compensation Behavior of DSTATCOM Under Dynamic Load Condition from [0.4-1]s

In this section, dynamic behaviors of DSTATCOM have been performed during t= [0.4s-1s]. Nonlinear and unbalanced linear load have been considered to observe compensation performance of DSTATCOM with its several control techniques. Figs. 19 to 22 represent the performance evaluation of DSTATCOM by SRF, SMC, ADALINE LMS, and proposed enhanced SRF SOGI-FLL controller, respectively. During the interval t = [0.4s-0.6s], only linear load has been applied, interval t= [0.6s-0.9s] only nonlinear load has been inserted, and interval t = [0.9s-1s] again nonlinear load has been disconnected, and only linear load has been connected. During t= [0.4s-0.6s], load current and source current are sinusoidal. In interval t=[0.6s-0.9s], load current is nonsinusoidal due to insertion of nonlinear load, and source current is sinusoidal due to compensation effect of DSTATCOM. DC voltage regulation occurs at approximately 700V, but, during insertion and removal of loads, a huge increase in magnitude of capacitor voltage occurs in the three controllers except proposed enhanced SRF SOGI-FLL controller.

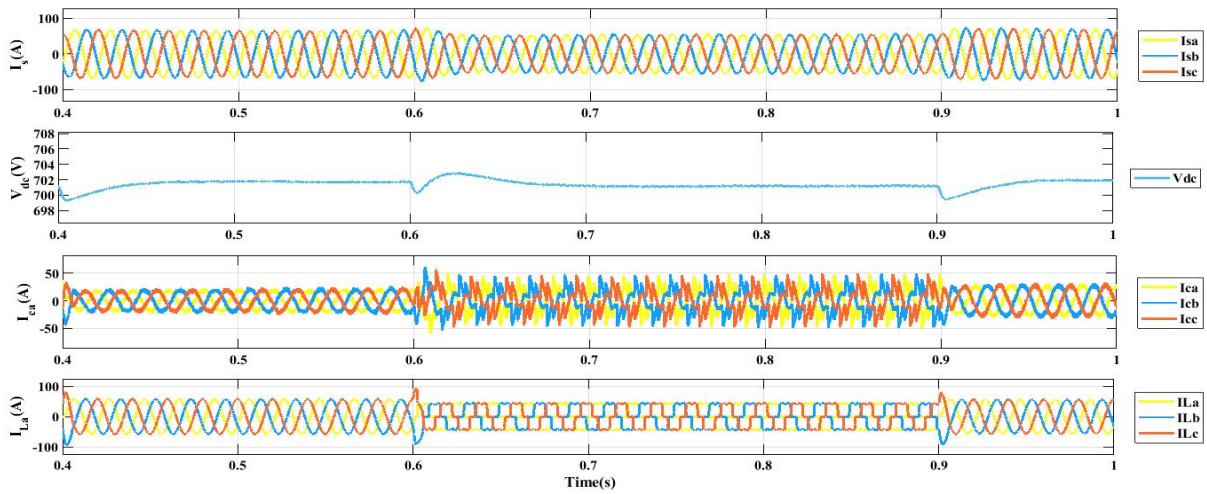

Figure 19. Performance of DSTATCOM under SRF controller.

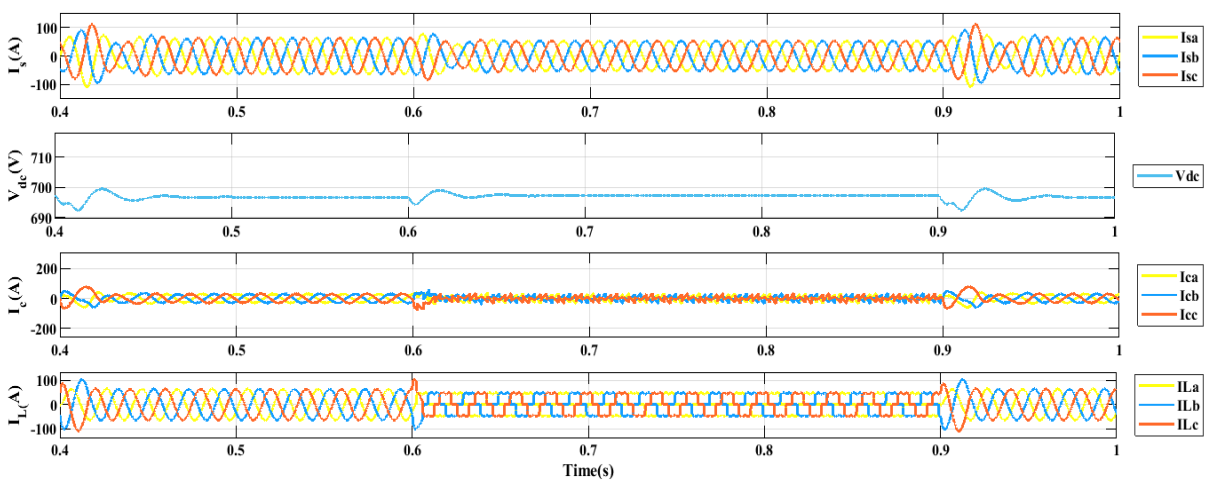

Figure 20. Performance of DSTATCOM under sliding mode controller.

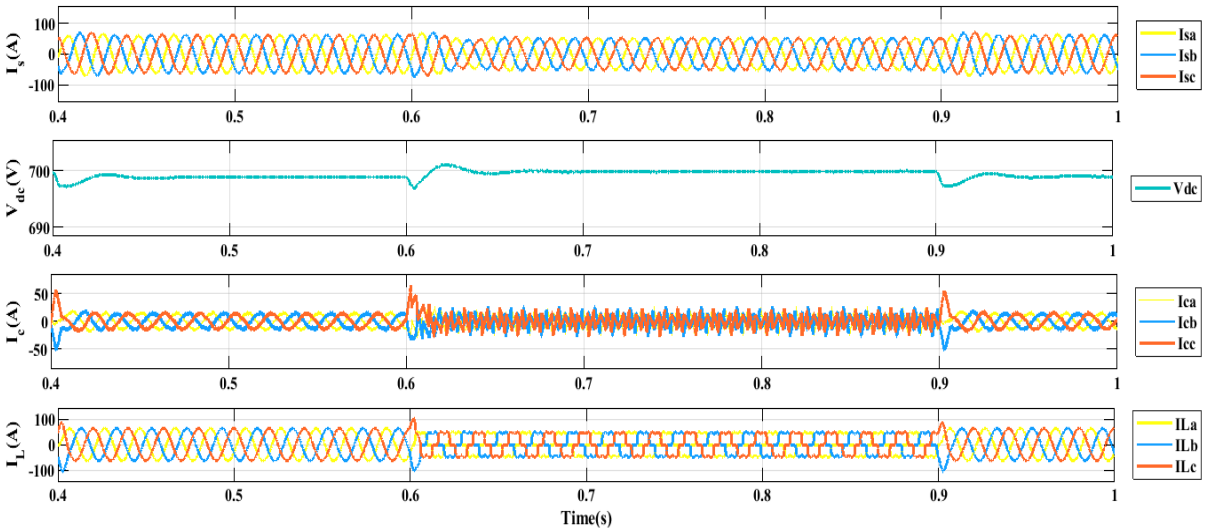

Figure 21. Performance of DSTATCOM under ADALINE LMS controller.

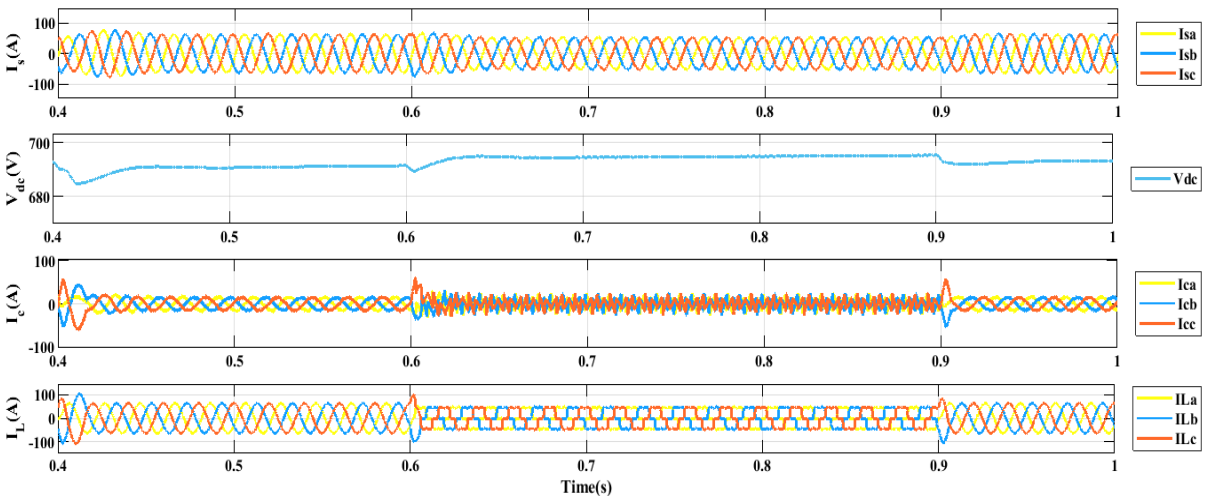

Figure 22. Performance of DSTATCOM under proposed enhanced SRF SOGI-FLL.

This increase in DC capacitor voltage will suddenly increase the reactive power demand and creates burden in the source side. It has been also observed that DSTATCOM current is sinusoidal for linear load, while DSTATCOM current is nonsinusoidal for nonlinear load.

Compensation Behavior of DSTATCOM Under Dynamic Load Condition from [1s-1.6s]

In this section, dynamic behaviors of DSTATCOM have been studied during t = [1s-1.6s]. Figs 23-26 represent the performance of DSTATCOM by SRF, SMC, ADALINE LMS, and proposed enhanced SRF SOGI-FLL controller, respectively. During t = [1s-1.2s], linear load has been employed. Hence, the wave form of source

current, DSTATCOM current, and load current are sinusoidal. In the interval t = [1.2s-1.4s], nonsinusoidal waveform occurs in load current and DSTATCOM current, while sinusoidal waveform of source current has been achieved due to DSTATCOM compensation.

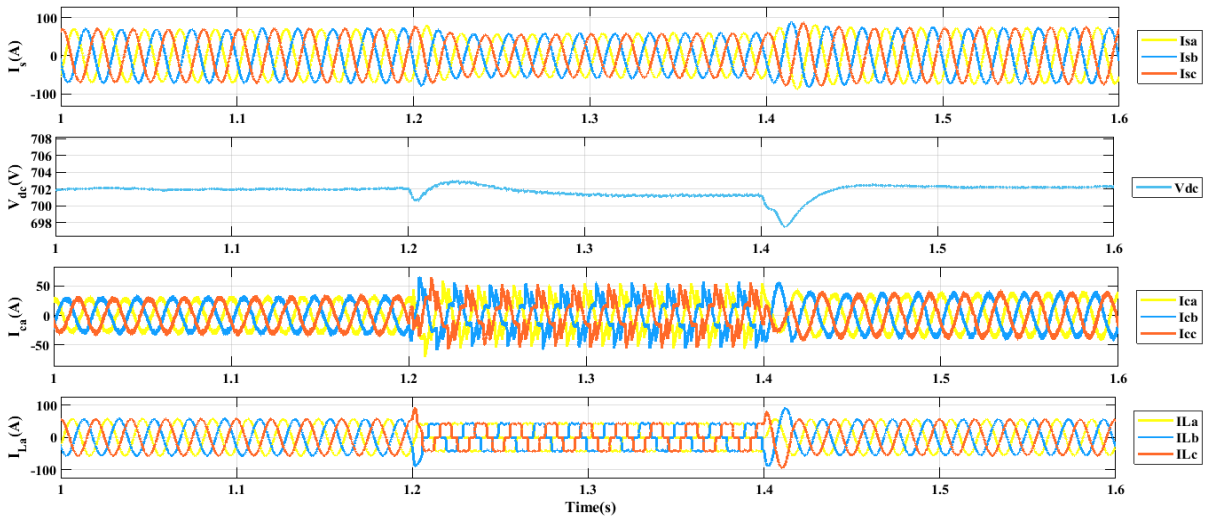

Figure 23. Performance of DSTATCOM under SRF controller.

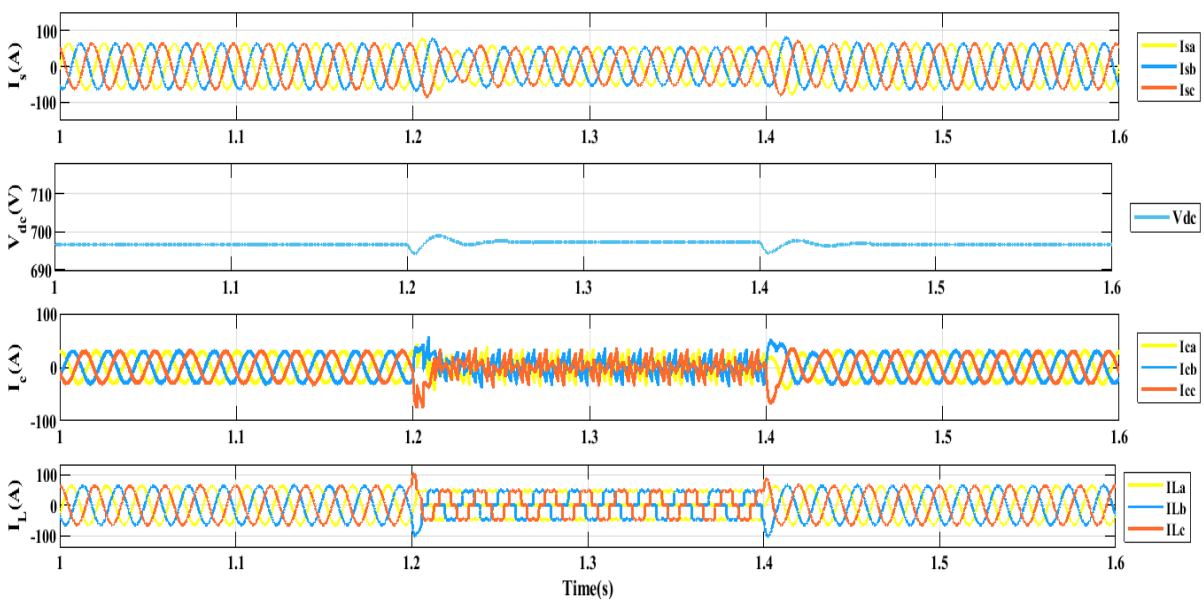

Figure 24. Performance of DSTATCOM under sliding mode controller.

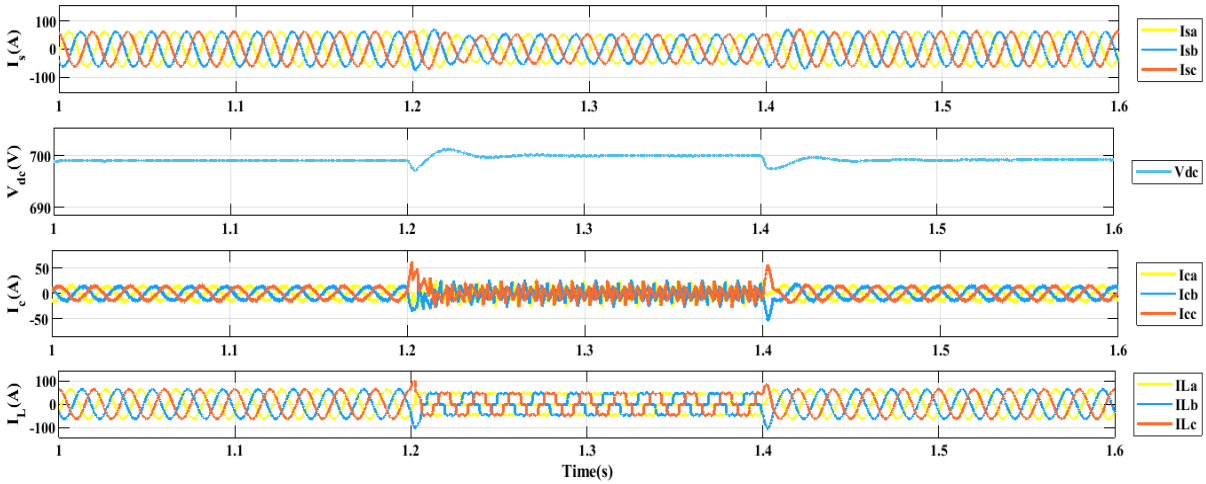

Figure 25. Performance of DSTATCOM under ADALINELMS controller.

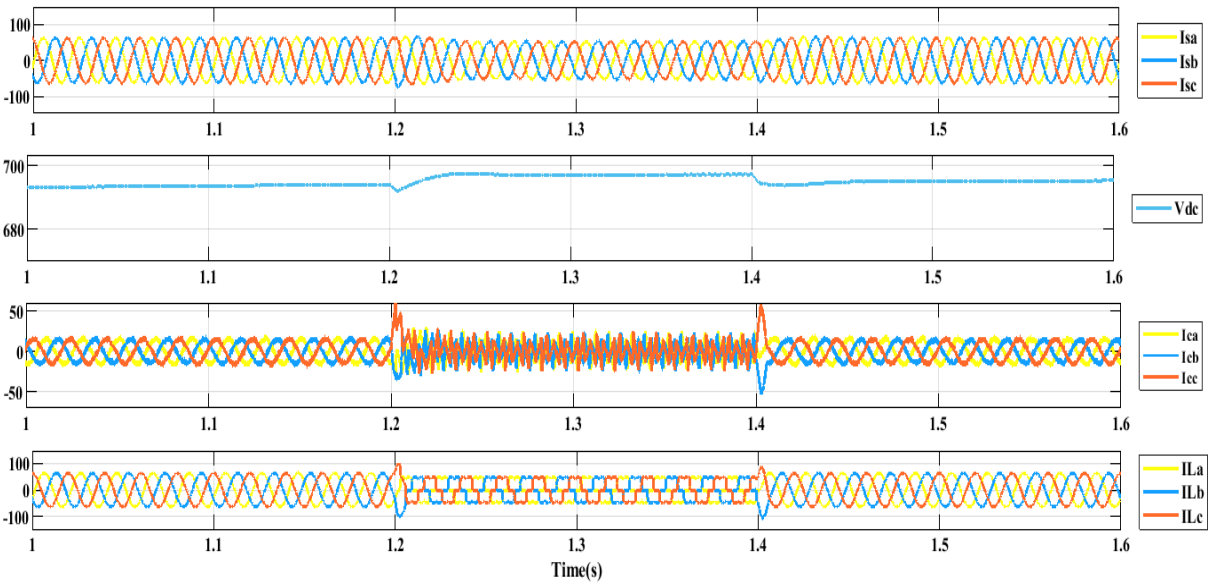

Figure 26. Performance of DSTATCOM under proposed enhanced SRF SOGI-FLL controller.

DC voltage regulation under proposed enhance SRF SOGI-FLL controller is 700V, but, in case of SRF, SMC, and ADALINE LMS, DC voltage regulation has been accomplished at 702V, 698V, and 697V, respectively.

Reactive Power Analysis of DSTATCOM Under Various Control Algorithms

Figs. 27 to 30 represent the performance evaluation by SRF, SMC, ADALINE LMS, and enhanced SRF SOGI-FLL controller, respectively, in terms of real and reactive power analysis. During interval t= [0s -0.2s], reactive power demand from load is increasing, and, after 0.2s, it comes to nearly "0" due to compensation effect of

DSTATCOM. When nonlinear load has been introduced and DSTATCOM is in "on" condition, then the reactive power demand by the load is full filled by the DSTATCOM. Hence, there is no impact on the source side, and it gives the null reactive power at that time. In the proposed controller, the reactive power is exactly at "0", but, in conventional controllers, reactive power is somewhat not zero but tends to reach zero. Figure 31 shows the grid voltage and current waveform. At t = 0s to 0.2s, when DSTATCOM is not in operation, source current is nonsinusoidal and out of phase with voltage. After t = 0.25s, when DSTATCOM starts compensation, source current is sinusoidal and in-phase with the source voltage, which shows power factor improvement on supply side.

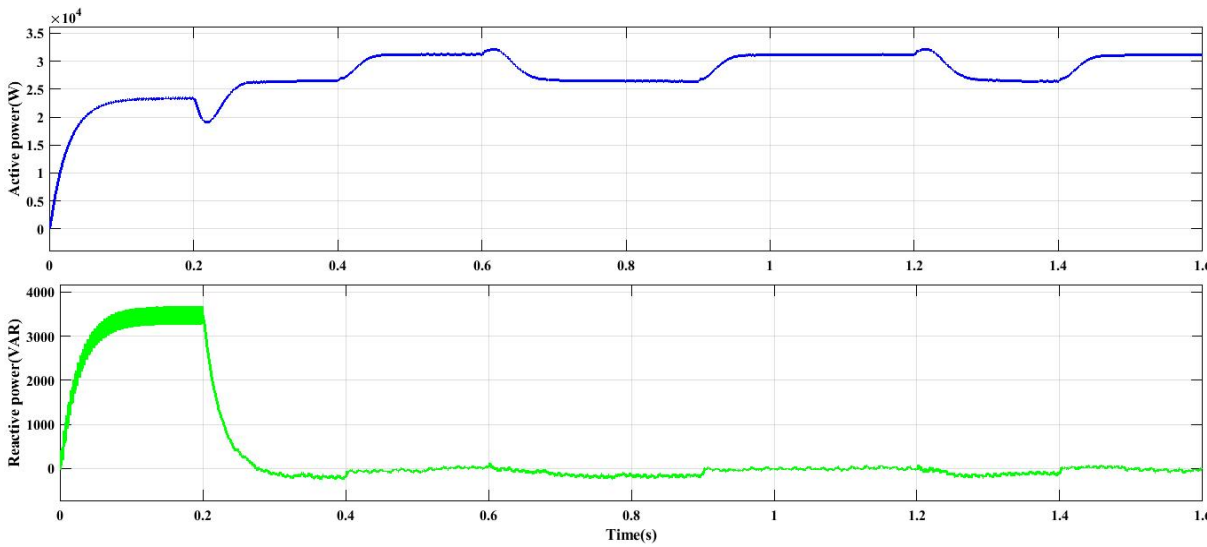

Figure 27. Reactive power analysis of DSTATCOM under SRF.

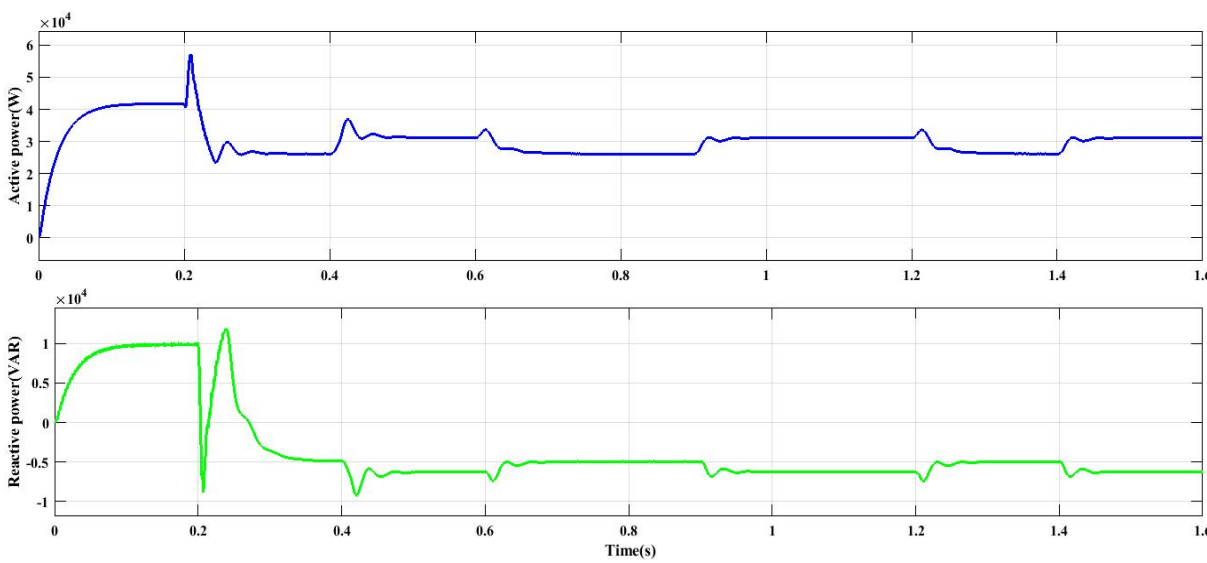

Figure 28. Reactive power analysis of DSTATCOM under SMC.

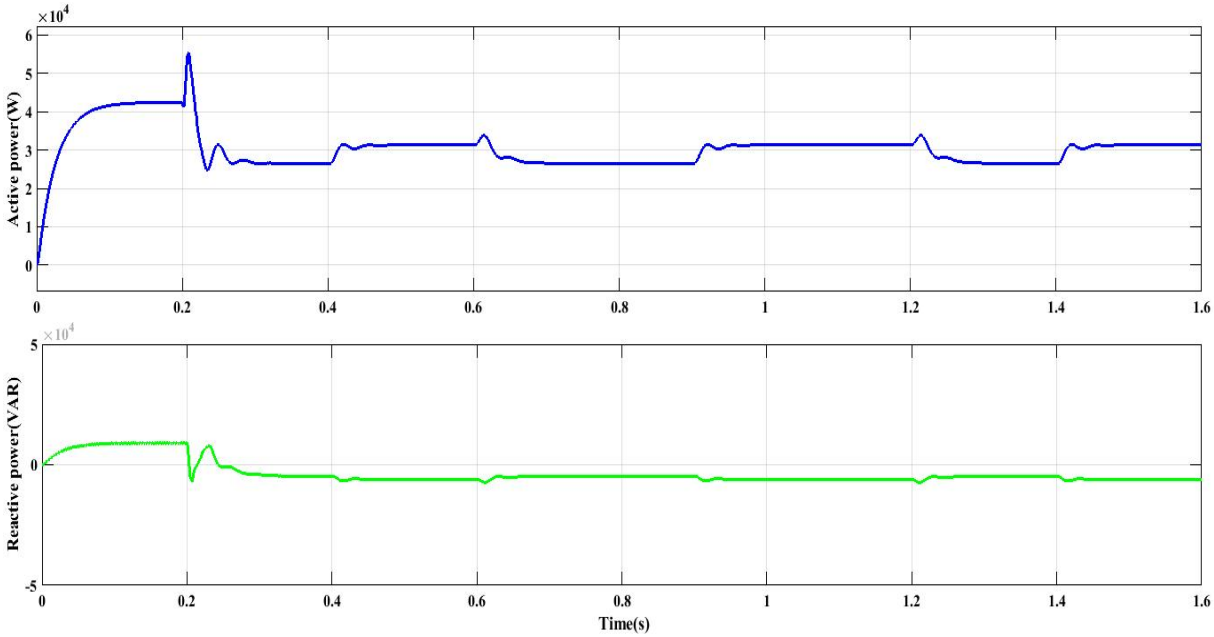

Figure 29. Reactive power analysis of DSTATCOM under ADALINE LMS.

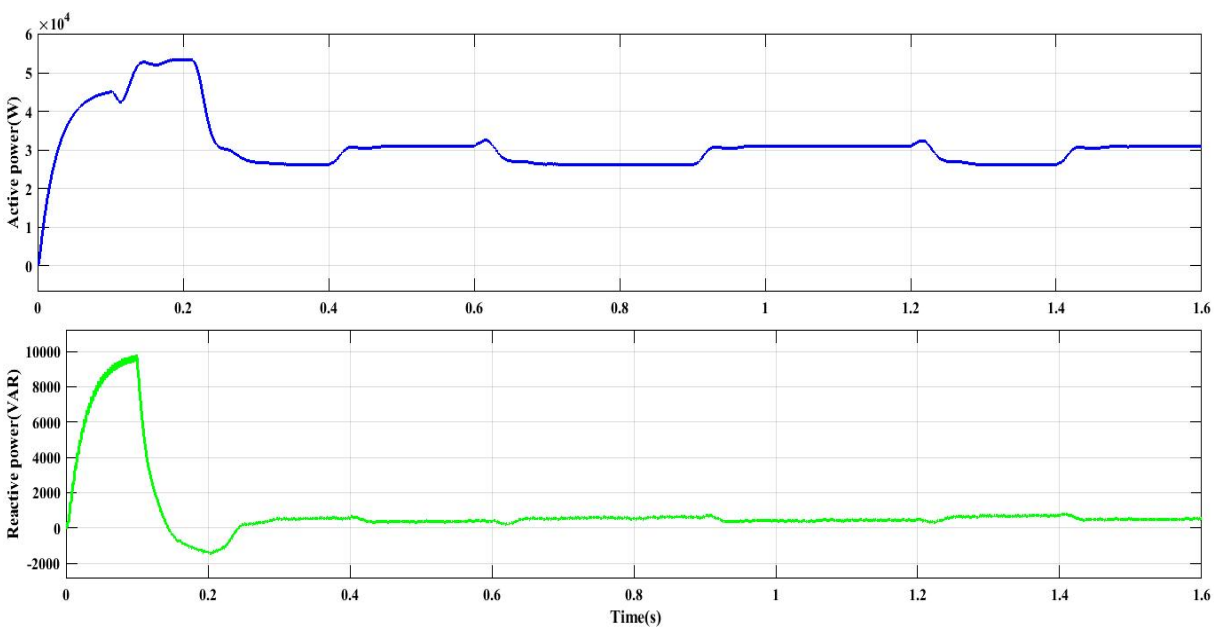

Figure 30. Reactive power analysis of DSTATCOM under proposed enhanced SRF SOGI FLL.

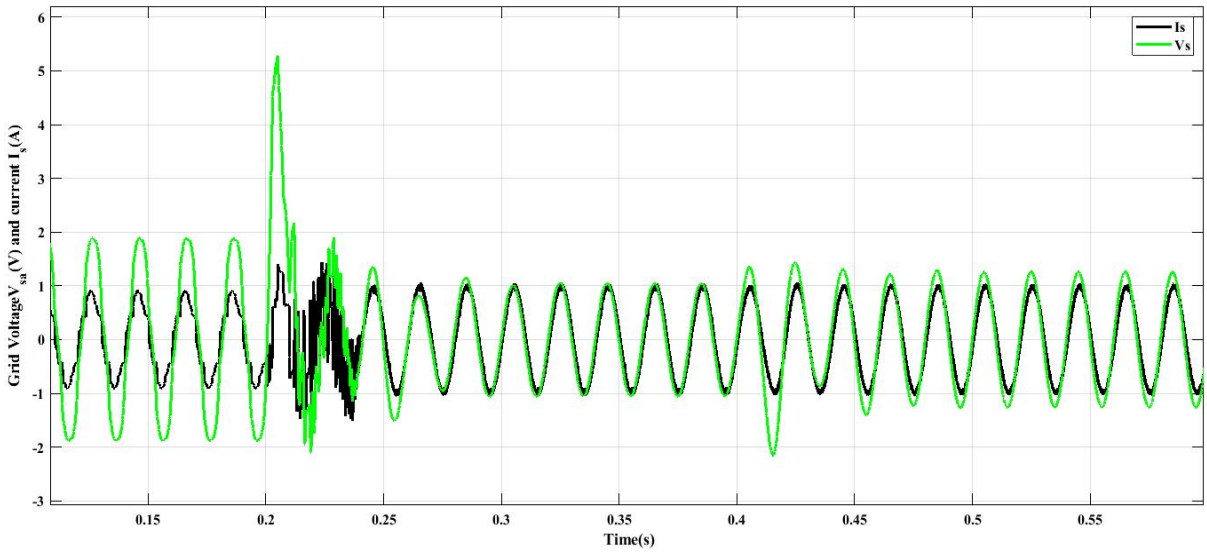

Figure 31. Grid voltage and current analysis under proposed enhanced SRF SOGI FLL.

Table 2. Obtained THD and Power factor data.

Control philosophies	Source current			Power factor
	I_{sa} THD (%)	I_{sb} THD (%)	I_{sc} THD (%)	
SRF	3.44	3.56	3.28	0.92
SMC	3.03	3.34	3.53	0.95
ADALINE LMS	1.81	1.93	1.93	0.97
Enhanced SRF SOGI FLL	1.32	1.46	1.23	1

Table 2 depicts the comparative analysis of source current THD and power factor in view of conventional and proposed controllers. Based on Table 2, it has been found that less source current THD has been achieved in proposed enhanced SRF SOGI FLL. Moreover, unity power factor has been occurred in enhanced SRF SOGI FLL. Table 3 indicates the comparative features of different control schemes adopted in the DSTATCOM.

Figure 32 shows the comparative power quality features of different control algorithms in chartable forms. To visualize the performances of power factor and THD, maximum value of DC voltage regulation has been taken as 7 instead of 700V. In this figure, the proposed controller represents better power quality performances.

Table 3. Comparison between SRF, SMC, ADALINE LMS, and enhanced SRF SOGI FLL.

Various parameter	SRF	SMC	ADALINE LMS	Enhanced SRF SOGI FLL
Computational burden	Complex calculation	Complex calculation	Complex calculation	Simple calculation
Efficiency	Good	Good	Good	Excellent
Complexity	More	Less	Less	Very less
Operational time	More	More	Less	Very less
Synchronization with grid capability	Present but conventional PLL have some disadvantages	Absent	Absent	Present with excellent characteristics
Harmonic compensation	Good (well within the IEEE-519)	Good (well within the IEEE-519)	Very good (Well within the IEEE-519	Excellent (well within the IEEE-519)
Dynamic behavior	It takes more time to be stable	It takes less time to be stable	It takes less time to be stable	It takes negligible time to be stable and acts very fast in dynamic situation

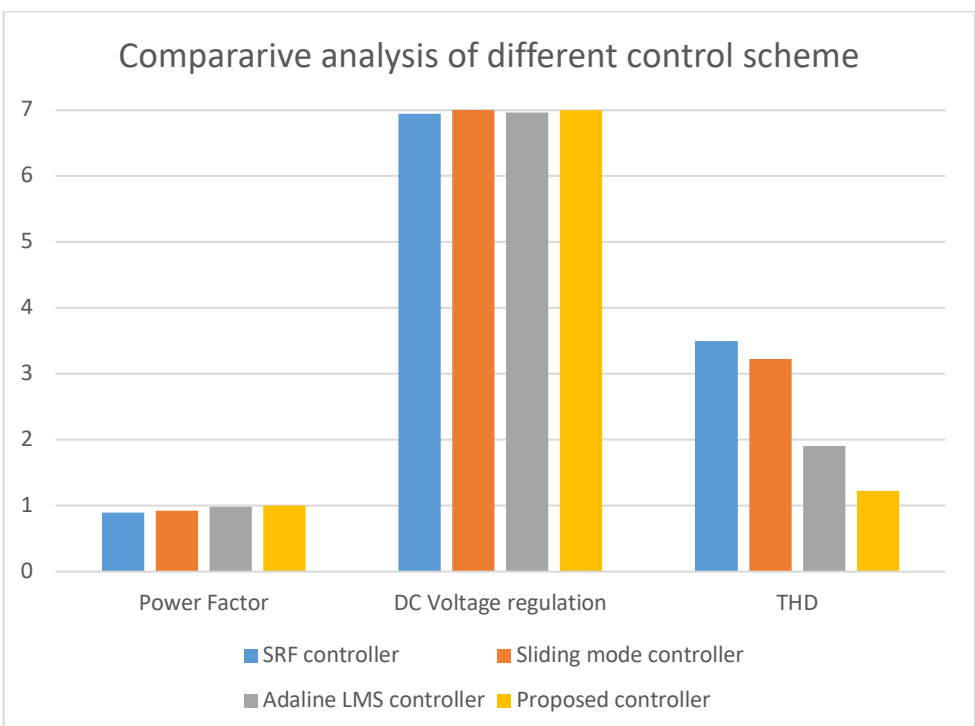

Figure 32. Chartable representations of comparative features.

CONCLUSION

The comparative studies of conventional, that is, SRF, SMC, ADALINE LMS, and proposed enhanced SRF SOGI FLL control based H-bridge DSTATCOM in three-phase four-wire distribution system have been elaborated in terms of power quality improvement. The performances of DSTATCOM have been tested under various dynamic loading conditions. On the basis of extensive simulation studies, it has been found that the above controllers are capable to restrict THD of the source currents as per IEEE-519 standard. Moreover, these controllers are also compensating the reactive power, balancing the voltages and currents phases, and improving the power factor on the supply side. In respect to comparison among these controllers, it has been found that the proposed enhanced SRF SOGI FLL performs the best power quality improvement features.

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