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Design of Area Efficient, Low-Power and Reliable Transmission Gate-based 10T SRAM Cell for Biomedical Application

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ABSTRACT

There is an immense necessity of several kilo bytes(kb) of embedded memory for Biomedical systems which typically operate in the sub-threshold domain with perfect efficiency. SRAM (Static Random Access Memory) dominates the total power consumption and the overall silicon area, as 70% of the die has been occupied by them. This paper proposes the design of a transmission gate-based SRAM cell for biomedical application eliminating the use of peripheral circuitry during the read operation. It commences the read operation directly with the help of transmission gates with which the data stored in the storage nodes can be read, instead of using the precharge and sense amplifier circuits which suits better for the implantable devices. This topology offers smaller area, reduced delay, low power consumption, and improved data stabilization in the read operation. The cell is implemented in 45nm CMOS technology operated at 0.45v.

Keywords: SRAM; Biomedical systems; Sub-threshold; Transmission Gate; Stability; 45-nm technology.

INTRODUCTION

SRAM with low power is a main concern of implantable devices like pacemakers, hearing aids, and wireless applications as shown in Fig.1. Pacemaker is a small device which is placed inside the human body in the chest region for controlling the patient's abnormal heart rhythms. These are particularly used to treat arrhythmias which is related to rhythm or rate of heart. In such devices, the input power or battery life is of a key concern (Chandrakasan et al., 2008; Chen et al., 2010), whose operational frequency ranges between some hundreds of kilohertz and a tens of megahertz (Liang et al., 2016). This is because of the major contribution of the SRAMs on the System on Chips (SoC) as they occupy about 70% of the die area, which could be further increased in the future (Maroof et al., 2017). The proliferation of the transistors count in SRAMs and the corresponding leaking current of these transistors in the downscaling technologies has prone these devices more to be power hungry.

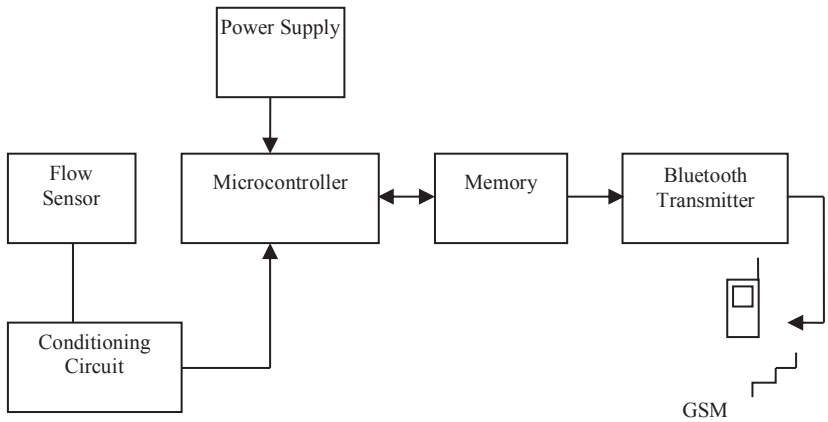

Figure 1. Medical control unit

Static Random Access Memories mostly contribute to the performance, area, and power dissipation of the digital integrated systems. The mentioned implantable and wireless applications require low power circuits operating for a long time, occupying less area without degrading the performance, as it provides inconvenience and may even be risky specially while considering the implantable devices. One of the most straight forward and worthwhile methods of achieving power efficiency is minimizing the voltage supplied, since the active power and the leakage power have an exponential and quadratic relation, respectively, with the supplied voltage (Kulkarni et al., 2012). However, lowering the supplied voltage would diminish the robustness of the circuit and can also cause the system to perform malfunction. Reducing the supply voltage while at the same time maintaining the robustness of the circuit is the most important thing for the power constrained systems, as data stability is one of the foremost concerns of the SRAM cells.

At the near and subthreshold region, the Conventional 6T design declines to function properly because of the deterioration of write ability and the read stability (Yamaoka et al., 2005). To have a triumphant write operation, it is desirable to use a wide access transistor which in turn could affect the read stability. This represents a tradeoff issue for the data stability during the write and read operations. Researchers proposed several cells basing on removal of the tradeoff between the read and write stability issues. In these proposals (such as Kim et al., 2009; Verma et al., 2008; Sinangil et al., 2009; Wu et al., 2011; Kulkarni et al., 2011; Tu et al., 2010; Liu et al., 2008; Calhoun et al., 2006; Rohit Lorenzo et al., 2020; Kim et al., 2008; Chang et al., 2009; and Soumitra et al., 2020), cells rely on decoupling the read & write ports by separating the read as well as write paths allowing each of the operations to be enhanced independently. However, they are either prone to leakage current, occupy more area, or utilize a single-ended read scheme that degrades the read sensitivity (Saeidi et al., 2014). To conquer the complication of single ended read scheme, various techniques were implemented enhancing differential read port by including extra transistors but with a penalty of extra area (Kulkarni et al., 2012). One more technique designed was using the transmission gates to improve the stability (Soumitra et al., 2019).

This paper proposes a new transmission gate-based 10T SRAM cell specifically designed for Read operation which efficiently improves the Read Noise Margin with reduced power and reduced delay. It particularly minimizes the area by using less number of transistors by eliminating the peripheral circuitry that is required to carry out the read process. The residual part of this paper provides the basic architecture of SRAM, projects the operation of the Conventional 6T, 8T, and other existing 10TSRAM designs, presents the proposed 10T SRAM design's performance with detailed explanation, gives the comparative results of the proposed design with the existing ones, and winds up with a conclusion.

SRAM ARCHITECTURE

Figure 2 displays the block diagram of a typical architecture of SRAM (Bellaouar et al., 1995). The SRAM chip chiefly consists of memory array, row decoder, column decoder, precharge circuit, and sense amplifier

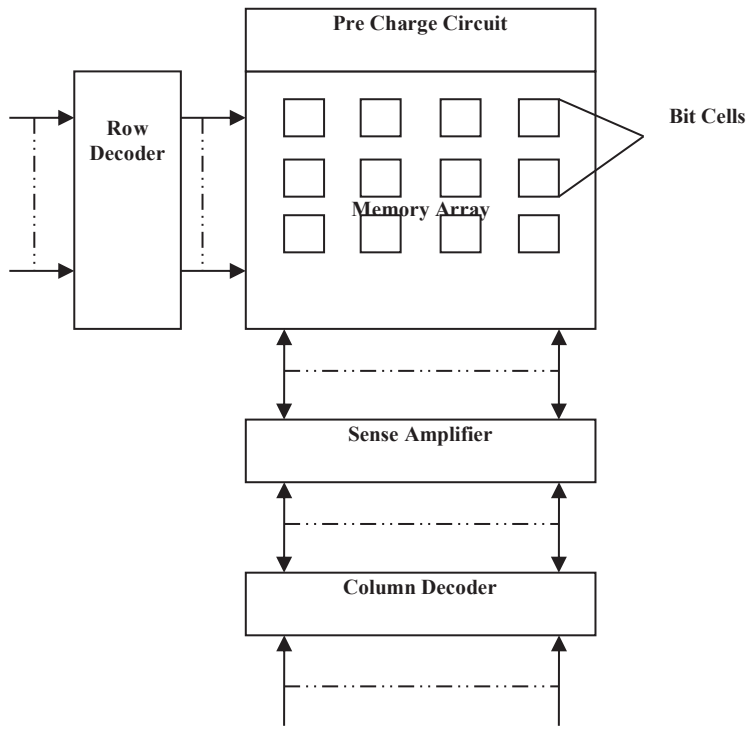

Figure 2. SRAM Architecture

The memory array consists of number of cells in which the data is to be stored or read. Each of the cells is capable of holding one bit of information. A row decoder and a column decoder select a particular cell from the array. The precharge circuit activates the precharging of Bit Lines. A sense amplifier particularly performs the read functionality. It detects the content of a cell in the form of a small voltage variation obtained between the cells' Bit Lines & produces the corresponding information that is accumulated in that particular cell.

EXISTING DESIGNS

In SRAMs, memory cell is a basic element as it occupies significant portion of the area. Implementation of Conventional 6T design is very simple as depicted in Fig.3. The cell is well structured with two pass transistors and two cross connected inverters. The two cross connected inverters form a simple latch capable of accumulating one bit of the data. The two passage transistors are connected with the two complementary type of Bit Lines (BL & BL Bar) and a Word Line (WL), providing connection between the cell and the outside world. SRAMs usually operate in three states, namely Read, Write, and Hold (Abhishek et al., 2014).

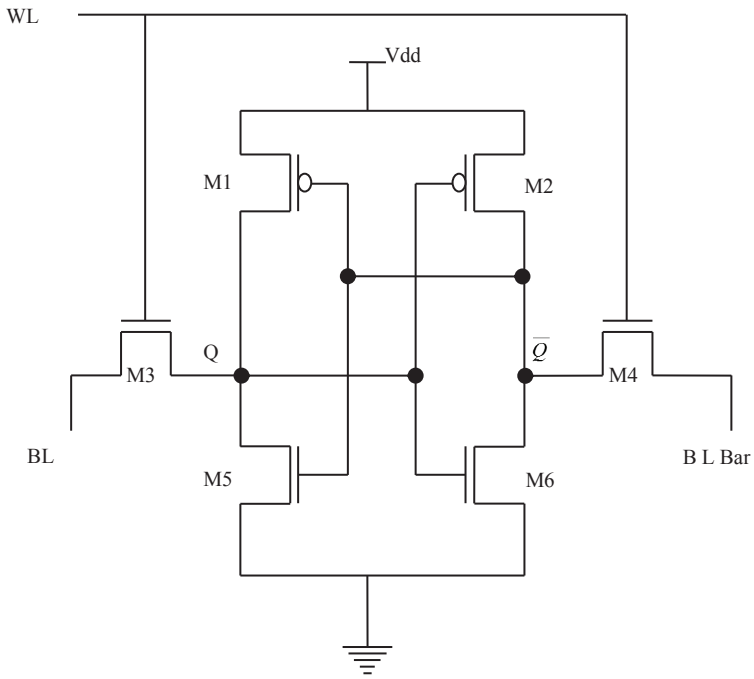

Figure 3. Conventional SRAM

For a Write function, the information to be entered is inclined to the two complementary Bit Lines. For instance, if we wish to write '1', then BL should be raised to '1' andBL Bar should be raised to '0'. The WL signal is then activated, and thus the data given to the Bit Lines is entered into the cell with the help of access transistors M3 and M4 and is accumulated in the two corresponding storage nodes Q and $\overline{Q}$.

For a Hold operation, WL is deactivated by breaking the connection between the cell and the two BLs. Thus, the two cross connected inverters will proceed to reinforce the information as long as they are given with the supply.

For a Read operation, the voltages at the two BLs are precharged initially to an equalized potential and then the WL is activated. Now relying on the info existing on two storage nodes, one Bit Line will be discharged to ground and the other Bit Line will be remained at Vdd. For Instance, if a value '1' is present on the storage node Q and a value '0' is present on the storage node $\overline{Q}$., then, BL Bar will be discharged to ground through M6 and M4, and simultaneously the current passes from Vdd to BL through M1 and M5. Thus, a small voltage variation emerges at the two Bit Lines where the voltage level will be higher at BL than BL Bar. This small voltage difference is then fed to the sense amplifier that detects and magnifies the signal and produces appropriate value present on the storage node Q.

The Conventional 6T SRAM cell declines in various conditions such as read stability due to the conflict between pull up or pull down and the access transistors and variability, that is, less reliable in submicron technology as a consequence of process parameters variations. Due to these overwhelming issues, various cells have been designed, which started with an 8T SRAM cell design (Chand et al., 2008) as given in Fig.4. The cell comprises of a decoupled read path with two extra NMOS transistors to eradicate the read disturb issue. But, it suffers from the leakage problem due to the added transistors relying on the information stored in the cell.

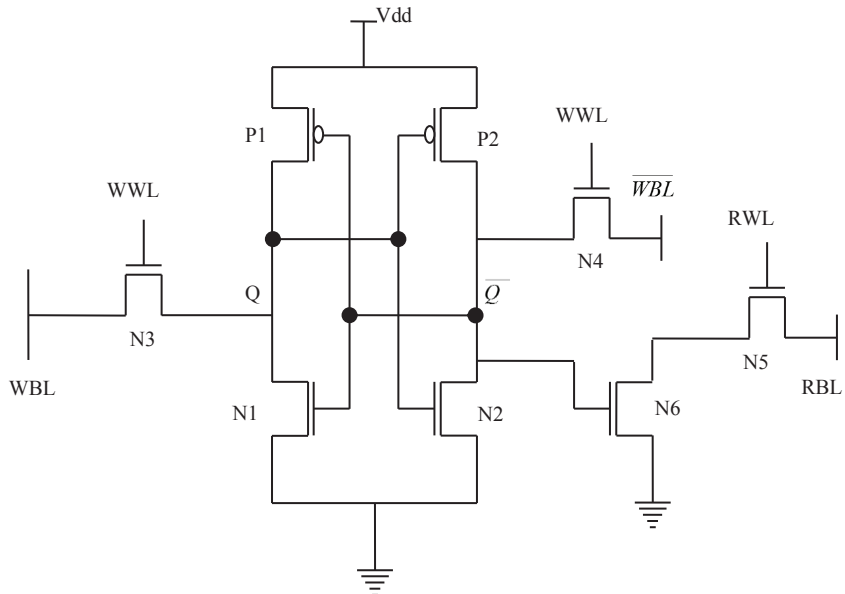

Figure 4. 8T SRAM Cell

To solve the leakage issue, many other cells have been designed. A recent work was presented in Ghasem et al., 2015, as shown in Fig.5 (referred to as 10T-E1) which includes a PMOS transistor at the read path, reducing the leaking current passing through M6 transistor. But the design at the same time also causes the passage of leaking current from the node into RBL which thereby leads to the reduction of sensing margin and is also data dependent.

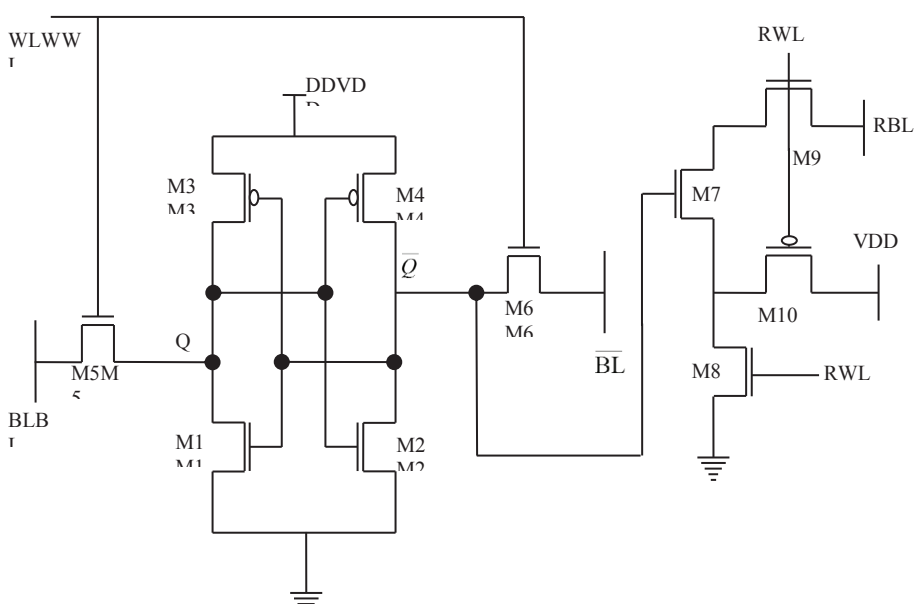

Figure 5. 10T-E1 SRAM Cell

10T-E1 is modified in Shourya et al.,2018, by designing the SRAM cells with NMOS-only based read ports as depicted in Figures6 and 7(referred to as 10T-E2 and 10T-E3). These designs use a separate read portion consisting of four NMOS transistors (M7, M8, M9, and M10) to perform the read functionality. The isolated read ports in both designs cause a destruction to free read operation with better read stability. Bit Line Leakage is also improved in such cases as the separated read port uses a stack of transistors (Chen et al., 1998). But Figure 6 is still data dependent, whereas Figure 7 maintains a complete data-independent leakage path.

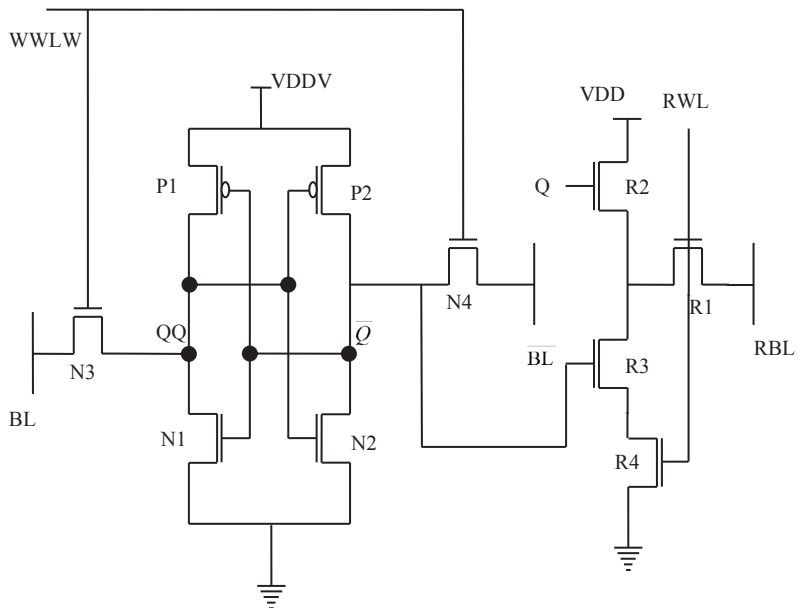

Figure 6. 10T-E2 SRAM Cell

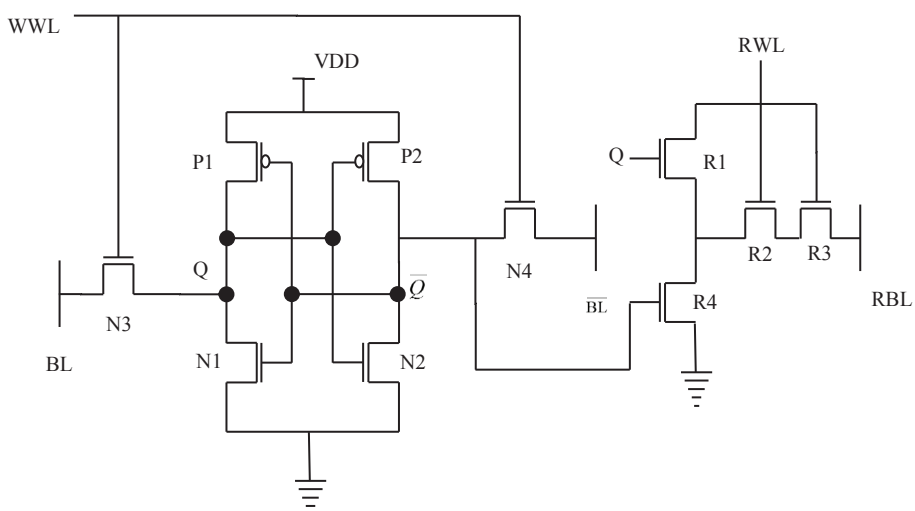

Figure 7. 10T-E3 SRAM Cell

The Conventional 6T and other advanced designs mentioned in this section also need complex peripheral circuitry such as precharge circuit, write drivers, and sense amplifier. The area occupied by those peripheral circuits encircling the cell area adds an enormous portion of the overall macro cell. A recent proclamation (Guo et al., 2018) insists that about 25% of the macro area is assigned to the peripheral circuitry.

PROPOSED SRAM CELL

The existing 10T cell and many other related cells succeed in improving the read stability but at a penalty of increase in area as they require more number of transistors to do so. However, for many applications, such as biomedical and wireless applications, area occupancy also plays a vital role. If considered in biomedical implants, less area occupancy of the device inside the body is considered less invasive to the human body. In view of such an issue related to the SRAM design, this brief presents a transmission gate-based 10T SRAM structure as shown in Figure 8. This design reduces the area occupancy by eliminating the peripheral circuitry.

The proposed design chiefly concentrates on the read operation, which in the existing designs exclusively instills on the peripheral circuits. The Write operation is homogeneous to the Conventional & the other SRAM designs. The Write functionality is managed by the Word Line (WL). The content which we incline to write is given to BL and $\overline{BL}$. Now, the enabled WL, making the access transistors active, allows the data of the BLs to intrude into the memory cell. The intruded data will thus be cached into the two storage nodes WQ and $\overline{WQ}$.

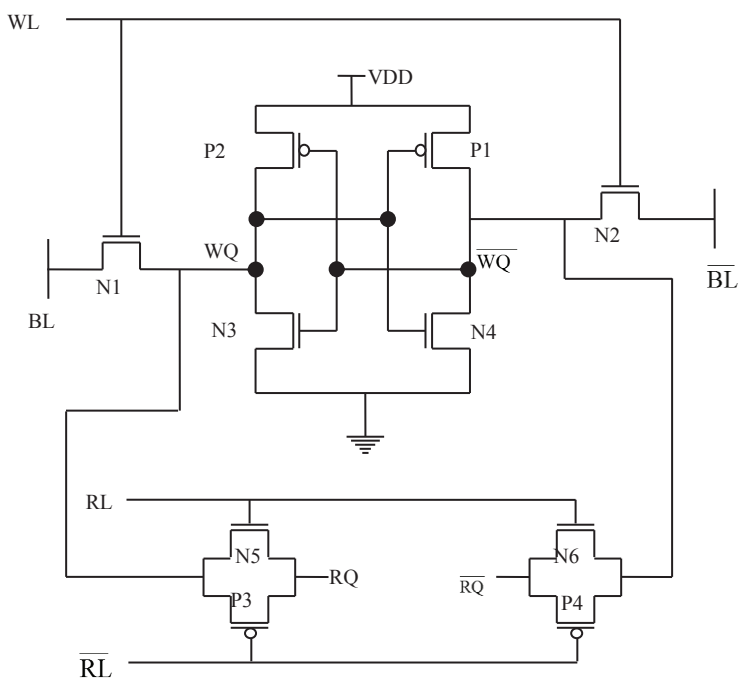

Figure 8. Proposed SRAM

The read operation is controlled by the two complementary Read Lines RL and $\overline{RL}$ and must be enabled before starting the read process. The read port is separately designed by employing two transmission gates. Here, the main intention is to get the information that is accumulated in the storage nodes WQ and $\overline{WQ}$. Therefore, the information that is cached in the storage nodes is conferred to the two transmission gates N5, N6, P3, and P4 which are in ON state as the Read Lines are enabled previously. Now, these transmission gates pass the data and confer it to the Read

nodes RQ and $\overline{RQ}$. The data stored in the node WQ will appear in the node RQ through N5 and P3 transistors and the data stored in the node $\overline{WQ}$ will appear in the node $\overline{RQ}$ through N6 and P4 transistors. Thus, the content of the cell can be directly read with the help of the transmission gates instead of using complex peripheral circuits.

This design reduces the chip area of about 15% as the number of transistors is reduced, for designing the peripheral circuits. The reduction in the count of transistors used, in turn, reduces the total power consumption. This is because the leakage power relays on the number of transistors used in a design as explained below.

$$P_{total} = P_{dyn} + P_{Leak} \tag{1}$$

$$P_{dyn} = CeV_{dd}^2 f \tag{2}$$

$$P_{Leak} = V_{dd}\ N_{tr}\ K_d\ I_s \tag{3}$$

N_{tr} represents the number of transistors, K_d is a device specific constant, and I_s is the normalized static current for each transistor.

The decrement in the transistor count yields to the lowering of leakage power of those transistors, thereby reducing the overall power dissipated in the circuit.

Since the sense amplifier and the precharge circuits used for the read functionality in the existing designs are eliminated in the proposed design, the delay of generating the output, that is, reading the data present in the storage nodes can also be reduced. This is because of undergoing the read operation directly with the help of transmission gates.

This approach also maintains the stability, since the read and write ports are separated. The averaging consequence of two parallelly placed transistors of a transmission gate helps in nullifying the read current producing better stability than that of using a single NMOS for the read current to pass by. The cell failure probability can be predicted by considering the Gaussian distribution for the threshold voltage of a transistor (Chang et al., 2012). It is calculated as follows:

$$P_{fail} = Prob\,[SNM < V_{th}] \tag{4}$$

where $V_{th} = kT/q$ (5)

kT = 26 mV at 300K

SIMULATION RESULTS AND PERFORMANCE EVALUATION

The Timing diagram of the work projected in the brief is represented in Figure9 which depicts the Write and Read functionality of the cell.

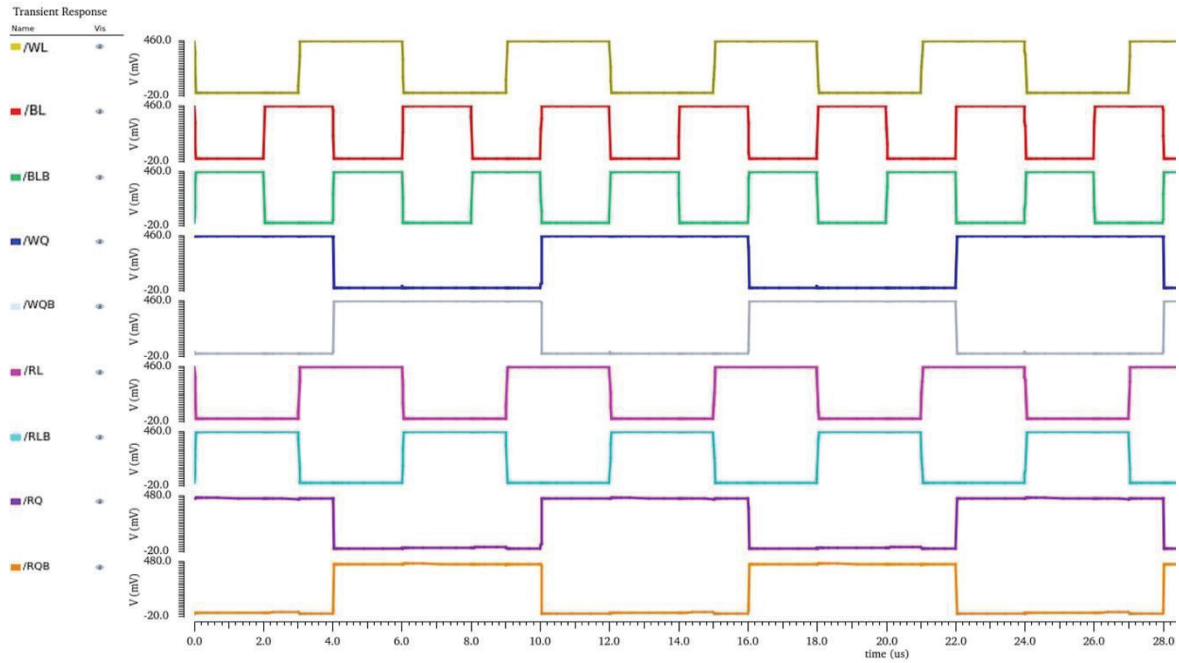

Figure 9. Timing diagram for subsequent read-write function of the proposed cell.

A comparison of the proposed work is done for the read functionality itself, since the design is intended to perform the read process only. The entire work carried out in this paper is done for a single bit only. Since the write and hold operations are similar to the existing designs, the performance results are also homogeneous. Therefore, the results discussed here consider the read state. Generally, the performance analysis of SRAMs is based on certain parameters such as Delay, Power Consumption, Stability, and Area occupancy of the cell. The performance comparison of the Conventional 6T (C6T), other existing techniques (8T,10T-E1,10T-E2, and 10T-E3) ,and the Proposed technique (P10T) is done in CMOS 45-nm Technology at 0.45v at room temperature as shown in Table.1.

Table 1. Parameters comparison.

Parameters	**C6T**	**8T**	**10T-E1**	**10T-E2**	**10T-E3**	**10T-P**
Technology (nm)	45	45	45	45	45	45
Supply Voltage(mV)	450	450	450	450	450	450
Read power(nW)	112.2	19.84	12.74	12.73	12.74	0.052
Read delay(us)	0.310	0.077	0.075	0.062	0.077	0.0055
Read SNM(mV)	86	180	175	180	170	180
Leakage power (pW) 0	3.196	8.752	10.76	17.9	8.53	1.827
Leakage power (pW) 1	3.29	13.27	491.4	13.35	8.583	1.88

POWER ANALYSIS

At a given voltage, the consummate power of the SRAM cell should be less enough as possible. It is examined from Table 1 that read power of the proposed design (P10T) drains the minimal power when compared to the other five designs. This is because since the peripheral circuits that are generally used by the remaining cells are excluded in this proposed work. Therefore, the power consumed by those circuits can be eliminated, thereby providing less power consumption for the proposed work.

ACCESS TIME ANALYSIS

Access time of the cell should also be given priority as it represents the time taken by the cell to perform a particular action. Table 1 provides the comparison of access time of the six cells, which generally represents the delay generated between the input and the output obtained. It can be explored that, the delay generated by this proposed cell (P10T) is less than the other five designs. This is for the reason that instead of precharging the two Bit Lines and then feeding them to the sense amplifier and finally the sense amplifier producing the stored data of the cell as done in the existing techniques, the proposed design directly produces the stored data which subsequently reduces the access time.

STABILITY ANALYSIS

In SRAMs, Stability of the cell is very much decisive since it personifies the reliability of any design. Typically, the SRAM's stability is calculated by Signal Noise Margin (SNM). SNM is a minimal noise voltage (dc) which can alter the data of a cell causing a failure of the design. The SNM should be high enough to maintain the reliability of the design.

Table 1 shows the comparison results of the read signal noise margin, RSNM, of the six SRAM cells. It explores that the RSNM of the proposed design is satisfactory when correlated to 8T,10T-E1,10T-E2, and 10T-E3 cells, while it gives tremendous improvement than the Conventional 6T as the main failure of C6T itself is providing less stability. Such an improvement is possible because of the decoupled write and read ports and the averaging effect of the transmission gate (18).

AREA ANALYSIS

In addition to the power, delay, and stability, one more influential parameter is the area occupancy of the cell in the Soc chip. Since about 25% of the macro cell has been encircled by the peripheral circuits (sense amplifier, precharge circuit, and write drivers) of the SRAM chip, the proposed design by abolishing the need of sense amplifier and precharge circuit leads to the saving of about 15% (10% of a sense amplifier and 5% of the precharge circuit) of the chip area. This provides a virtuous advantage for the considered biomedical application in the medical implants.

LEAKAGE POWER

Leakage Power is another principal factor to be considered which comes into picture whenever the cell is in the Standby state. It gives the power drained by the cell whenever it is in an unused state. This is measured by considering two states, that is, when the cell stores 'zero' and when the cell stores 'one'. It could be noticed from Table 1 that this proposed cell consumes lowest Leakage Power when compared with the other five considered cells.

Figures10, 11, 12, 13, and 14 represent the read power, read delay, RSNM, and the leakage power measurements at varying supply voltages, respectively. It is clearly spotted that the read power, delay, and the leakage power of the proposed design provide good improvement when compared with the other five considered cells. It also maintains almost equal noise margin with 8T, 10T- E1, 10T- E2, and 10T- E3 cells and a huge improvement than the C6T cell at most voltages.

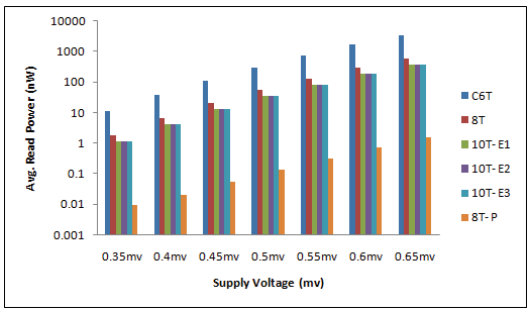

Figure 10. Read power comparison of considered cells with varying supply voltages.

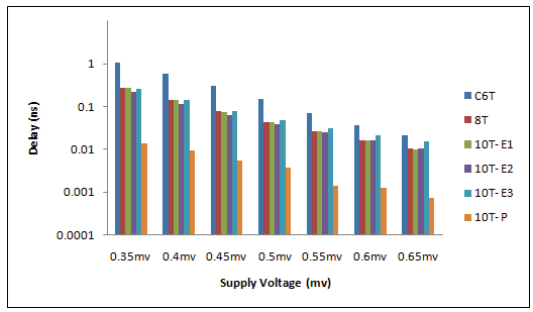

Figure 11. Delay comparison of considered cells with varying supply voltages.

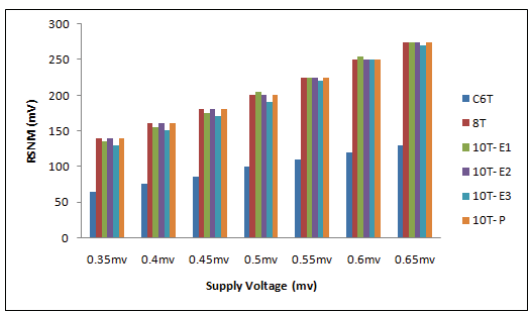

Figure 12. RSNM comparison of considered cells with varying supply voltages comparison of considered cells.

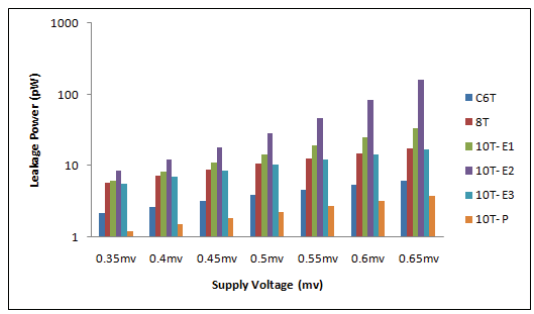

Figure 13. Leakage power when the cell stores 'zero' with varying supply voltage.

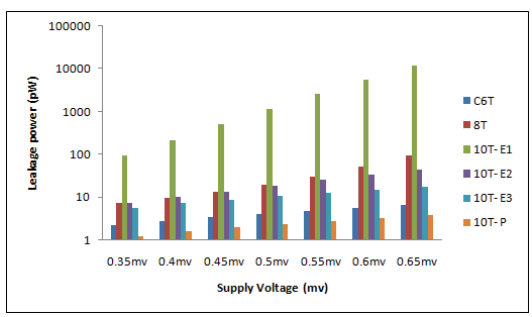

Figure 14. Leakage power when the cell stores 'one' comparison of considered cells with varying supply voltage.

Figures15, 16, 17, 18, and 19 represent the measured read power, read delay, read noise margin, and leakage power at different temperatures, respectively. It projects that the proposed cell has a comparable or better results in power and delay compared to the considered cells. It also exhibits a comparable or good RSNM when compared to the C6T and maintains similarity with the other five considered cells. From Fig.17, it is observed that the cell is more reliable at low temperatures than at the higher temperatures.

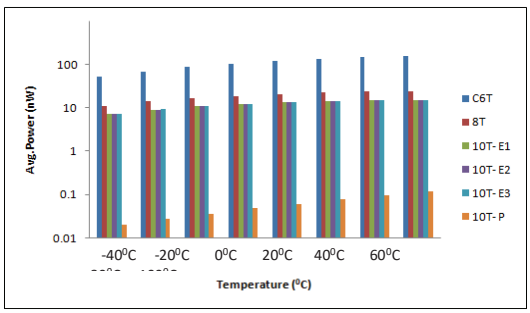

Figure 15. Read power comparison of considered cells under various temperatures.

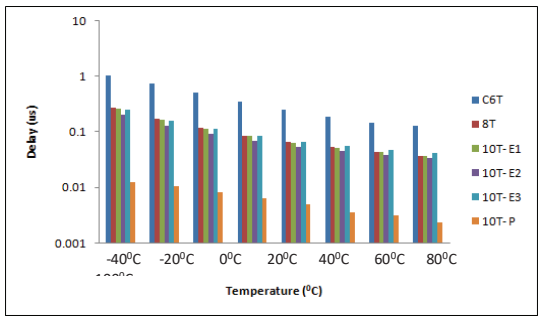

Figure 16. Delaycomparison of considered cells under various temperatures.

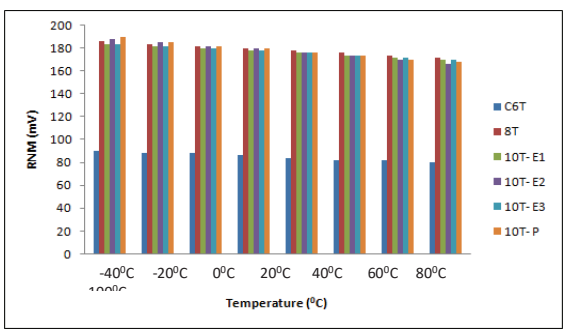

Figure 17. RSNM comparison of considered cells under various temperatures.

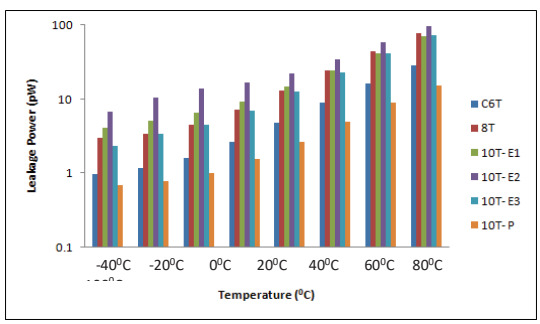

Figure 18. Leakage Power when the cell stores 'zero' comparison of considered cells under various temperatures.

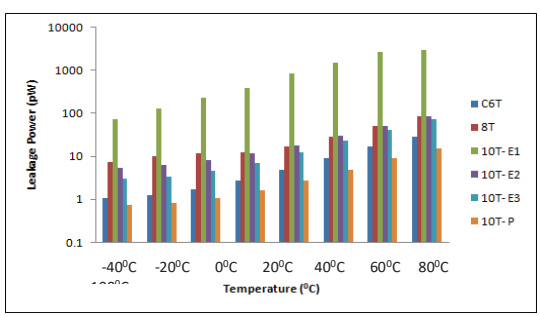

Figure 19. Leakage Power when the cell stores 'one' comparison of considered cells under various temperatures.

CONCLUSION

In this paper, a transmission gate-based 10T SRAM design is implemented for biomedical applications. This design with decouple read port eliminates the necessity of peripheral circuits to undergo the read operation. Such design provides virtuous improvement in power consumption, delay, stability, and area. This is feasible because of reducing the count of transistors used in the peripheral circuits of precharge and sense amplifier through which the area can be optimized. And also due to the reduction in transistors count, the power consumption can also be reduced up to 99% compared to the Conventional 6T and the other considered techniques. Eliminating the peripheral circuitry during the read operation and directly performing it with the help of transmission gates result in the optimization of delay of about 98% when compared to the Conventional 6T and 8T and about 92.7%, 91.2%, and 92.9% compared to 10T-E1, 10T-E2, and 10t-E3, respectively. The decoupled read port achieves 52.2% better read noise margin providing stability to the design when compared with the Conventional 6T and maintains almost the same noise margin with the other considered cells. The proposed cell consumes lowest leakage power of 42.8%, 79.1%, 83%, 89.7%, and 78.5% compared to Conventional 6T, 8T, 10T-E1, 10T-E2, and 10T-E3, respectively, when the cell stores 'zero', and about 42.8%, 85.8%, 99%, 85.9%, and 78% compared to Conventional 6t, 8T, 10T-E1, 10T-E2, and 10T-E3, respectively, when the cell stores 'one'. The proposed design also achieves better results in all the parameters of power, delay, read noise margin, and leakage power at different supply voltages and different temperatures than the existing designs. When compared to the considered cells, the proposed work enlarges the design for memory designers in Bio-Medical devices especially like pacemakers and hearing aids.

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