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A low power and high speed approximate adder for image processing applications

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ABSTRACT

Low power is an essential requirement for suitable multimedia devices, image compression techniques utilizing several signal processing architectures and algorithms. In numerous multimedia applications, human beings are able to congregate practical information from somewhat erroneous outputs. Therefore, exact outputs are not necessary to produce. In digital signal processing system, adders play a vital role as an arithmetic module in fixing the power and area utilization of the system. The trade-off parameters such as area, time and power utilization and also the fault tolerance environment of few applications have been employed as a base for the adverse development and use of approximate adders. In this paper, various types of existing adders and approximate adders are analyzed based on the area, delay and power consumption. Also, an approximate, high speed and power efficient adder is proposed, which yields better performance than that of the existing adders. It can be used in various image processing applications and data mining, where the accurate outputs are not needed. The existing and proposed approximate adders are simulated by using Xilinx ISE for time and area utilization. Power simulation has been done by using Microwind Software.

Keywords: Approximate adder; Area consumption; CMOS; High speed; Image processing; Power efficient.

INTRODUCTION

In inexact computing, approximate adders are the essential building block for the arithmetic circuits. Approximate adders have inaccurate outputs for carry and sum with some combinations of inputs, which have incorrect outputs for sum and carry. So, the hardware requirement of the system gets reduced for inexact computing. As a result, approximate computing yields high speed and low power consumption for the design. However, approximate computing is a suitable choice for DSP applications like video, image, and audio processing, where accurate results are not essential. Adders are implemented by using various digital CMOS technologies (Ashim et al., 2016; Chip-Hong et al., 2005) such as Transmission Gate Adder (TGA), Complementary Pass Transistor Logic (CPL), and (Uming et al., 1995) Double Pass Transistor Logic (DPL) in order to reduce the power consumption of the design. High Performance Error Tolerant Adders and Multiplexer based arithmetic full adders (MBAFA) are proposed (R. Jothin et al., 2018) to reduce the design parameters such as

area and power consumption and also to improve the accuracy. Various types of approximate adders are proposed (Fazel Sharifi et al., 2017; Jeevan Jot Singh et al., 2018; Zhixi Yang et al., 2013; Vaibhav Gupta et al., 2013), and their performance is analyzed based on the area, power, speed and accuracy of the results. In Honglan Jiang et al. (2015), various types of approximate adder techniques are analyzed. Error and circuit characteristics are compared. Equal segmentation Adder (ESA) is proposed, which results in better hardware efficiency, but with the lowest accuracy in terms of error. The approximate full adders (AFA) are compared (Sunil Dutt et al., 2017) with the existing ripple carry adder (RCA) in terms of area and power. In Tongxin Yang et al. (2018), the approximate adder is based on the carry look ahead adder, and accuracy is realized by masking the carry propagation at run time. It results in reduced power and delay and is used for error tolerant applications. Approximate adders are used in data mining and multimedia signal processing, which can tolerate error, and the exact computing is not necessary. A 4-2 compressor tree was proposed (J.Anjana et al., 2018), and one of the Xor gate is replaced by OR gate to reduce the hardware requirement. Approximate multipliers are also designed (Kalvala et al., 2017; Suganthi et al., 2017) by using approximate adders, which are used in image processing applications. Algorithmic noise Tolerant (ANT) schemes (Rajamohana Hegde et al., 2001) are used to compensate the degradation of the algorithmic performance due to input dependent errors, and this error control scheme is used in soft DSP. Prediction based error control scheme was proposed to improve the performance of the filtering algorithm even when the errors occurred due to the approximate computation. Approximate computing was used in DCT image compression (Haider A.F.Almurib et al., 2018; S Geetha and P Amritvalli. 2017). A set of images are compressed to analyze the different parameters such as delay, energy consumption, and PSNR.

Accurate adders (G. Narmadha et al., 2015 and 2016; Manickam Ramasamy et al., 2019) are also designed, implemented, and analyzed for achieving the power efficiency and reducing the hardware requirement. Section 2 depicts the existing approximate adder structures. Section 3 presents the proposed approximate adder structure. Section 4 provides the performance analysis of existing and proposed approximate adders. This paper concludes with section 5.

EXISTING APPROXIMATE ADDER STRUCTURES

In R. Jothin et al. (2018), MBAFA1 and MBAFA2 have been designed to reduce the number of gates required and delay with minimum errors. MBAFA1 and MBAFA2 are shown in Figures 1 and 2, respectively, and are assumed as Approximate 1 and 2. Adder has three inputs A, B, and C and two outputs sum and carry. The outputs of single bit accurate and approximate full adders are given in Table 1.

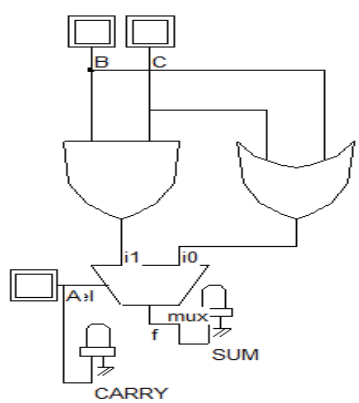

Figure 1. Multiplexer Based Approximate Full Adder 1(MBAFA1)-Approximate 1.

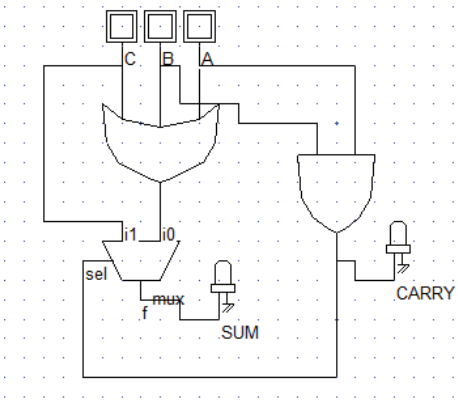

Figure 2. Multiplexer Based Approximate Full Adder 2 (MBAFA2)-Approximate 2.

Approximate adders have been designed by using Carbon Nano Tube Field Effect Transistor (CNFET) in Fazel Sharifi et al. (2017) to reduce the power consumption, and its design in terms of gates was shown in Figure 3. This design was assumed as Approximate 3.

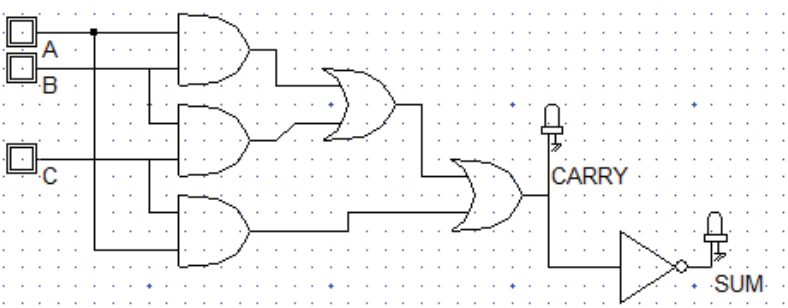

Figure 3. Approximate 3.

In Jeevan Jot Singh et al. (2018), different types of inexact adders have been designed for image compression techniques. These designs are taken as Approximate 4, Approximate 5, and Approximate 6 and are given in Figure 4, Figure 5, and Figure 6 respectively. Approximate adder 4 incurs a smaller number of gates and reduces the chip size.

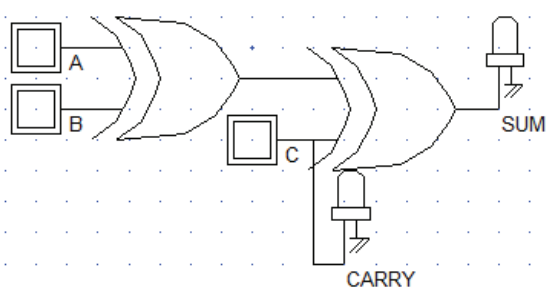

Figure 4. Approximate 4.

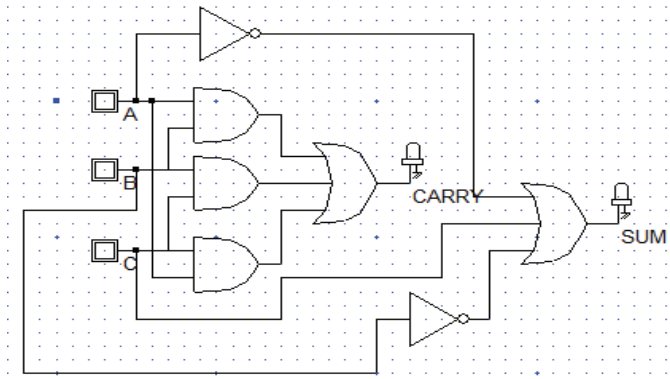

Figure 5. Approximate 5.

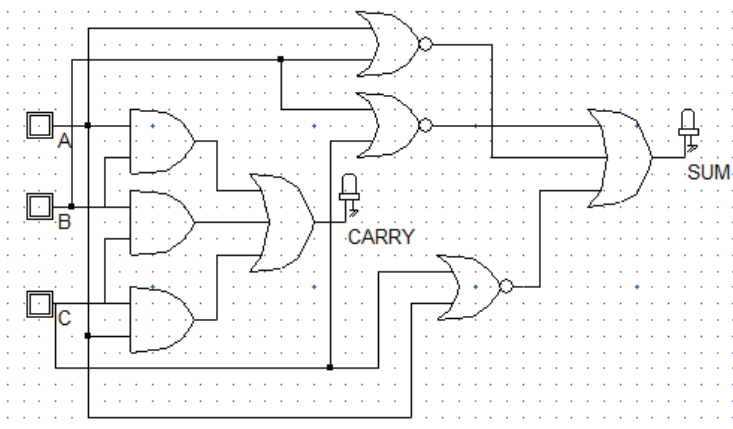

Figure 6. Approximate 6.

XNOR and XOR based adders have been designed in Zhixi Yang et al. (2013) to reduce the count of transistors and power. The three types of adders are assumed here as Approximate 7, Approximate 8, and Approximate 9. The corresponding design using gates is shown in Figure 7, Figure 8, and Figure 9 respectively.

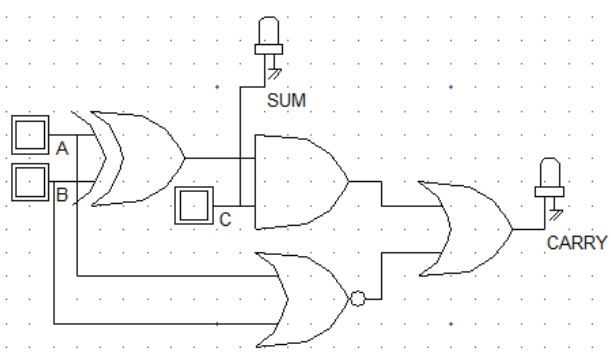

Figure 7. Approximate 7.

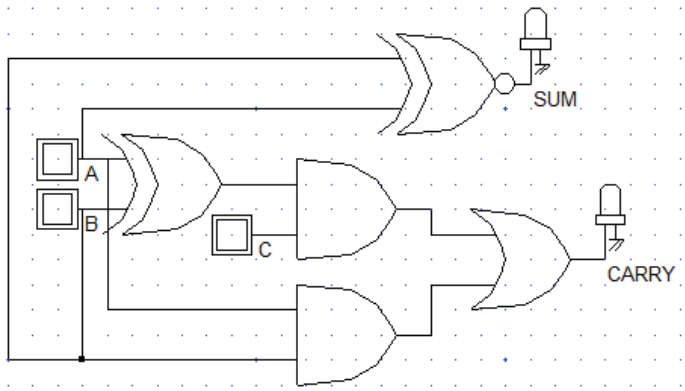

Figure 8. Approximate 8.

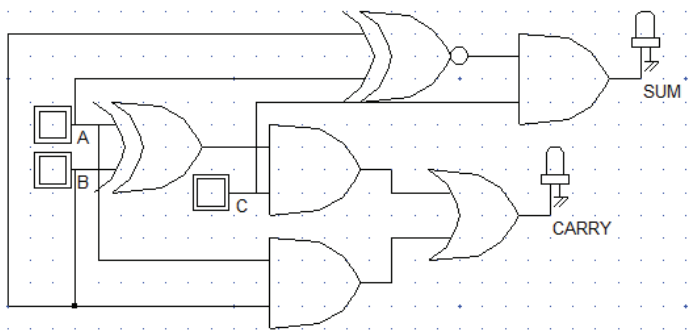

Figure 9. Approximate 9.

Area efficient and low power approximate multipliers have also been designed in Suganthi et al. (2017) by using approximate adder shown in Figure 10, which is assumed as Approximate 10. In accurate adder, 2 XOR gates are required for sum generation. To reduce the transistor count, one of the XOR gate is replaced by OR gate in sum generation and carry was generated by using only one AND gate. High speed error tolerant adder has also been designed for image processing and multimedia applications (S Geetha et al., 2017) and is shown in Figure 11. This type of adder is assumed as Approximate 11. These types of adders are used in Discrete Cosine Transform (DCT) and Inverse Discrete Cosine Transform (IDCT) for image compression techniques.

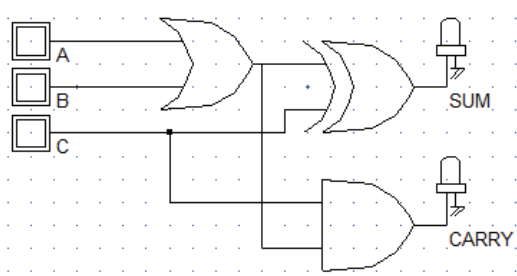

Figure 10. Approximate 10.

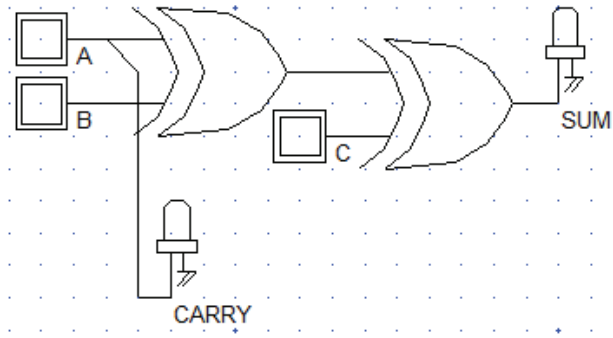

Figure 11. Approximate 11.

Various approximate adders have been discussed and its performance gets differed based on the design parameters such as area, power and delay.

PROPOSED APPROXIMATE ADDER

In order to reduce the transistor count, chip size and power consumption with minimum error, an efficient approximate adder is proposed. It consists of only one OR gate and one XOR gate for sum term and no gates for carry term. The proposed design is shown in Figure 12 and its sum and carry equations are given below.

SUM = (A XOR B)+C
CARRY = A

Output terms of existing and proposed designs are given in Tables 1 and 2 with the representation of errors in output terms. Proposed design has a smaller number of errors with the minimum chip size, low power consumption and high speed.

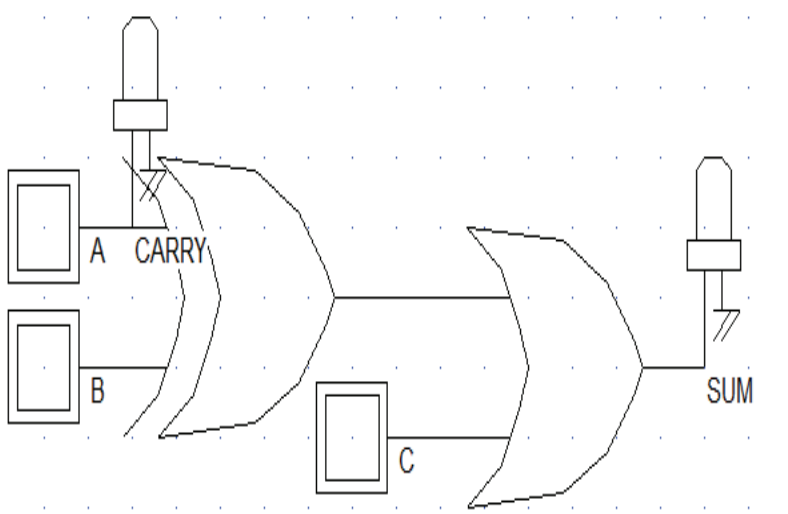

Figure 12. Proposed Approximate Adder.

Table 1. Output of Existing Approximate Adders 1–6.

INPUTS			OUTPUTS		R. Jothin et al., 2018				Fazel Sharifi et al., 2017		Jeevan Jot Singh et al., 2018					
			Accurate		Approximate 1		Approximate 2		Approximate 3		Approximate 4		Approximate 5		Approximate 6	
A	B	C	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
0	0	1	1	0	1	0	1	0	1	0	1	1	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	1	0	1	1	0	1	0	0	1	0	1	1	1	0	1
1	0	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	0	0	1	0	1	1	1	0	1
1	1	0	0	1	0	1	0	1	0	1	0	0	0	1	0	1
1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1

Table 2. Output of Existing Approximate Adders 7 – 11 and Proposed Adder.

INPUTS			Zhixi Yang et al., 2013						Suganthi et al., 2017		S Geetha et al., 2017		Proposed	
			Approximate 7		Approximate 8		Approximate 9		Approximate 10		Approximate 11			
A	B	C	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	0	1	0	0	0	0	1	0	1	0	1	0
0	1	1	1	0	0	1	0	1	0	1	0	0	1	0
1	0	0	0	1	0	0	0	0	1	0	1	1	1	1
1	0	1	1	0	0	1	0	1	0	1	0	1	1	1
1	1	0	0	1	1	1	0	1	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1	0	1	1	1	1	1

PERFORMANCE ANALYSIS

The existing approximate adders and proposed approximate adder are simulated by using Microwind 3.0 with 0.12µm CMOS technology. The design parameters like chip size, number of transistors, power consumption, and speed are observed for all the designs and its results are given in Table 3. Error Distance is the difference between the accurate result (Y) and approximate result (Y'). The total error distance can be calculated by the sum of error distance which is calculated for all the inputs.

Error Distance = (Y – Y')
Total Error Distance = ∑ (Error Distance for all the input combinations)
Total Error distance is also mentioned in Table 3.

Table 3. Simulation Results of Existing and Proposed Approximate Adders.

Adder Type	No. of transistors	Chip Size (Width X Height) (µm)	Power Consumption in (nW)	Frequency (GHz)	Total Error Distance
Approximate 1	18	13 X 12	4.095	0.167	4
Approximate 2	20	14 X 12	3.559	0.25	4
Approximate 3	32	15 X 11	7.057	0.25	2
Approximate 4	12	8 X 10	4.052	0.25	2
Approximate 5	38	17 X 12	6.824	0.25	2
Approximate 6	46	19 X 12	7.762	0.25	2
Approximate 7	22	11 X 11	5.11	0.333	8
Approximate 8	30	15 X 12	5.26	0.25	4
Approximate 9	36	17 X 12	5.424	0.25	2
Approximate 10	18	10 X 10	3.297	0.25	2
Approximate 11	12	8 X 10	8.663	0.25	2
Proposed	12	7 X 10	1.832	0.965	4

From the Table 3, it is evident that the proposed adder yields better performance when compared to the existing approximate adders in terms of power consumption and speed. The performance of approximate adders is compared based on the power consumption and frequency and are shown in Figure 13 and Figure 14 respectively.

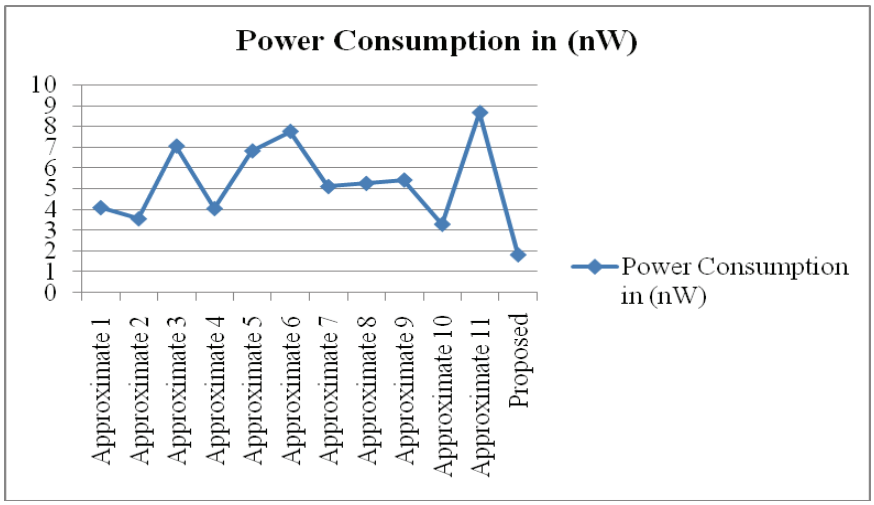

Figure 13. Power Consumption of Approximate Adders.

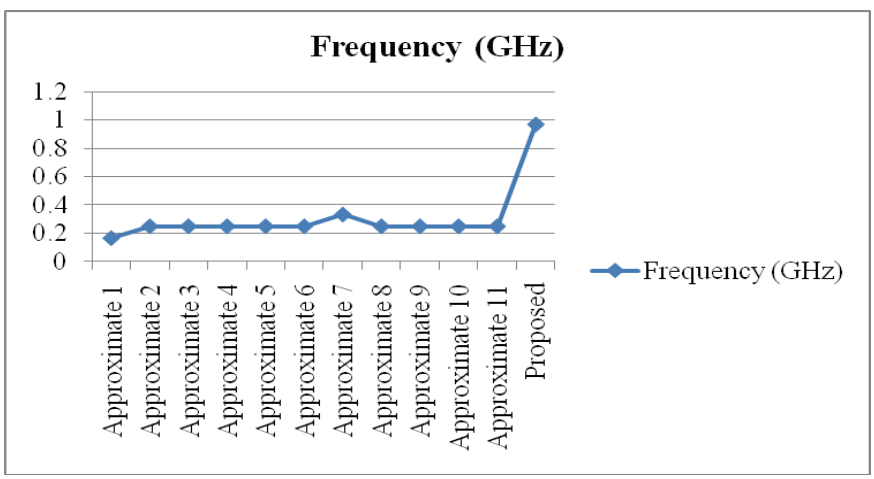

Figure 14. Frequency or speed of operation by Approximate Adders.

CONCLUSION

This paper depicts the overall view of existing approximate adders also, a new high speed and low power efficient adder is proposed. Performance comparison is made based on the design parameters. The proposed adder results in extremely low power and high speed with the minimum number of transistors. So, the chip size also gets reduced compared to the other existing designs. Approximate 11 consumes more power and so, the power consumption is reduced by 78.85% with the proposed adder design. When considering the frequency, that is, the speed of operation, Approximate 1 has the low frequency thereby, the frequency is increased by 65.38 % with the proposed design. In Approximate 4 and Approximate 11, two XOR gates are used, whereas, in the proposed adder, one XOR and one OR gate is used. So, one XOR gate is replaced by one OR gate in the proposed adder. The delay incurred for OR gate is low compared to the XOR gate. Hence, the speed of the proposed adder is automatically increased when compared to Approximate 4 and Approximate 11. Because of the same reason, power consumption

is also reduced. If the proposed adder is enhanced to various bit sizes for different applications, it will result in high speed and, reduced area with low power consumption. Mostly, the approximate adders are used in multimedia applications and in DCT for image compression techniques, where the accuracy is not a constraint. So, the proposed design can be used for achieving better performance in implementing the image processing applications with FPGA.

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