Designing programmable parallel LFSR using parallel prefix trees

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ABSTRACT

The throughput of an LFSR (Linear Feedback Shift Register) is affected by the sampling rate as well as the clock rate. On the other hand, the system-level characteristics of an LFSR such as its error detection capabilities are determined by the generating polynomial. Parallel LFSRs aim at improving the sampling rate in order to meet high throughput demands in parallel transmission or computation environments. Moreover, programmable LFSRs provide more system-level flexibility by allowing different generating polynomials to be used. Thus, using programmable parallel LFSRs looks an attractive solution to improve both throughput and system-level parameters. Programmable parallel LFSRs can be useful in stream ciphers, microprocessors, and many other environments. But parallelism and programmability can reduce the clock rate by increasing the logical depth and increase power and area by increasing the number of gates. Thus, we will need an efficient solution to manage the tradeoffs. This paper proposes an approach based on Parallel Prefix Trees (PPTs) to design programmable parallel LFSRs. PPTs are a family of topologies previously used in the design of parallel arithmetic circuits in order to manage the tradeoff between different circuit-level parameters. Our approach allows designers to use different PPTs in order to improve different circuit level parameters. A sample PPT-based programmable parallel LFR is designed and evaluated. Empirical results show more than 23% improvement in throughput and more than 27% improvement in area compared to state-of-the-art programmable parallel LFSR architectures.

Keywords: Parallel Prefix Tree; Parallel LFSR; Programmable LFSR; Brent-Kung; Programmable Parallel LFSR.

INTRODUCTION

Linear Feedback Shift Registers (LFSRs) are widely used in real-world applications such as generating and checking error detection codes (Wu, 2015; Parhi, 2004; Zhang et al., 2005), sequence generation and Pseudo-Random Number Generation (PRNG) (Li et al., 2016; Rahimov et al., 2011), Automatic Test Pattern Generation (ATPG) (Acevedo et al., 2016; Pomeranz, 2016), Built-In Self-Test (BIST) (Ying et al., 2018; Xiang, el at., 2017; Yasodharan et al., 2014; Acevedo et al., 2015), coding and cryptography (Mashhady et al., 2015; Upadhyay et al., 2015; Matsui, 2014; Lee et al., 2014), and modular arithmetic computation (Morales-Sandoval et al., 2009). Therefore, these circuits are of much importance to the designers and the researchers (Li et al., 2017; Wang et al., 2016). LFSRs may occasionally be implemented in software (Delgado-Mohatar et al., 2011), but the common trend is to implement them in hardware by forming a shift register with a feedback loop and a number of $GF(2)$ addition elements (XOR gates) that are essentially used to accomplish $GF(2)$ polynomial division.

An LFSR is specified by its generating sequence that determines the locations of $GF(2)$ addition elements on the feedback loop. The binary generating sequence can be represented by a $GF(2)$ polynomial that is called the generating polynomial. The degree of an LFSR is defined as the number of flip-flops constructing the LFSR or equivalently the degree of its generating polynomial.

There are two types of LFSRs: Fibonacci-type LFSRs and Galois-type LFSRs (Wei et al., 2015; Pomeranz, 2017). The XOR gates lay on the feedback loop in the former type and out of the feedback loop in the latter. The two types can
be converted to each other by reversing the generating sequences and selecting proper initial values (Dubrova, 2009). Figure 1 shows two counterpart LFSRs, one of which is of Fibonacci type and the other is of Galois type. In this paper, the focus is on Galois-type LFSRs because they are more common in real-world applications due to their lower delay in the feedback loop, which allows higher clock frequencies. We also assume that LFRS are implemented using XOR gates although they have occasionally been implemented using XNOR gates (Ahmad et al., 2008).

![A Galois-type LFSR](image1)

![A Fibonacci-type equivalent](image2)

**Fig. 1.** Fibonacci and Galois type LFSRs.

A programmable LFSR is an LFSR that can operate on any generating sequence with a given length in contrast with a static LFSR, which operates only on a specific generating sequence.

Programmability provides system-level design flexibility by allowing the designers to select among different generating sequences. For instance, in LFSR-based error detection systems, programmability allows detecting different categories of errors by choosing different generating sequences. Programmable LFSRs have been of particular interest for researchers during the last decades (Ren et al., 2015; Gai et al., 1986; Toal et al., 2009; Grymel et al., 2011). For example, it has been proposed to use a single programmable LFSR in a microprocessor for many applications such as cryptography, BIST, and PRNG, each of which requires its own generating function (Gai et al., 1986). A programmable LFSR is shown in Figure 2.

![Fig. 2. A programmable LFSR of degree n.](image3)

In this figure, \( F_i \) through \( F_n \) are the flip-flops that form the shift register and the XOR gates perform the \( GF(2) \) additions if enabled by the corresponding AND gates according to the generating sequence \((D_n \ldots D_1 \ldots D_1 \ldots D_0)\). The input sequence \((M_i \ldots M_1 \ldots M_0)\) is fed into the LFSR one bit per clock. It should be noted that there may be LFSRs, into which no data enters except the initial values loaded in flip-flops. In such a case, it can be assumed that \( M_i = \ldots = M_1 = M_0 = 0 \).
Since LFSRs sample one single bit in each clock cycle, they may not be able to provide adequate throughput in applications where data stream arrives at a rate higher than one bit per clock or in applications in which data should be processed in words. This problem can be solved by using parallel LFSRs. An \( n \)-bit \( j \)-parallel LFSR (\( j > 1 \)) is a circuit that performs the same function as an ordinary \( n \)-bit LFSR but samples \( j \) bits in each clock cycle. Therefore, parameter \( j \) can be viewed as the sampling rate of a parallel LFSR.

The two notions of programmability and parallelism in LFSRs can be combined together to form a programmable parallel LFSR, in which the generating sequence can be changed depending on the application while the overall structure remains parallel. Figure 3 shows a schematic representation of such a circuit. In this figure, \( F_i^k \) represents the value of flip-flop \( F_i \) after \( k \) iterations. The oval box represents a combinational circuit that takes \( F_0^0 \) through \( F_n^0 \) along with \( M_0 \) through \( M_{j-1} \) and \( D_0 \) through \( D_n \) as input and produces \( F_1^j \) through \( F_n^j \) as output.

If, in addition to the generating sequence, the operational mode of a parallel LFSR is also adjustable, then a reconfigurable parallel LFSR is formed. It has been shown that this level of reconfigurability has an adverse effect on the logical depth and performance of a parallel LFSR (Zibin et al., 2013; Savic et al., 2014). On the other hand, programmability of the generating sequence often provides sufficient flexibility without sacrificing performance (Toal et al., 2009; Grymel et al., 2011). Therefore, this paper focuses only on programmable parallel LFSRs.

![Fig. 3. A programmable \( n \)-bit \( j \)-parallel LFSR.](image)

Programmable parallel LFSRs, as they are, provide system level design flexibility as well as high performance. What we are seeking in this paper is adding circuit level design flexibility. We are going to present a flexible architecture for designing programmable parallel LFSRs that allows designers to select among a variety of design options. This will make it possible to choose among various tradeoff points depending on design objectives and constraints on sampling rate, clock period, and area. Similar research works have previously been presented in the area of arithmetic circuits on the basis of PPTs (Zarandi et al., 2014). Among the PPTs used in arithmetic circuit design, we can refer to Brent-Kung, Kogge-Stone, Sklansky, Knowles, Han-Carlson, and Lander-Fischer PPTs (Harris, 2003). Taxonomies and characterizations presented in this regard show that selecting different kinds of PPTs can improve different circuit level parameters. This helps the designers maneuver in a space of design schemes to manage the tradeoffs according to design constraints and objectives (Harris, 2003; Hoe et al., 2011).

The rest of this paper is organized as follows. Section 2 studies relevant works. Section 3 establishes a relation between programmable parallel LFSRs and PPTs. Section 4 discusses the design details. Section 5 presents the results of evaluations. Section 6 concludes the paper and suggests further works.
RELATED WORKS

There are two categories of research works that can be considered relevant to this work. The first category consists of those related to the design of reconfigurable parallel LFSR and the second includes those related to PPT-based parallel logic circuits. Each of the two categories will be discussed in the next section.

Reconfigurable and Programmable Parallel LFSR

The design of parallel LFSR has been the focus of research for the last two decades (Hu et al., 2017; Kim et al., 2015). There are various approaches to design such circuits (Panda et al., 2014; Singh et al., 2013; Manikandan et al., 2013). For example, an approach based on the Chinese Remainder Theorem (CRT) has been proposed in Chen (2009). An approach based on transition and control matrices has also been proposed in Grymel et al. (2011). There are also approaches based on division on shorter generating polynomials with less feedback terms (Glaise, 1997). Moreover, there are special techniques for designing parallel LFSRs for specific applications. For example, in Condo et al. (2014) a variable-parallelism parallel LFSR has been proposed for 3GPP-LTE/LTE-Advanced applications. As another example, a parallel CRC computation circuit convenient for SoCs has been proposed in Toal et al. (2009). But the most relevant works are those proposing approaches based on unfolding, mathematical deduction, and recursive equations.

A common approach for the design of parallel LFSRs is unfolding, which essentially aims at revealing hidden concurrents in DSP programs. Unfolding was proposed and developed later as a technique for mitigating the problem of high fan-outs in LFSRs that affects the clock frequency (Zhang et al., 2005). Since this method leads to long clock periods and this adversely affects the throughput, it needed some optimizations in order to be convenient in high throughput parallel applications. For this purpose, techniques such as pipelining and retiming were considered later (Cheng et al., 2006). It has been proven that increasing the unfolding factor more than a specific threshold decreases throughput because of notable increase in the clock period. The literature comes with techniques for alleviating this problem (Cheng et al., 2009; Ayinala et al., 2011). Among these techniques, we can refer to those based on Look-ahead transformations (Lin et al., 2013).

Mathematical deduction (Parhi, 2004) is another approach that has been used by researchers to design parallel LFSRs. The main idea behind mathematical deduction is focusing on the mathematical function of the LFSR and designing circuits, which can implement the combined function of multiple iterations. Mathematical deduction may be based on recursive equations (Parhi, 2004).

There are also research works that present approaches based on look-ahead for designing parallel LFSRs (Lin et al., 2013).

On the other hand, there are several applications in which it is very useful to choose among a number of generating polynomials. For instance, we can refer to microprocessors performing LFSR instructions, multiple-standard modems, stream ciphers, and pseudo-random number generators. Programmable and reconfigurable LFSRs have been introduced in response to this demand (Ouahab et al., 2017; Mishra et al., 2016; Lama et al., 2016). Combining the notions of parallel LFSR and reconfigurable/programmable LFSR seems a natural idea to achieve the advantages of both notions (Wei et al., 2015). However, the existing programmable parallel LFSRs in the literature suffer from the lack of circuit-level design flexibility. In other words, their designs do not provide enough degree of freedom to efficiently manage the tradeoffs among different circuit-level design parameters such as delay and area.

The most relevant research works to which we compare our proposed architecture are Toal et al. (2009) and Grymel et al. (2011). A 4.92Gbps field programmable parallel CRC (Cyclic Redundancy Check) calculator has been designed, synthesized, and mapped to 130-nm UMC library in Toal et al. (2009) based on matrix calculations. In the proposed architecture, called cell array architecture, the main component consists of a number of configurable cells. Each cell includes two multiplexers, a configuration register, and an XOR gate. A preprocessing stage consisting of
a number of XOR gates along with a post-processing stage performing matrix multiplications is added to the main component. Another 15.38Gbps programmable parallel LFSR has been designed and mapped to the same library in Grymel et al. (2011). The latter programmable parallel LFSR uses XNOR gates and latches instead of multiplexers in the main component. We compare our proposed programmable parallel LFSR to these designs.

**PPT-based parallel logic circuits**

Parallel prefix trees have been studied for the last few decades (Harris, 2003). PPTs can be used as part of a parallel solution to any recursive equation provided that the recursive equation is stated using an associative operation. There are various families of PPTs with the same functionality but different structures (Jaberipur et al., 2015; Abdel-Hafeez et al., 2013; Hobson, 2015; Kumar et al., 2015). Their structural differences create differing implementation complexity (Sergeev, 2013), depth (Lin et al., 2009), deficiency (Zhu et al., 2006), fan-out (Lin et al., 2009), problem-size-independability (Lin et al., 2009), capability of running on parallel machines (Sergeev, 2013), convenience for running on pipeline systems (Santos, 2002), application in different branches of science (Lin et al., 2013), and implementation technology (Lin et al., 2003). PPTs have been previously used in the design of various parallel logic circuits. PPT-based parallel adders have been well studied, developed, and evaluated (Lina et al., 2005). The literature also comes with parallel priority encoders (Huang et al., 2002), parallel comparators (Abdel-Hafeez et al., 2013), parallel round robin arbiters (Ügurdag et al., 2012), and parallel, reverse converters (Panda et al., 2014) designed using PPTs.

**PPTs AND PROGRAMMABLE PARALLEL LFSRs**

PPTs are topologies originally presented to be used in prefix processing, which is a kind of parallelizable recursive computation. The prefix processing problem is the problem of calculating \( Y = \{ y_1, y_2, \ldots, y_n \} \) from \( X = \{ x_1, x_2, \ldots, x_n \} \) where \( \forall k \in \{1:n\}, y_k = x_k \circ \cdots \circ x_1 \) and “\( \circ \)” is an associative operation. In this paper, we define a LOO (Last Output Only) prefix processing problem as the problem of calculating only \( y_n = x_n \circ \cdots \circ x_1 \) from \( X = \{ x_1, \ldots, x_n \} \).

PPTs can also be modified to parallelize computations formalized as LOO prefix processing problems. To do this, we should simply remove the edges and nodes not contributing to the calculation of \( y_n \). Figure 4-a shows the Brent-Kung PPT for \( n = 5 \). Moreover, Figure 4-b shows a LOO PPT designed on the basis of the Brent-Kung topology for \( n = 5 \).

An obvious serial algorithm to solve a classical prefix processing as well as a LOO prefix processing problem is as follows.

\[
y_1 \leftarrow x_1
\]

\[
\text{For } i = 2 \rightarrow n \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \ quad
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Fig. 4-a The Brent-Kung topology for $n = 5$

Fig. 4-b The Brent-Kung LOO PPT for $n = 5$

Fig. 4. Sample PPTs for solving classical and LOO prefix processing problems.

There are two general challenges that need to be handled in order to use PPTs for parallelizing every sequential circuit. The first challenge is to restate the function of the sequential circuit in the form of a proper recursive equation. The second is to define a proper associative logic operation to convert the recursive equation to a prefix processing problem. These challenges motivate several research works (Esposito et al., 2016; Gurusamy et al., 2016; Hepzibha et al., 2016).

Let us resolve the first general challenge in the design of PPT-based programmable parallel LFSRs by deriving a recursive description of the sequential programmable LFSR shown in Figure 2. To do this, we derive the set of equations that state the value of each individual flip-flop at the end of the $k$th clock cycle, in terms of the values of the flip-flops in the $(k - j)$th cycle. This set of equations is referred to as the $j$th State Transition Equation System (STES) in this paper. The logic function of the programmable LFSR of Figure 2 can be modeled by the following equation.

$$F^n_k = D_{i-1}F^{k-1}_n + F^{k-1}_{i-1}$$

$$k \in [1, j]$$

(1)

In Equation 1, addition and multiplication operations are in $GF(2)$, $F^n_k$ denotes the value of $F_i$ in the $k$th iteration, and $F^{k-1}_n$ is the value of $F_i$ in the $(k - 1)$th cycle or equivalently the value on the feedback loop in the $k$th cycle. The initial value of the $i$th flip-flop is shown by $F^0_i$. Moreover, $D_i$ represents the $i$th least significant bit of the generating sequence. It is assumed that $D_n = 1$ and $D_0 = 1$ because the generating polynomial must be prime and of degree $n$ and indivisible by the GF(2) polynomial “x”.

During the recursive application of Equation 1, $D_i$ should be replaced by 0 if $i < 0$. Moreover, $F^0_i$ should be replaced by $M_{-i}$ for $i \leq 0$ in recursive applications of the equation.

The recursive nature of Equation 1 shows that we have overcome the first general challenge.
Now let us handle the second general challenge by defining a proper associative logic operation through which Equation 1 can be converted to a prefix processing problem. It can be easily shown that the AX (AND-XOR) operation, defined as follows, can meet this requirement.

\[
a \cup^D b = a + D \cdot b
\]

Equation

The circuit shown in Figure 5 implements an AX operation. This circuit can be used as a building block in the proposed programmable parallel LFSR.

Fig. 5. Logic implementation of the AX operation.

There is still an extra challenge to be handled, which is specific to programmable parallel LFSRs. The problem here is that the recurrence in Equation 1 should be resolved for two indices (i and k), while classical PPTs have been originally proposed to solve single-index recursive computing problems. We solve this problem by decomposing Equation 1 into two LOO prefix processing problems resolved using two cascaded stages of PPTs. The first PPT stage calculates \(F^k_i\) (the value on the feedback loop in the kth cycle) for \(k \in [1, j - 1]\). The second stage calculates \(F^i_j\) for \(i \in [1, n]\). The jth STES of a programmable parallel LFSR consists of the two mentioned equations. Figure 6 shows the architecture of a PPT-based programmable parallel LFSR designed based on this approach.

Fig. 6. The architecture of a PPT-based n-bit j-parallel programmable parallel LFSR.
Now let us start decomposing Equation 1. This equation can be expanded as follows.

\[ F_i^j = D_{i-1}F_n^{j-1} + F_{i-1}^{j-1} = \]
\[ D_{i-1}F_n^{j-1} + D_{i-2}F_n^{j-2} + F_{i-2}^{j-2} = \]
\[ D_{i-1}F_n^{j-1} + D_{i-2}F_n^{j-2} + D_{i-3}F_n^{j-3} + F_{i-3}^{j-3} = \]
\[ \cdots \]
\[ = \sum_{t=1}^{j} D_{i-t}F_n^{j-t} + F_i^0 \]
\[ i \in [1, n] \]  

(2)

Since \( D_i \)'s and \( F_n^i \)'s are given, the sum in Equation 2 can be computed using a PPT including associative AX operations if the \( F_n^k \)'s are known. The second PPT stage in Figure 6 is designed on the basis of this equation.

We can also calculate \( F_n^k \)'s using Equation 1 as follows.

\[ F_n^k = F_n^0 -k + \sum_{t=1}^{k} D_{n-t}F_n^{k-t} \]
\[ k \in [1, j] \]  

(3)

The sum in Equation 3 can also be computed using another PPT, which constructs stage 1 of the architecture shown in Figure 6. Equations 2 and 3 form the \( j \)th STES of the programmable parallel LFSR of Figure 2. Equation 2 actually represents \( n \) equations for \( n \) different values of \( i \). We refer to these equations as the \( j \)th stage 2 STES equations in this paper. Also Equation 3 represents \( j \) equations for \( j \) different values of \( k \). The latter are referred to as the \( j \)th stage 1 STES equations in this paper.

THE DESIGN METHOD

In this section, we design a programmable 8-bit 5-parallel LFSR using the proposed method to illustrate how the method works.

The Design of the First Stage

According to Equations 3, the \( 5 \)th stage 1 STES equations of a programmable parallel LFSR of degree 8 are as follows.
\[ F^1_8 = F^0_7 + D_7 F^0_8 \]

\[ F^2_8 = F^0_6 + D_7 F^1_8 + D_6 F^0_8 \]

\[ F^3_8 = F^0_5 + D_7 F^2_8 + D_6 F^1_8 + D_5 F^0_8 \]

\[ F^4_8 = F^0_4 + D_7 F^3_8 + D_6 F^2_8 + D_5 F^1_8 + D_4 F^0_8 \]

\[ F^5_8 = F^0_3 + D_7 F^4_8 + D_6 F^3_8 + D_5 F^2_8 + D_4 F^1_8 + D_3 F^0_8 \]  \( \text{(3)} \)

Each of the above equations represents a LOO prefix processing problem, which can be parallelized using a PPT. Figure 7 shows the first stage of a programmable 8-bit 5-parallel LFSR designed without the use of any PPT. Figure 8 shows the same circuit in which every LOO prefix processing problem has been solved using a Brent-Kung PPT. This circuit has been designed as a sample by feeding the AX operation as a building block into the Brent-Kung topology.

**The Design of the Second Stage**

According to Equations 2, the 5\textsuperscript{th} stage 2 STES equations of a programmable parallel LFSR of degree 8 are as follows.

\[ F^5_1 = D_0 F^4_8 + M_4 \]

\[ F^5_2 = D_1 F^4_8 + D_0 F^3_8 + M_3 \]

\[ F^5_3 = D_2 F^4_8 + D_1 F^3_8 + D_0 F^2_8 + M_2 \]

\[ F^5_4 = D_3 F^4_8 + D_2 F^3_8 + D_1 F^2_8 + D_0 F^1_8 + M_1 \]

\[ F^5_5 = D_4 F^4_8 + D_3 F^3_8 + D_2 F^2_8 + D_1 F^1_8 + D_0 F^0_8 + M_0 \]

\[ F^5_6 = D_5 F^4_8 + D_4 F^3_8 + D_3 F^2_8 + D_2 F^1_8 + D_1 F^0_8 + F^0_1 \]

\[ F^5_7 = D_6 F^4_8 + D_5 F^3_8 + D_4 F^2_8 + D_3 F^1_8 + D_2 F^0_8 + F^0_2 \]

\[ F^5_8 = D_7 F^4_8 + D_6 F^3_8 + D_5 F^2_8 + D_4 F^1_8 + D_3 F^0_8 + F^0_2 \]  \( \text{(2)} \)
Fig. 7. The first stage of the programmable 8-bit 5-parallel programmable LFSR.

Fig. 8. The first stage of the programmable 8-bit 5-parallel programmable LFSR using Brent-Kung PPT.

Again, each of the above equations represents a LOO prefix processing problem, which can be parallelized using a PPT. Figure 9 shows a sample implementation for the second stage of the PPT-Based programmable 8-bit 5-parallel LFSR. Again, it has been constructed through applying the AX operation into the Brent-Kung topology.

It should be noted here that an independent PPT should be selected for parallelizing every individual LOO prefix processing problem in the STES. The selected PPTs can be mutually different or the same according to the design objectives. Thus, this approach gives the designer at least $n + j$ options in the circuit-level design space. This is the main contribution of this paper. In Figure 8, we have selected the Bren-Kung PPT only to illustrate the design process.
The Design of the Post Processing Module

The post processing stage should convert $\sum_{t=1}^{k} D_{i-t} F_n^{q-t}$ to $F_n^k = F_n^{0-n-k} + \sum_{t=1}^{k} D_{n-t} F_n^{k-t}$ for every $q \in [0, n-1]$. This stage does not depend on the generating sequence. In this stage, $D_{i-t}$ should be replaced by 0 if $i-t < 0$ and $F_n^{0-n-min(k,f)}$ should be replaced by $M_{k-n}$ if $n - k \leq 0$. The following figure shows the third stage for the 8-bit 5-parallel LFSR.

Pipelined Design

A PPT-based $n$-bit $j$-parallel programmable LFSR can be designed in a pipelined form. Let us assume that we can write $j$ as the product of $e$ and $f$ ($j = e \cdot f$). We can construct a PPT-based $n$-bit $j$-parallel programmable LFSR of $e$ cascaded $n$-bit $f$-parallel programmable LFSRs with latches between them. A sample pipelined implementation is shown in the next section. In this case, our approach will give the designers $e \cdot (n + f) = e \cdot n + e \cdot f$ options, which will obviously be more than $n + j = n + e \cdot f$ assuming $e > 1$. 

Fig. 9. The second stage for a programmable 8-bit 5-parallel LFSR.
EVALUATION

As mentioned in previous sections, PPT-based programmable parallel LFSR aims at allowing designers to maneuver in a large space of tradeoff points in order to meet circuit level design objectives. Let us assume here that the design objective is to maximize the throughput. The reason for making such an assumption is that the state-of-the-art programmable parallel LFSRs have considered throughput as the main objective (Toal et al., 2009; Grymel et al., 2011). With such an objective, the main tradeoff in current research works is the tradeoff between the sampling rate and the clock frequency. The reason is that programmability and parallelism both increase the logical depth and consequently tend to reduce the clock frequency. It can be shown that the Brent-Kung topology minimizes the logical depth (Harris, 2003). Thus, we will use the Brent-Kung PPT to solve all LOO prefix processing problems in the design of our programmable parallel LFSR in this section. We will compare Brent-Kung programmable parallel LFSR with the art programmable parallel LFSRs presented in Toal et al. (2009) and Grymel et al. (2011) in terms of throughput, area, and power to highlight the tradeoffs.

The degree of the generating polynomial and the sampling rate are both equal to 32 similar to Toal et al. (2009) and Grymel et al. (2011). Pipelining has been applied to the design. The PPT-based 32-parallel Programmable LFSR has been designed by cascading 8 instances of a 4-parallel programmable LFSR. Figure 11 shows the pipelined architecture.
VHDL code has been used with ModelSim in the design phase and 130-nm TSMS technology has been used with Synopsys Design Compiler in the synthesis phase with the objective of overall optimization. In Figure 11, $L_i^k$ is the $i$th latch temporarily storing $F_i^{4,k}$. 

Fig. 11. Pipelined programmable 32-bit 32-parallel LFSR.
Table 1. Comparison.

<table>
<thead>
<tr>
<th></th>
<th>TR</th>
<th>GR</th>
<th>Proposed</th>
<th>Improvement TR</th>
<th>Improvement GR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Frequency</td>
<td>154 MHZ</td>
<td>481 MHZ</td>
<td>592 MHz</td>
<td>284%</td>
<td>23%</td>
</tr>
<tr>
<td>Throughput</td>
<td>4.92 Gbps</td>
<td>15.38 Gbps</td>
<td>18.94 Gbps</td>
<td>284%</td>
<td>23%</td>
</tr>
<tr>
<td>Total Power</td>
<td>12.21 mw</td>
<td>14.74 mw</td>
<td>18.42 mw</td>
<td>-51%</td>
<td>-25%</td>
</tr>
<tr>
<td>Total Area</td>
<td>0.150 mm²</td>
<td>0.033 mm²</td>
<td>0.024 mm²</td>
<td>72%</td>
<td>27%</td>
</tr>
</tbody>
</table>

In the above table, TR represents the programmable parallel LFSR designed in Toal et al. (2009) and GR represents the one designed in Toal et al. (2009). The above table shows a tangible improvement in the throughput (284% against TR and 23% against GR) and area (72% against TR and 27% against GR). But as shown in the table, this improvement is gained at the cost of increased power. This clarifies the reason why we have not used FPGAs in our design. FPGAs are widely used for rapid prototyping as well as a standalone product. However, they suffer from high power consumption due to their internal structure. As such, using an FPGA to measure the power consumption of a circuit is not a viable option and, therefore, is not common in the literature.

There is another point to consider regarding the tradeoff between area and power; reducing the area does not necessarily reduce the power. This is due to the fact that eliminating some circuit elements might increase the activity of others. The extra activity imposed on other resources might increase their dynamic power consumption. This is indeed the case when one moves from an ordinary serial LFSR to a parallel one.

CONCLUSIONS AND FURTHER WORKS

In this paper, a PPT-based architecture was presented for designing programmable parallel LFSRs using simple building blocks. This architecture allows designers to select among a variety of PPT topologies to maneuver in a large space of tradeoff points with respect to circuit level design objectives and constraints. We illustrated how it is possible to improve throughput and area using this approach at the cost of increased power. Presenting taxonomy of prefix-based programmable parallel LFSRs designed on the basis of different PPT topologies is suggested as further work. The work of this paper can also be continued by developing novel PPT topologies for improving parameters such as throughput and power in PPT-based programmable parallel LFSRs.

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تحسين متوازية قابلة للاستخدام LFSR

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الخلاصة

تتأثر انتاجية سجلات التغذية الخفية المرجوة (LFSR) معدل اختيار العينات بالإضافة إلى معدل التزامن. من ناحية أخرى، يتم تحديد الخصائص على مستوى النظام من LFSR، مثل: القدرة على اكتشاف الأخطاء، بواسطة توليد متعددة الحدود. تهدف المتوازية إلى تحسين معدل اختيار العينات من أجل تلبية متطلبات الانتاجية العالية في بيئة الرسالة أو الحزمة LFSRs المتوازية. علاوة على ذلك، توفر المتوازية LFSRs القابلة للبرمجة المزدوج من المرونة على مستوى النظام من خلال السماح باستخدام LFSRs المتوازية القابلة للبرمجة بدون حلاء جاذبا لتحسين كل من معلمات المتوازية LFSRs المتعددة الحدود المختلفة. وبالتالي، فإن استخدام المتوازية LFSRs الإنتاجية ومستوى النظام. وقد تكون المتوازيّة قابلة للبرمجة مفيدة في التشغيل الابتكاري، والعروض الدقيقة والعديد من البيئات الأخرى. ولكن التوازي وقابلية البرمجة يمكن أن يعملا على التقليل من معدل التزامن عن طريق زيادة العميق المنطقي وزيادة الطاقة والمساحة عن طريق زيادة عدد الطرق. وبالتالي، سنحتاج إلى حل فعال لإدارة المقارنات. يقترح مجموعة PPTs المتوازية القابلة للبرمجة (PPTs) لتصميم المتوازية LFSRs هذه البحث نهج يركز على أشياء بادئة متوازية من الطيور الحسابية المتوازية من أجل إدارة المقارنات بين المعلوما المختلفة لمستوى الدائرة. وهذا النهج يسمح للمصممين باستخدام أنواع PPTs مختلفة لتحسين مختلف العناصر لمستوى الدائرة. تم تصميم وتقسيم نجاح متوازي قابل للبرمجة يركز على PPT وأظهرت النتائج التجريبية تحسن في الإنتاجية بنسبة تزيد عن 23 PPT وكذلك تحسن بنسبة تزيد عن 27 % في المادة مقارنة بخدمة LFSR المتوازية البرمجية الحالية.