

# Investigation of the effect of the gap at the zero-crossing point of PWMs creating the first level voltage in a multi-level inverter

Erol CAN\*, HASAN HÜSEYİN SAYAN\*\*

\*Department of Aviation Electric Electronics, School of Civil Aviation, Erzincan Binali Yıldırım University, Erzincan

\*\*Department Of Electrical Electronics Engineering, Faculty of Technology, Gazi University, Ankara

Corresponding Author: cn\_e@hotmail.com

**Submitted** : 12-10-2021

**Revised** : 30-12-2021

**Accepted** : 09-01-2022

## ABSTRACT

The usage of multi-level inverters in converting direct current to alternating current is one of the most demanded and used methods. While creating multi-level voltage with inverters, the operating times of the switches that constitute the first step of the alternating voltage determine the gap of the step at the zero-crossing point. This situation can be preferred to create an extra level. Therefore, this article examines the effect of variation in operating times and frequencies of first-step PWMs on this zero-crossing point. First, the inverter structure providing load voltage is given in the study. Then, the transition of PWM run times is tried for different first-level voltages on the loads. The results obtained show the operation times of PWM at the transition point are quite effective on the load currents and voltages.

**Keywords:** Zero-Point Crossing; PWM Operating; Different First-Level.

## 1. INTRODUCTION

Obtaining and converting electrical energy are very technical and important studies. The usage of multi-level inverters in electrical energy conversion is a very common practice ( Sarebanzadeh, et al., 2021; Gupta, 2022; Can, 2021; Can, E. 2020a.). While generating multi-level voltage with inverters on the load, it is desired that the Total Harmonic Distortion (THD) of this voltage is low or within international standards (Abbas, et al 2021; Barbie, et al 2021; Can, et al 2017). In order to reduce the harmonic distortion of the generated energy and to obtain energy close to the sine; some studies present multi-level inverter designs (Dhanamjayulu, et al., 2021; Hassan, et al., 2021; Can, et al., 2020b), while some studies focus on PWM and the pulse width modulation controlling the inverters (Padmanaban, et al., 2021; Lee, et al., 2015; Law, et al., 2017). Although it has been shown that the source values used for the inverter levels have an effect on the distortion (Can, 2019), the effect of the operation rates of the PWMs which constitute the first step in multi-level inverters has not been revealed. In this study, the effect of PWM operating times at the zero-crossing point of the first level voltage on the energy quality is investigated. In order to examine the effect of the first-level voltages of PWMs, the structure, and operation of the nine-level inverter are introduced in the second chapter. In the third part, the system is tested by using different Sine Pulse Width Modulation (SPWM) creating the first level voltage. The results obtained reveal that the operating times of the PWMs at the first transition point have a significant effect on the alternating electrical energy generated on the load.

## 2. NINE-LEVEL INVERTER AND OPERATION LOGIC

There are 9-IGBT switches as power switches in the nine-level inverter structure. These switches are from I0 to I9. Again, there are four Direct currents (DC) of voltage sources in the inverter structure. These sources are from Vdc1 to Vdc4. While the inverter circuit structure is given in Figure 1, the working order of the source and switches is given in Table 1.

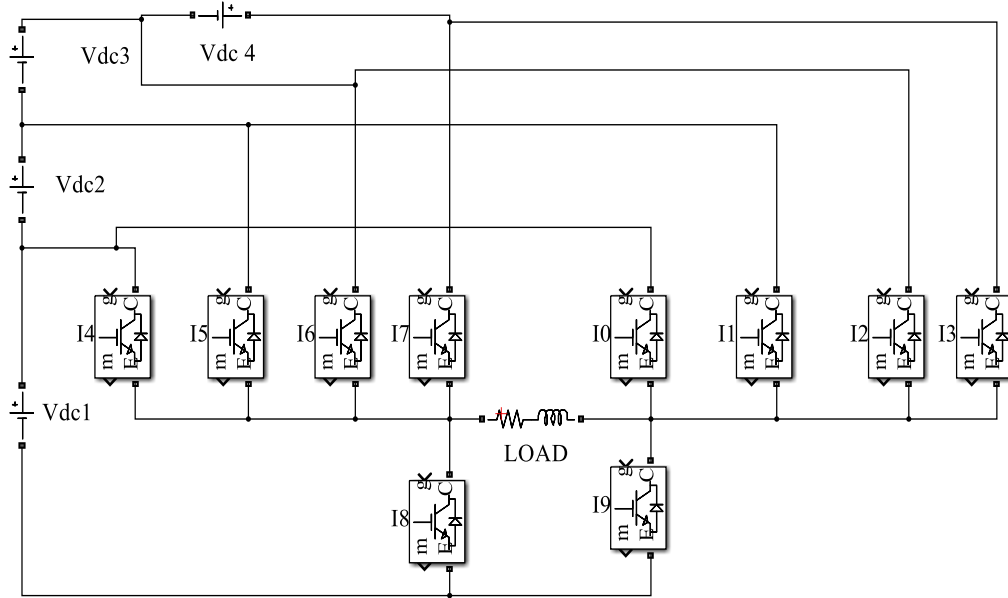


Figure 1. the inverter circuit structure

Table1: the working order of the source and switches

Vdc.1	Vdc.2	Vdc.3	Vdc.4	I0.	I1.	I2.	I3.	I4.	I5.	I6.	I7.	I8.	I9.
1	0	0	0	0	0	0	0	1	0	0	0	0	1
1	1	0	0	0	0	0	0	1	1	0	0	0	1
1	1	1	0	0	0	0	0	1	1	1	0	0	1
1	1	1	1	0	0	0	0	1	1	1	1	0	1
1	0	0	0	1	0	0	0	0	0	0	0	1	0
1	1	0	0	1	1	0	0	0	0	0	0	1	0
1	1	1	0	1	1	1	0	0	0	0	0	1	0
1	1	1	1	1	1	1	1	0	0	0	0	1	0

To create the first step of alternating voltage, the Vdc1 source is applied to the load with switches I4 and I9 for the positive side of voltage to be created, while Vdc1 is delivered to the load with I0 and I8 for the negative side of the voltage. To create the second level of the alternating voltage; the Vdc1, and Vdc2 of sources are applied to the load with switches I4, I5, and I9 for the positive side of the voltage. Then, the Vdc1 and Vdc2 of the sources are delivered to the load with I0, I1, and I8 for the negative side of the voltage. For creating the third step of alternating voltage; Vdc1, Vdc2, and Vdc3 of sources are delivered to the load with I0, I1, I2, and I8 for the negative side of the voltage. the Vdc1, Vdc2, and Vdc3 of sources are again applied to the load with switches I4, I5, I6, and I9 for creating the positive side of voltage at the third step. Finally, for creating the fourth step of alternating voltage; the Vdc1, Vdc2, Vdc3, and Vdc4 of sources are implemented to the load with switches I4, I5, I6, I7, and I9 for the positive side of voltage. Vdc1, Vdc2, Vdc3, and Vdc4 are operated with I0, I1, I2, and I8 for the creating negative side of the load voltage. The PWMs that provide the first step voltage are given in Figure 2.

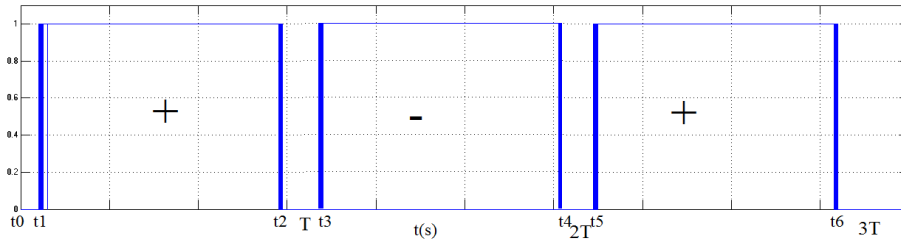


Figure2. The PWMs providing the first step voltage

For the positive side of the voltage to be generated, the PWM time( $D_n$ ) can be expressed as in equations 1 and 2:

$$D_n = t_2 - t_1 \tag{1}$$

For the negative side of the voltage to be generated, the PWM time ( $D_n$ ) can be expressed as in equations 2 and 4:

$$D_n = t_4 - t_3 \tag{2}$$

The gap between two PWMs ( $T_g$ ) can be given as in equation 5.

$$T_g = t_3 - t_2 \tag{3}$$

If the PWM is repeated with T periods as in Figure 3, the Fourier analysis can be done more effectively.

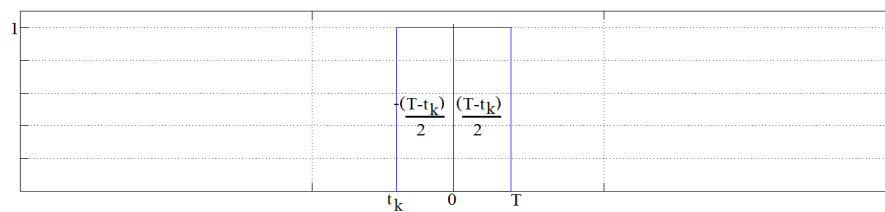


Figure3. The PWM repeated with T periods for Fourier analysis

$k \in Z^+ \rightarrow k = \{1,2,3 \dots \dots \infty\}$  and  $n \in Z^+ \rightarrow n = \{1,2,3 \dots \dots \infty\}$ , A is amplitude of PWM. Fourier analysis equations for PWM can be done as follows:

$$a_n = \frac{2}{T} \int_0^T A \cos\left(\frac{2\pi n t}{T}\right) dt \tag{4}$$

$$a_n = \frac{2}{T} \int_{\frac{-T+t_k}{2}}^{\frac{T-t_k}{2}} A \cos\left(\frac{2\pi n t}{T}\right) dt \tag{5}$$

$$a_n = \frac{2A}{T} \left[ \frac{T}{2\pi n} \sin \frac{2\pi n t}{T} \right] \Big|_{\frac{T-t_k}{2}}^{\frac{T+t_k}{2}} \quad (6)$$

$$a_n = \frac{2A}{n\pi} [\sin \pi n D_n] \quad (7)$$

### 3. SIMULATION STUDY AND RESULTS

The MATLAB Simulink model of the 9-level inverter is given in Figure 4. The speed of running the simulation is  $6 \times 10^{-6}$  sec. For the first step voltage of the circuit in Figure 4, the time between PWMs ( $T_g$ ) is determined as 0.0003s as in Figure 7. The voltage of harmonic distortion on the 0.1 ohms of load occurs as in Figure 5, while the current of harmonic distortion values is as in Figure 6.

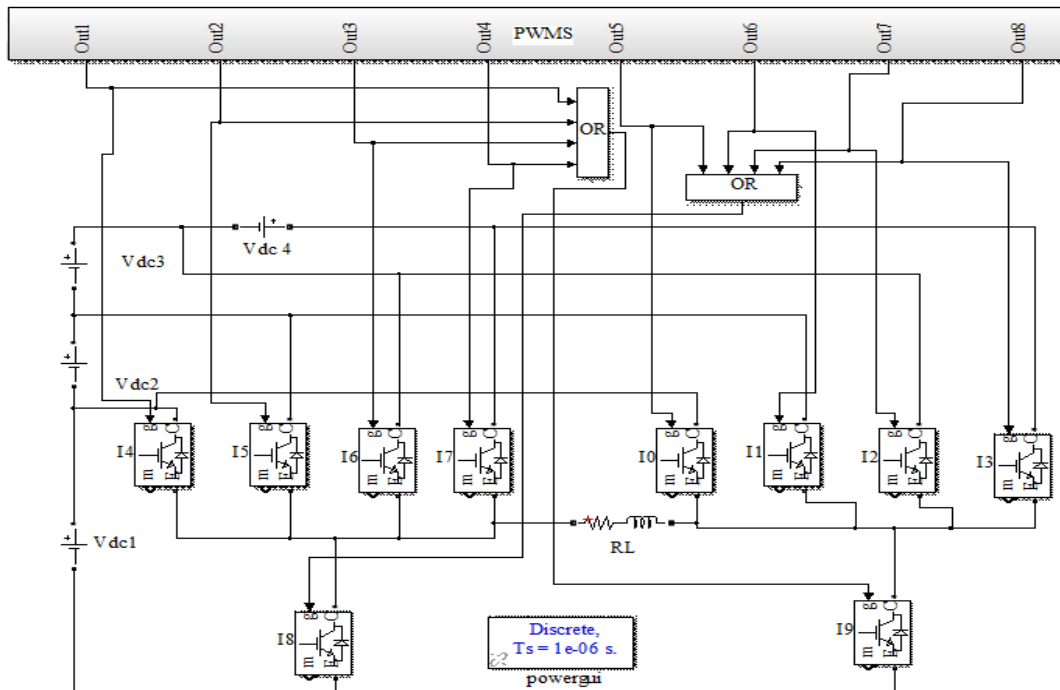


Figure4. MATLAB Simulink model of 9-level inverter

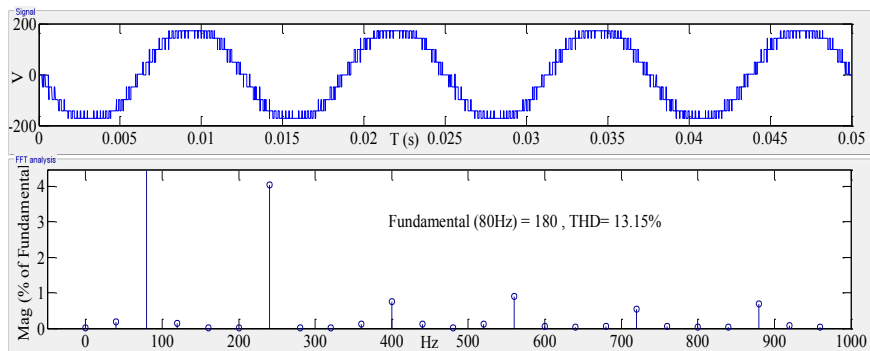


Figure5. Voltage and harmonic distortion on the 0.1 ohms of the load of the time between PWMs of 0.0002s

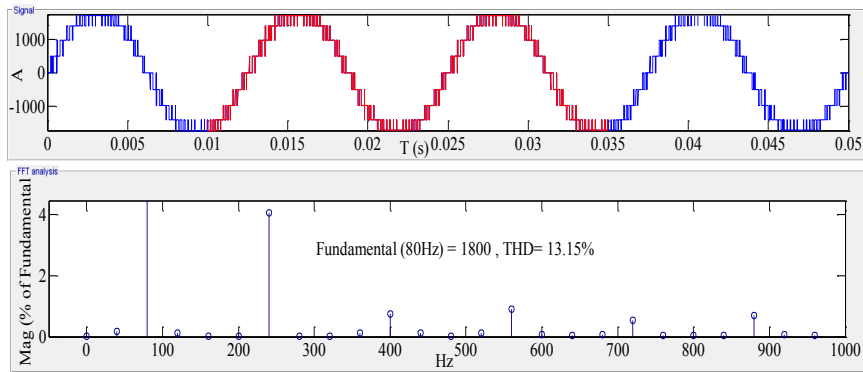


Figure 6. Current and harmonic distortion on the 0.1 ohms of the load of the time between PWMs of 0.0003s

80-volt of DC source on a 0.1-ohm of resistive load causes a 13.15% distortion. For a purely resistive load; distortion is more than 5% as a result. But, with an inverter without a level, the distortion has much higher values in a voltage conversion. Resistive (R) of 0.01 ohm and Inductive (L) of 0.002 H are connected in series for RL load; as in Figure 7, when the carrier triangle signal amplitude value is determined between 0.1V and 0.5V, the gap of the PWMs at the zero-crossing point becomes 0.003s as seen in figure 8. The load voltage, the load current, and the load current distortion are as in Figure 9 if the measurement is made again for  $T_g$  of 0.0003s.

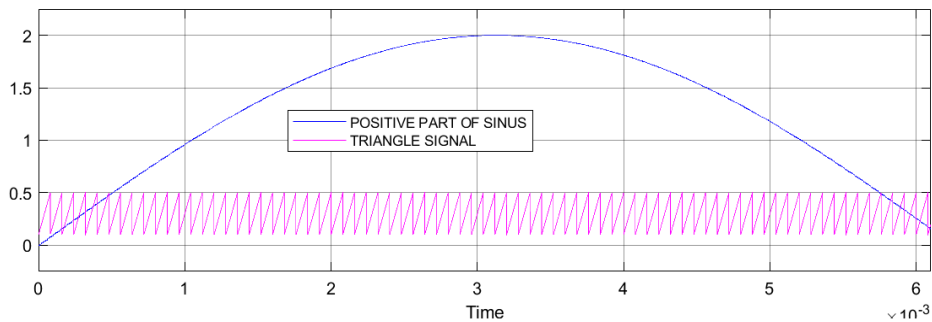


Figure 7. The carrier triangle signal amplitude value determined between 0.1V and 0.5V

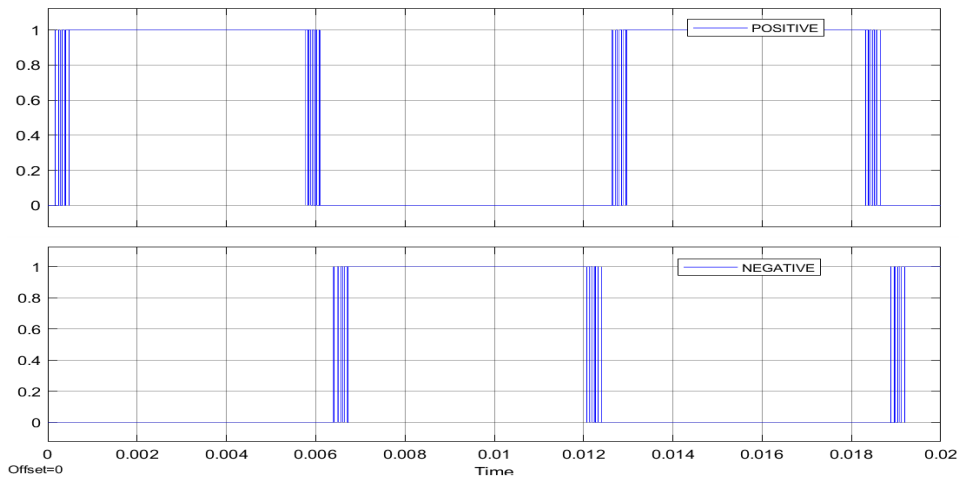


Figure 8. The time between PWMs ( $T_g$ ) for 0.0003s

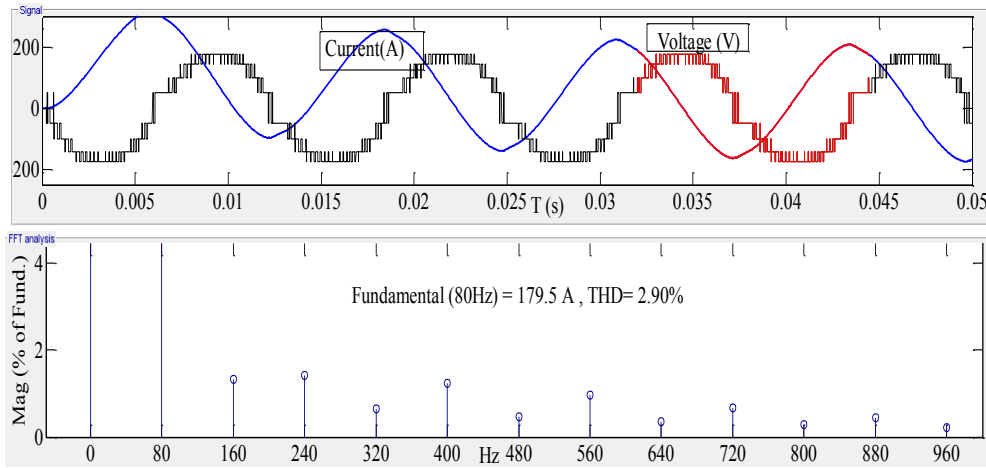


Figure9. Current and harmonic distortion on the RL of load at the time between PWMs of 0.0003s

When the load current reaches 179.5 A, the harmonic distortion is 2.9% for the 0.0003s value of  $T_g$ . This value is below 5%, which is the acceptable distortion value.

While the carrier triangle signal amplitude value is determined between 0.2V and 0.5V as in Figure 10, the gap of the PWMs at the zero-crossing point becomes 0.0004s as seen in Figure 11. When  $T_g$  becomes 0.0004s, the start of the working time of PWM is from 0.0065 s to 0.0066 s, as in Figure 11.

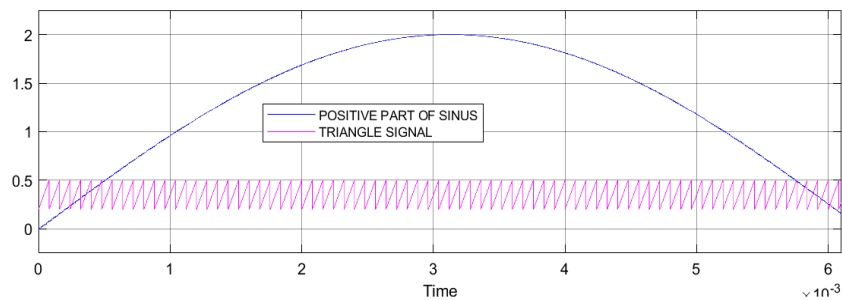


Figure 10. The carrier triangle signal amplitude value determined between 0.2V and 0.5V

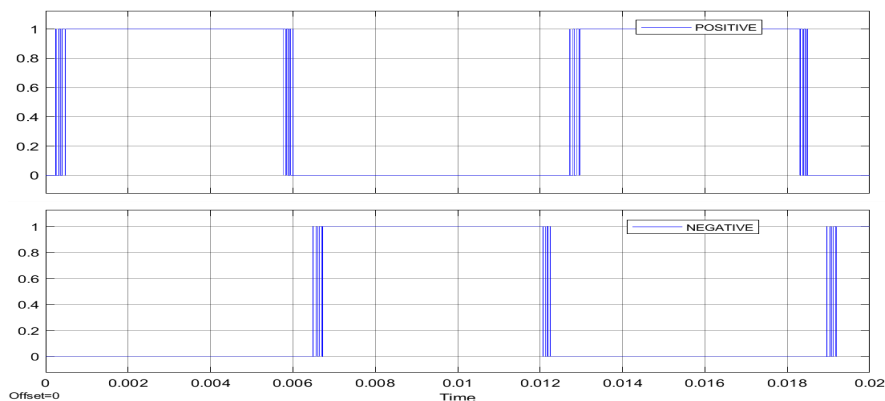


Figure 11. PWM for  $T_g$  of 0.0004s

A resistive (R) load of 0.01 ohm and an inductive (L) load of 0.002 H are connected in series for RL load; if the measurement is made again for  $T_g$  of 0.0004s; the load voltage, load current, and load current distortion value is as in figure 12.

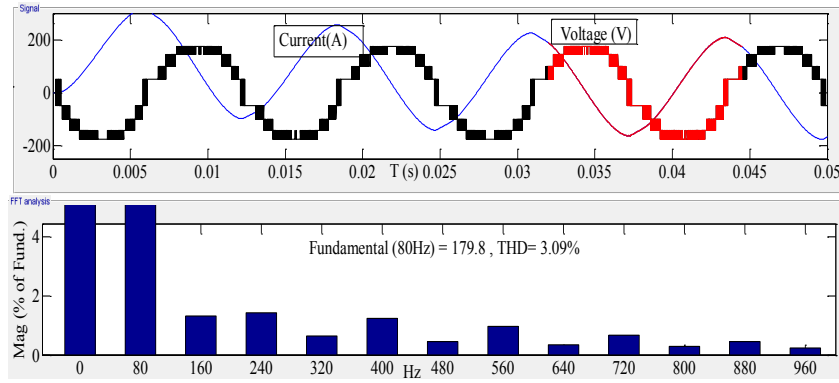


Figure 12. Current and harmonic distortion on the RL load at the time between PWMs of 0.0004s

While the alternating current on the load is 179.8 A, the total harmonic distortion (THD) of the current is 3.09%. Although the deterioration is within the value determined by international standards, there is an increase of 0.19% in the THD value.

The triangular signals between 0.3V and 0.5V in amplitude are compared with the sine signal in Figure 13.  $T_g$  becomes 0.0005s when the start of the working time of PWM is taken from 0.0066 s to 0.0067 s in Figure 14. Then, a resistive (R) load of 0.01 ohm and an inductive (L) load of 0.002 H are connected in series for RL load. if the measurement is made again for  $T_g$  of 0.0005; the load voltage, load current, and load current distortion value is as in Figure 15.

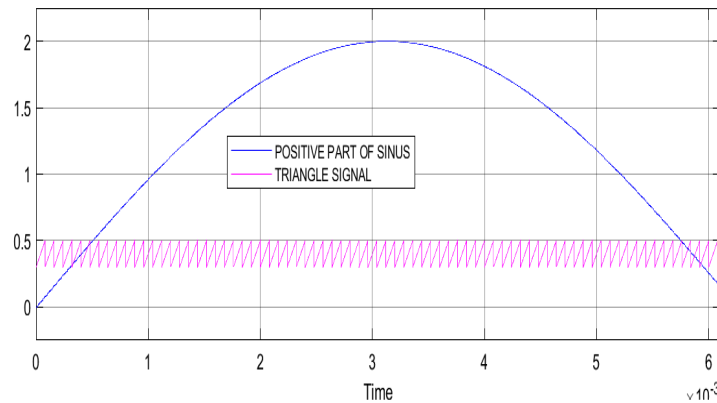


Figure13. The triangular signals between 0.3V and 0.5V in amplitude,

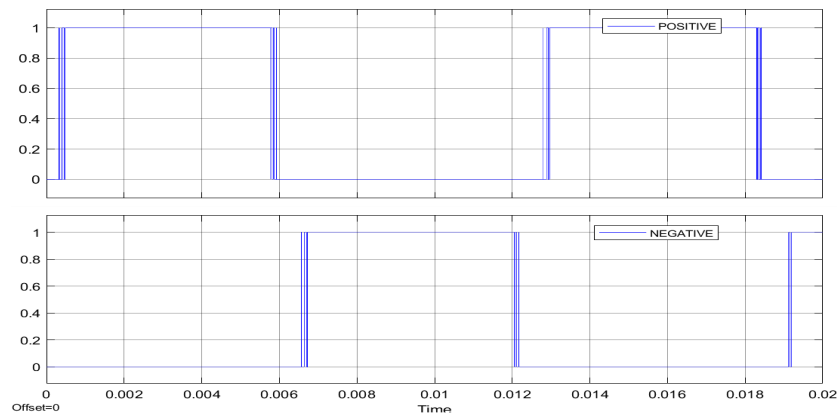


Figure14. PWM for  $T_g$  of 0.0005s

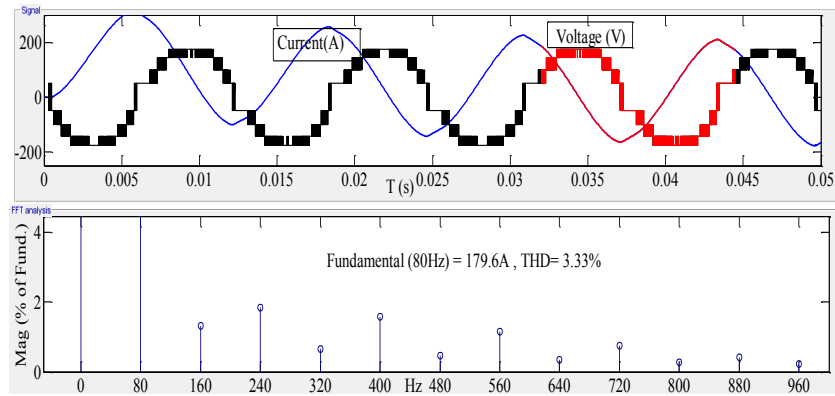


Figure 15. Current and harmonic distortion on the RL of load at the time between PWMs of 0.0005s

While the alternating current on the load is 179.6 A, the total harmonic distortion (THD) of the current is 3.33%. Although the deterioration is within the value determined by international standards, there is an increase of 0.22 % in the THD value.

The triangular signals between 0.4V and 0.5V in amplitude are a comparison with the sine signal in Figure 16.  $T_g$  is 0.0006s because the start of the working time of PWM is taken from 0.0067 s to 0.0068 s, as in Figure 17. A Resistive (R) load of 0.01 ohm and an inductive (L) load of 0.001 H are connected in series for RL load; if the measurement is made again for  $T_g$  of 0.0006s; the load voltage, load current, and load current distortion value is as in Figure 18.

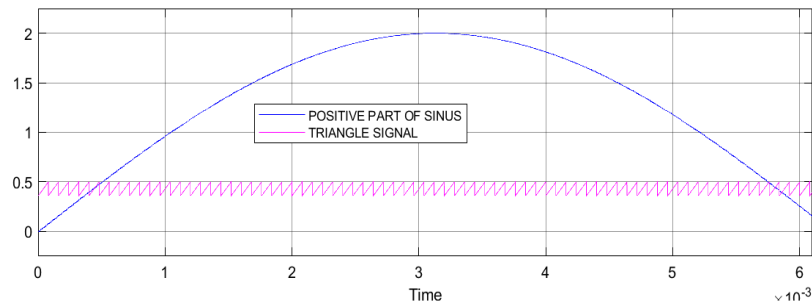


Figure16. The triangular signals between 0.4V and 0.5V in amplitude

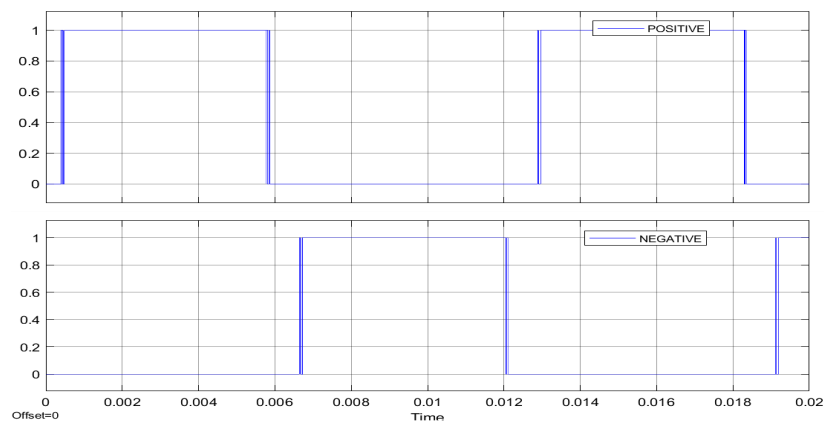


Figure17. PWM for  $T_g$  of 0.0006s



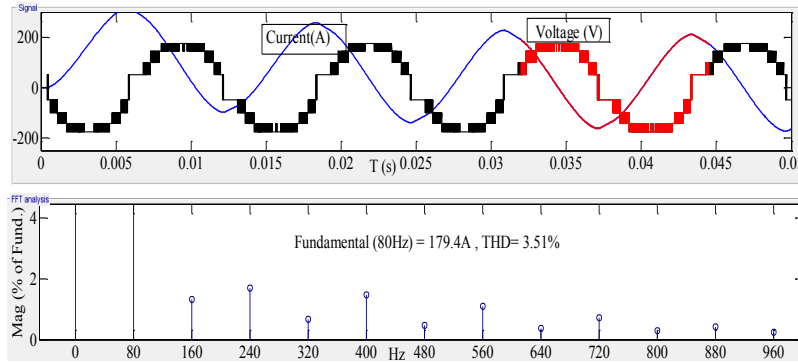


Figure 18. Current and harmonic distortion on the RL of load at the time between PWMs of 0.0006s

While the alternating current on the load is 179.4A, the total harmonic distortion (THD) of the current is 3.51%. Although the distortion is within the value determined by international standards, there is an increase of 0.18 % in the THD value.

The comparison of the carrier triangle signal with amplitude between 0V and 0.5V and the sinus signal is shown in Figure 19. The PWMs with a gap of 0.0001s, which will manage the zero-crossing point, are given in Figure 20 as a result of this comparison. PWM starting point is taken as 0.0063s in each  $T_g$  of calculation. So,  $T_g$  is 0.0001s when the start of the working time of PWM is taken from 0.0066 s to 0.0063 s. A resistive (R) load of 0.01 ohm and an inductive (L) load of 0.002 H are connected in series for RL load; if the measurement is made again for  $T_g$  of 0.0001s; the load voltage, load current, and load current distortion value is as in figure 21.

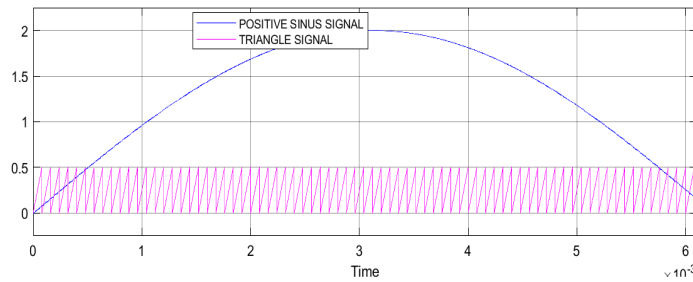


Figure19. The comparison of the carrier triangle signal with between 0V and 0.5V

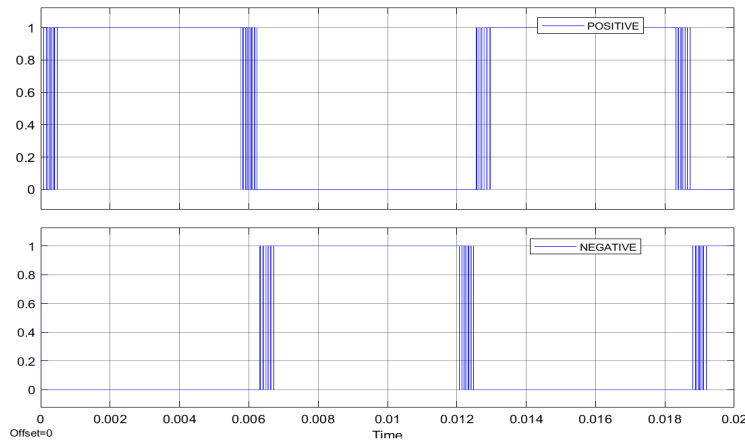


Figure20. PWM for  $T_g$  of 0.0001s

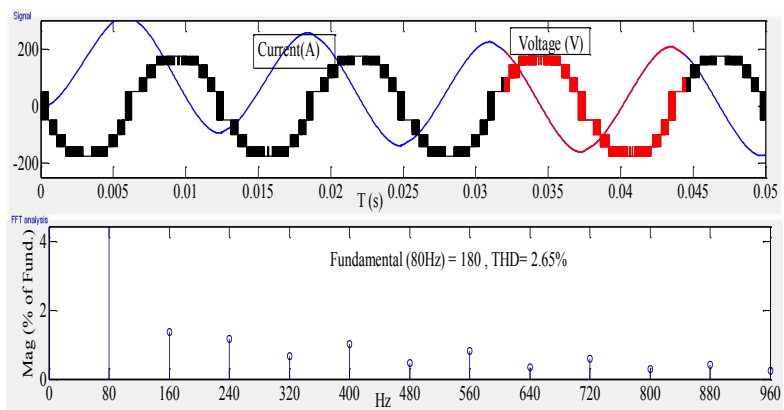


Figure 21. Current and harmonic distortion on the RL of load at the time between PWMs of 0.0001s

When  $T_g$  creates an opening of 0.0001s, the load current value becomes 180 A, and THD becomes 2.65%. According to the last experiment, there is a 0.86% improvement in the THD value. Distortion change according to  $T_g$  is given in Figure 22.

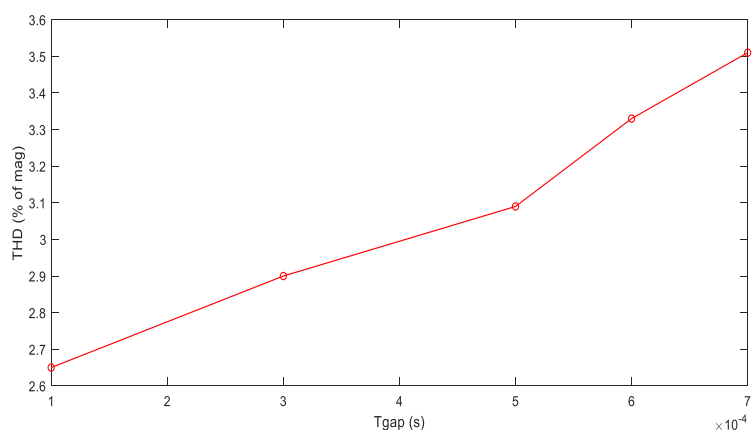


Figure22. Distortion changes according to  $T_g$

As seen in the graph in Figure 22, the THD value increases as the  $T_g$  ratio increases. The lowest distortion occurs when the  $T_g$  value decreases to 0.0001s. The results of the study show that regulating the operating times of PWMs in the transition from positive voltage to negative voltage side is as important as developing multilevel inverter circuits and modulation techniques in order to reduce harmonic distortion.

#### 4. CONCLUSIONS

The paper presents the effects of PWM operating times in the transition of first-level voltage at a load of the inverter. In this study, a nine-level inverter circuit has been operated with a sinus pulse width modulation technique. In order to examine the effect on the zero-point transitions of the alternating voltage formed, the duration of the PWMs forming the first step voltage is taken from 0.00063s to 0.00068s. When  $T_g$  creates an opening of 0.0001s, the load current value is 180.1A, and THD becomes 2.65%.  $T_g$  is 0.0006s if the start of the working time of PWM is taken from 0.0067 s to 0.0068 s. While the alternating current on the load is 179.4A, the total harmonic distortion (THD) of the current is 3.51%. The distortion is within the value determined by IEEE standards. The results of this study demonstrated that it is very important and essential to regulate the operating times of PWMs in the transition from the positive voltage to the negative voltage side after the multi-level inverter circuits and modulation techniques are studied to reduce the distortion.

## REFERENCES

- Abbas, A. S., El-Sehiemy, R. A., El-Ela, A., Ali, E. S., Mahmoud, K., Lehtonen, M., & Darwish, M. M. 2021.** Optimal Harmonic Mitigation in Distribution Systems with Inverter Based Distributed Generation. *Applied Sciences*, 11(2), 774.
- Barbie, E., Rabinovici, R., & Kuperman, A. 2021.** Analytical formulation and optimization of Weighted Total Harmonic Distortion in three-phase staircase modulated multilevel inverters. *Energy*, (215), 119137.
- Can, E. 2019.** The design and experimentation of the new cascaded DC-DC boost converter for renewable energy. *International Journal of Electronics*, 106(9), 1374-1393.
- Can, E. 2020a.** A new multi-level inverter with reverse connected dual dc to dc converter at simulation. *International Journal of Modelling and Simulation*, 1-13.
- Can, E. 2020b.** Energy transformation without using filter on high resistive load. *Engineering Review*, 39-47.
- Can, E. 2021.** The inverter with reverse connected double converter driving unbalanced loads. *International Journal of Modelling and Simulation*, 1-10.
- Can, E., & Sayan, H. H. 2017.** The increasing harmonic effects of SSPWM multilevel inverter controlling load currents investigated on modulation index. *Tehnički vjesnik*, 24(2), 397-404.
- Dhanamjayulu, C., Prasad, D., Padmanaban, S., Maroti, P. K., Holm-Nielsen, J. B., & Blaabjerg, F. 2021.** Design and implementation of seventeen level inverter with reduced components. *IEEE Access*, 9, 16746-16760.
- Gupta, A. 2022.** Power quality evaluation of photovoltaic grid interfaced cascaded H-bridge nine-level multilevel inverter systems using D-STATCOM and UPQC. *Energy*, (238), 121707.
- Hassan, A., Yang, X., & Chen, W. 2021.** A step-up D-type multilevel inverter topology with reduced components counts for renewable energy applications. *International Transactions on Electrical Energy Systems*, 31(9), e13004.
- Law, K., Ng, W., & Wong, W. 2017.** Flyback cascaded multilevel inverter based SHE-PWM control for STATCOM applications. *International Journal of Power Electronics and Drive Systems*, 8(1), 100-108.
- Lee, S. S., Chu, B., Idris, N. R. N., Goh, H. H., & Heng, Y. E. 2015.** Switched-battery boost-multilevel inverter with GA optimized SHEPWM for standalone application. *IEEE Transactions on Industrial Electronics*, 63(4), 2133-2142.
- Padmanaban, S., Dhanamjayulu, C., & Khan, B. 2021.** Artificial Neural Network and Newton Raphson (ANN-NR) Algorithm Based Selective Harmonic Elimination in Cascaded Multilevel Inverter for PV Applications. *IEEE Access*, 9, 75058-75070.
- Sarebanzadeh, M., Hosseinzadeh, M. A., Garcia, C., Babaei, E., Islam, S., & Rodriguez, J. 2021.** Reduced Switch Multilevel Inverter Topologies for Renewable Energy Sources. *IEEE Access*, (9), 120580-12059.

