Optimizing CNTFET design parameters using Taguchi method for high performance and low power applications

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ABSTRACT

The features of CNT (Nanotube Carbon) are fascinating to study due to their unique structural and electrical capabilities. The small structure of the CNT in Field-Effect Transistor technology can produce a smaller device with a better performance. In this work, the Taguchi method had been implemented to optimize the Carbon Nanotube Field-Effect Transistor (CNTFET). The Minitab 19 software had been used to carry out the Taguchi method analysis. Three design parameters (diameter of CNT, pitch and the number of CNT) with three different sizes each had been chosen to improve the CNTFET capabilities. L27 orthogonal array and signal-to-noise (SNR) was used to collect and analyze the data. The result from the Taguchi method was validated by using ANOVA. The analysis results displayed the best combination of the three design parameters that produce the optimum performance in terms of high power and low power application. The study showed that the most dominant design parameter that affects the CNTFET's current characteristics is the diameter of CNT with 59.93%, 96.15% and 99.14% towards on-current (Ion), off-current (Ioff) and current ratio (Ion/Ioff), respectively. By identifying the most dominant structure in CNTFET, the device can be further optimized. Eventually, the CNTFET devices in terms of high power and low power application can be enhanced.

Keywords: carbon nanotube; field-effect transistor; optimization; Taguchi method; inverter.

INTRODUCTION

Due to this rapid advancement of electronics manufacturing technologies, there have been numerous obstacles in developing electronic circuits. To reduce these limitations, several nanoelectronics devices was introduced to replace Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) technology, such as Carbon Nanotube Field-Effect Transistor (CNTFET). CNTFET used the Carbon Nanotube (CNT) as a channel material instead of bulk silicon like in MOSFET technology. CNT, founded by Ijiima in 1991, was made up of a rolled-up single layer of the graphene sheet, as in Fig. 1.

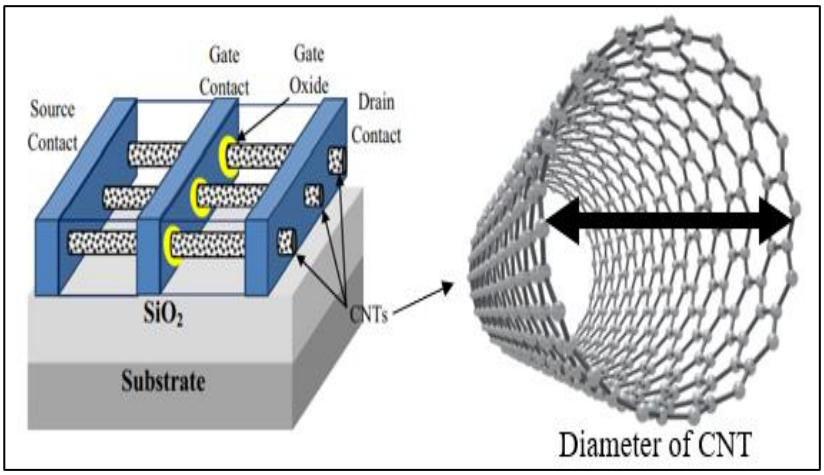

Figure 1. The structure of CNTFET (Vidu et al., 2014; Saiphani Kumar et al., 2018).

There are still many aspects that can be improved to have an optimum performance of CNTFET. One of the improvements in the CNTFET device can be made by changing its geometric architecture (Shimaa. I. Sayed et al., 2016; Shimaa. I. Sayed et al., 2017; Prakash et al., 2017). Changing the geometric structure of the CNTFET can affect the performance of the CNTFET.

In an attempt to achieve the best device performance, there is a need to have a method to optimize the geometric architecture. A study by Shimaa. I. Sayed et al. (2016) used a trial-and-error based search to optimize the design parameter of CNTFET. However, this technique is

time-consuming as many experimental trials were set to simulate the CNTFET model. Another study by Shimaa. I. Sayed et al. (2017) used an optimization technique called Genetic Algorithm Parameter. This Genetic Algorithm optimization manages to find the best Power-Delay product (PDP) of the CNTFET by varying the design parameter such as the diameter of CNT, number of CNT and CNT pitch. Even so, this technique is unable to identify which design parameter provides a significant effect on the performance of CNTFET. Another optimization technique used to optimize the CNTFET design parameters is Particle Swarm Optimization (PSO) (Reena Monica et al., 2016) and Whale Optimization Algorithm (Prakash, Sundaram, and Bennet 2017). These two optimization methods are able to find the optimal design parameter for the CNTFET. However, this technique also cannot provide any information about the influence of the design parameter on the performance of CNTFET.

Hence, an optimization technique of the Taguchi Method was applied to find the best combination of CNTFET design parameters that provide the optimum performance in terms of Ion, Ioff and Ion/Ioff. In addition, this method can also determine the contribution factor of each of the CNTFET's design parameters towards the response variables (Ion, Ioff and Ion/Ioff). Therefore, by identifying the most significant contributing factor, the optimization process can focus on the targeted design parameter to get better performance.

METHODOLOGY

HSPICE tools were used to simulate the Stanford University Carbon Nanotube Field Effect Transistors (CNTFET) model as in Fig. 2 (Albert Lin et al., 2009). This model can be simulated with the lowest channel length of 10 nm. The channel length of the CNTFET was fixed to 32.0 nm with the width of the metal gate of 6.4 nm. The oxide thickness that separates the gate from the channel was set to 4.0 nm. The dielectric constant was specified to K=16.

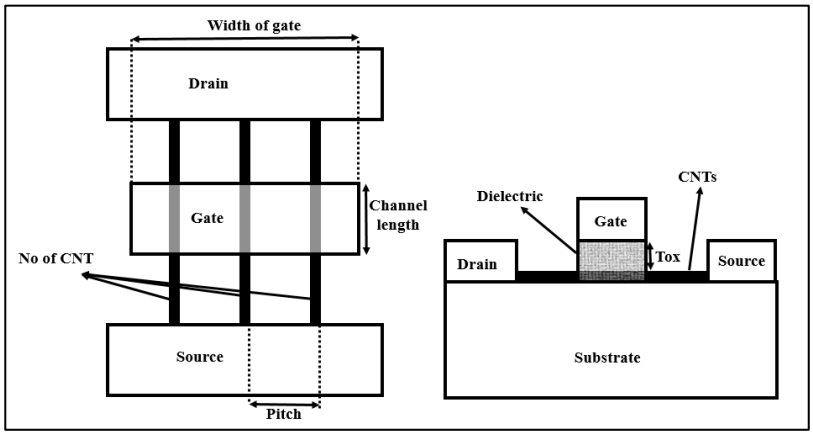

Figure 2. Structure of CNTFET and related parameters.

Three parameters were chosen to optimize the performance of CNTFET, which were the diameter of CNT, pitch and the number of CNT in the transistor. The three design parameters were the common parameters which the previous study used to optimize the CNTFET performance. The manipulated ranged value of CNT diameter was selected according to the previous fabricated CNTFET with 1.2 nm (Bishop et al., 2020). The size of the pitch was varied based on the previous simulated model by Moaiyeri et al. (2017) and Almudever et al. (2015) with 3.0 nm and 4.0 nm, respectively. Finally, the number of CNT in the transistor was varied according to the previous model (Chen et al. 2007). All the scope of the model has been summarized in Table 1.

Table 1. Device structure parameters and values.

Parameters	**Fixed Values**	**Manipulated Ranged**	**References**
Diameter of CNT, nm	-	1.0-1.4	(Albert Lin et al., 2009; Bishop et al. 2020)
Pitch, nm	-	3.0-5.0	(Albert Lin et al., 2009; Moaiyeri et al., 2017; Almudever et al., 2015)
Number of CNT	-	1-5	(Albert Lin et al., 2009; Chen et al. 2007)
Channel length, nm	32.0	-	(Albert Lin et al., 2009)
Oxide thickness, nm	4.0	-	(Albert Lin et al., 2009)
Dielectric Constant, K	16	-	(Albert Lin et al., 2009)
Width of the metal gate, nm	6.4	-	(Albert Lin et al., 2009)

Fig. 3 shows the procedure for the application of the Taguchi method to optimize the CNTFET

design parameters and subsequently demonstrates the influence on inverter circuits for high performance and low power applications.

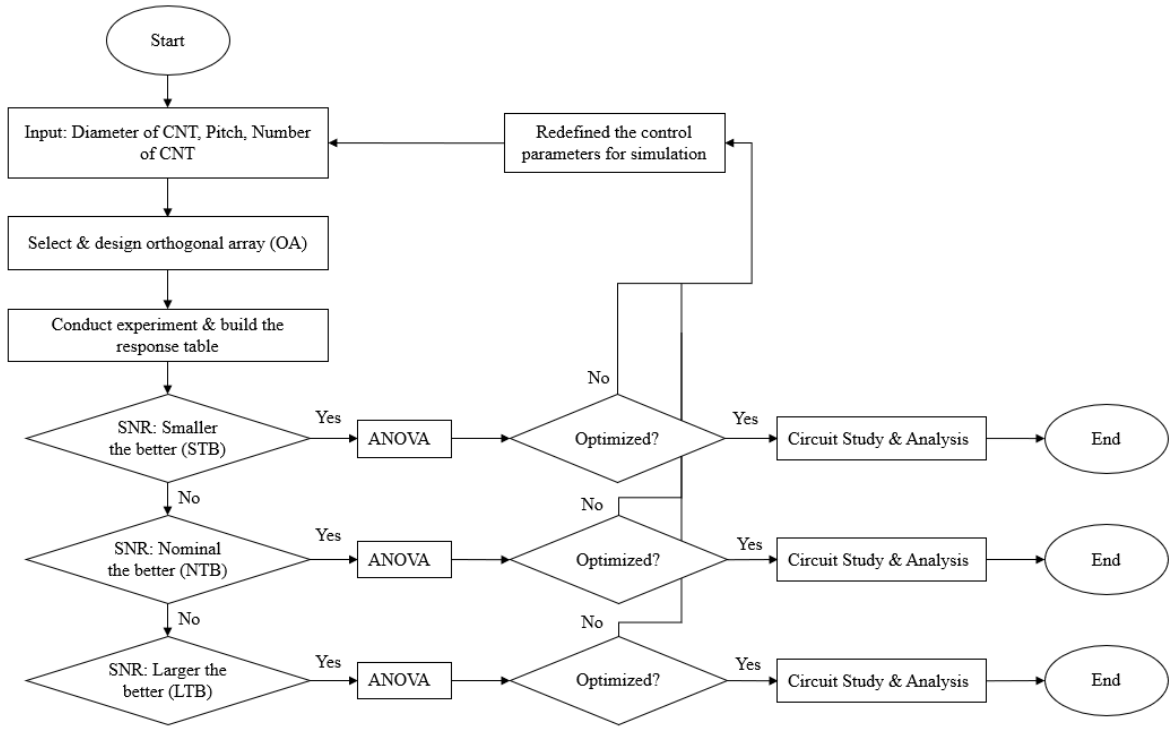

Figure 3. Block diagram for the Taguchi method.

Three parameters that influence the CNTFET performance were chosen for this simulation. The three parameters were the CNT diameter, CNT pitch and the number of CNT in a transistor assigned as A, B and C, respectively, as in Table 2. Each of the parameters is set into three-level, which are level 0, level 1 and level 2. Level 0 defines the smallest value of parameters, while level 2 is the largest value of parameters.

Table 2. Design of experiment for the Taguchi method.

Symbol	Parameters	Level		
		0	**1**	**2**
A	Diameter of CNT, nm	1.0	1.2	1.4
B	CNT pitch, nm	3.0	4.0	5.0
C	Number of CNT	1	3	5

Taguchi Method

The Taguchi method utilized the signal-to-noise ratio (SNR) to determine the quality characteristic of CNTFET (Ashwni et al., 2021). Three types of SNR need to be selected

according to the characteristic of the response. The type of SNR is as in Equation (1-3). If the response variable needs to be maximized, the LTB type of SNR needs to be chosen. Meanwhile, the STB type of SNR will be chosen if the response variable needs to be minimized. For NTB, this type of SNR is used when the target value for the response variable needs to be specified (M. Yusoff, 2008; L. Salavaravu et al., 2021). The goal for NTB is to have minimal variability around the target.

Larger the better (LTB): $$\frac{S}{N} = -10 \log \frac{1}{n}\left(\sum \frac{1}{y^2}\right) \quad (1)$$

Smaller the better (STB): $$\frac{S}{N} = -10 \log \frac{1}{n}\left(\sum y^2\right) \quad (2)$$

Nominal the better (NTB): $$\frac{S}{N} = 10 \log \frac{1}{n}\left(\frac{\hat{y}^2}{s_y^2}\right) \quad (3)$$

RESULTS AND DISCUSSION

The Taguchi method used an L27 orthogonal array to simulate all three possible parameters combinations in this work. The orthogonal array used for the simulation includes the simulated value of Ion, Ioff and the current ratio of the CNTFET. Only 27 experimental trials were required for the L27 orthogonal array.

Signal-to-Noise Ratio Analysis

The SNR was calculated from the orthogonal array for each response variable (Ion, Ioff & Ion/Ioff) according to its SNR type. The goal for the SNR analysis is to select the highest possible SNR among the response variables. The design parameter with the highest value of SNR indicates a higher signal than the noise factor and provide a better performance towards CNTFET.

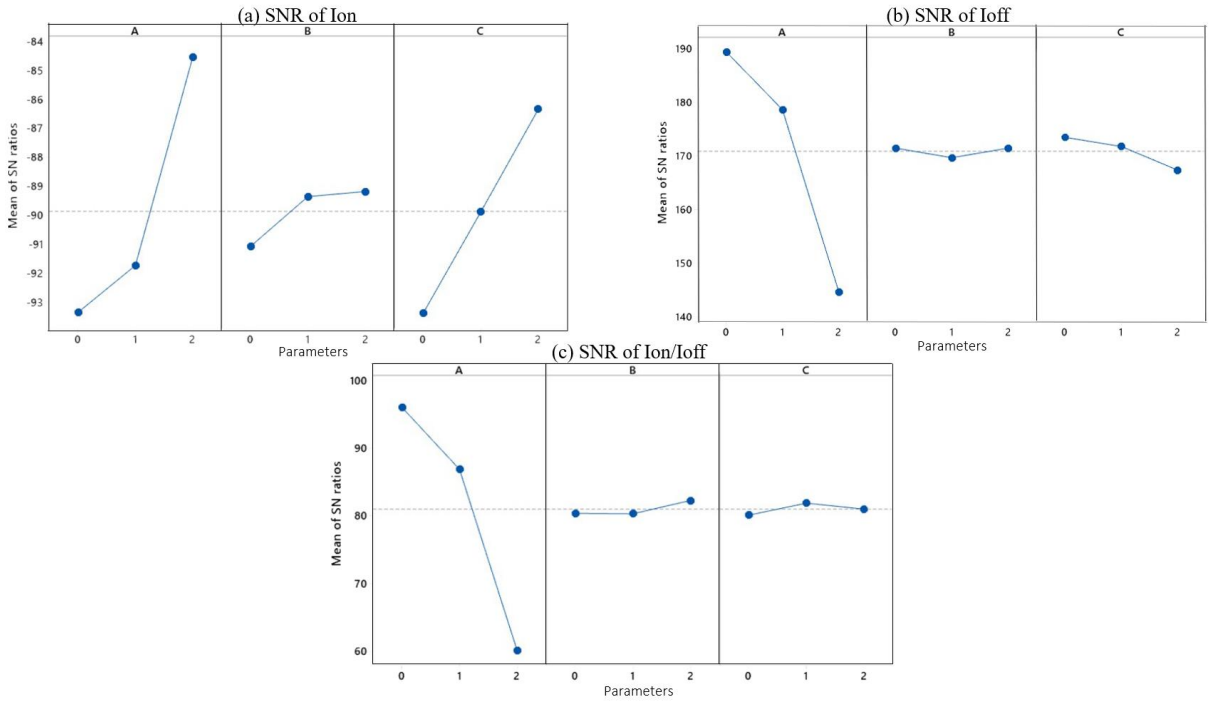

Figure 4. The-result-for SNR for (a) Ion, (b) Ioff, and (c) current ratio.

For the Ion, the value needs to be as high as possible in order to produce a CNTFET with better performance. The LTB type of SNR needs to be applied for this response variable using Equation (1). The result for the SNR ratio was analyzed and plotted as displayed in Fig. 4 (a). The combination factors that produced that the highest Ion was A2B2C2. This was the best combination to produce the optimum Ion for CNTFET, representing the 1.4 nm of CNT diameter, 5.0 nm of CNT pitch and 5 number of tubes in the CNTFET, respectively. The SNR graph can determine the most significant process parameters towards Ion. This can be calculated by observing the slope of each process parameter which is the difference between the value of SNR at the highest point and the value SNR at the lowest point. In the case of the Ion response variable, the most significant contribution parameter is the diameter of CNT followed by the number of CNT and CNT pitches.

As for the Ioff, the value target needs to be the lowest as possible in order to produce a CNTFET with better performance. Therefore, the STB type of SNR needs to be applied using Equation (2) for this response variable. The result for the SNR ratio was analyzed and plotted as displayed

in Fig. 4 (b). The technique to determine the best SNR for STB was the same as LTB which the larger SNR between the parameter is chosen. The combination factors that produced the lowest Ioff were A0B0C0, representing the 1.0 nm of CNT diameter, 3.0 nm of CNT pitch, and 1 number of tubes in the CNTFET, respectively. The highest value difference between the SNR at the highest point and the SNR at the lowest point of the slope is the diameter of CNT, followed by the number of CNT and CNT pitches. This indicates that the Ioff of the CNTFET was influenced the most by the diameter of CNT.

In the case of Ion/Ioff ratio performance, a similar method is applied to determine the best parameter combination for CNTFET. The Ion/Ioff ratio needs to be high as possible to provide better performance. Hence, the LTB of SNR is chosen. The combination factors that produced the optimum Ion/Ioff ratio performance were A0B2C1 as displayed in Fig. 4 (c), representing the 1.0 nm of CNT diameter, 5.0 nm of CNT pitch, and 3 number of tubes in the CNTFET, respectively. The most significant contribution was the diameter of CNT followed by CNT pitch and the number of CNT in the CNTFET.

The best combination of each response variable can be determined by applying the Taguchi method. However, the relative significance of the process parameter towards each response variable needs to be validated. This validating process continued in the next section using analysis of variance (ANOVA).

Analysis of Variance (ANOVA)

The analysis of variance (ANOVA) was conducted to determine which the most significant process parameter towards response variables. For this study, the F-ratio was 95% of confidence level. Table 3 shows the results of ANOVA for Ion. Based on the results, factor A (diameter of CNT) and factor C (number of CNT) were identified as the most dominant process parameters that influenced the Ion due to their highest factor effect on SNR, 59.93% and 33.81%, respectively. On the other hand, factor B (CNT pitch) was shown to be less significant

with a 2.99% contribution. This result corresponds to the previous SNR analysis for Ion in 3.1.

Table 3. Analysis of Variance for Ion.

Source	DF	Seq SS	Contribution	Adj SS	Adj MS	F-Value	P-Value
A	2	5.2487	59.93%	5.2487	2.62435	183.26	0
B	2	0.2615	2.99%	0.2615	0.13076	9.13	0.002
C	2	2.9611	33.81%	2.9611	1.48057	103.39	0
Error	20	0.2864	3.27%	0.2864	0.01432		
Total	26	8.7578	100.00%				

Table 4 shows the results of ANOVA for Ioff. The results show that the diameter of CNT greatly affects the Ioff performance by contributing a 96.15% factor effect on SNR. This contribution percentage was followed by factor C (number of CNT) and factor B (CNT pitch) with factor effect on SNR of 1.78 % and 0.19%, respectively. This ANOVA result fits with the previous SNR analysis for Ioff in 3.1. In order to achieve the lowest value of Ioff, the size of the CNT diameter need to be small.

Table 4. Analysis of Variance for Ioff.

Source	DF	Seq SS	Contribution	Adj SS	Adj MS	F-Value	P-Value
A	2	130.209	96.15%	130.209	65.1047	510.97	0
B	2	0.255	0.19%	0.255	0.1276	1	0.385
C	2	2.413	1.78%	2.413	1.2064	9.47	0.001
Error	20	2.548	1.88%	2.548	0.1274		
Total	26	135.426	100.00%				

Table 5 shows the result of ANOVA for Ion/Ioff. Similar to the results of ANOVA for Ioff, the diameter of CNT contributes the most to the Ion/Ioff ratio performance with a 99.14% factor effect on SNR. On the other hand, the CNT pitch and the CNT number are considered less significant with 0.24% and 0.11% contributions. This result corresponds to the previous SNR analysis for Ion/Ioff in 3.1. Therefore, based on the three response variables, it can be deduced that the CNT diameter greatly affects the CNTFET performance. Therefore, in order to optimize the CNTFET design parameter, the diameter of CNT is essential to be one of the variables.

Table 5. Analysis of Variance for Ion/Ioff.

Source	DF	Seq SS	Contribution	Adj SS	Adj MS	F-Value	P-Value
A	2	0.030708	99.14%	0.030708	0.015354	1949.39	0
B	2	0.000075	0.24%	0.000075	0.000038	4.78	0.02
C	2	0.000034	0.11%	0.000034	0.000017	2.13	0.145
Error	20	0.000158	0.51%	0.000158	0.000008		
Total	26	0.030974	100.00%				

Electrical Characterization of CNTFET

In the experiment, two data analysis techniques were used to optimize and validate the performance of CNTFET, which were the Taguchi method and ANOVA. Both techniques produce the same result on the parameters that affect most on the on-current, off-current and current ratio. Moreover, by using the Taguchi method, a preferable value for the response variable of the CNTFET can be achieved according to the type of SNR.

For the on-current performance, this response variable used LTB type of SNR to achieve a higher value when the design parameters of CNTFET had been optimized. Based on the result in Fig. 5, the on-current of the optimized CNTFET was enhanced. From Table 6, the on-current increase to a higher value from 57.9uA to 110uA. A higher on-current produced a better high-performance device. The Ion of the optimized CNTFET is also higher compared to the previous model that had been published, but the value is still far from ITRS 2022, which is 912 uA (Moaiyeri et al., 2017**;** IEEE 2020).

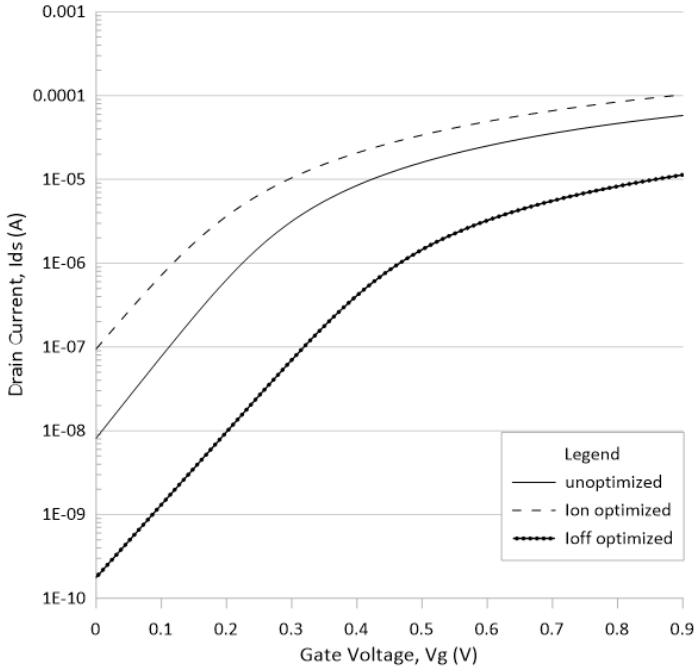

Figure 5. IV characteristics to compare between the unoptimized CNTFET and optimized CNTFET.

Table 6. Comparison between the unoptimized CNTFET and optimized CNTFET according to each response variable.

	Unoptimized CNTFET	**Optimized CNTFET (Ion)**	**Optimized CNTFET (Ioff)**	**Optimized CNTFET (Ion/Ioff)**	**32nm** (Moaiyeri et al., 2017)	**ITRS 2022-High Performance** (IEEE 2020)
Ion (uA)	57.9	110.00			97	912
Ioff (uA)	0.00816		0.000178		0.006	0.01
Ion/Ioff	7100			87982.03	16166.7	91200.0

As for off-current performance, this response variable used STB type of SNR to achieve a lower value when the design parameters of CNTFET had been optimized. Based on the result in Fig. 5, the off-current of the optimized CNTFET was enhanced. As a result, the off-current decreased to a lower value from 0.00816uA to 0.000178uA, as in Table 6. The Ioff value of the optimized CNTFET is also less than the previous model (Moaiyeri et al., 2017). An Ioff can produce a better low power device. For the current ratio, a higher ratio value is preferable in order to produce a faster switching device. This response variable used the same type of SNR

as on-current, which is the LTB, in order to achieve a higher ratio value. Based on the result, the current ratio of the optimized CNTFET had an increment compared to the unoptimized CNTFET design parameters. From Table 6, the current ratio increases to a higher value from 7100 to 87982.029. The current ratio, which was optimized by using the Taguchi method, surpassed the previous CNTFET model stated in Table 6. However, the current ratio of the optimized CNTFET was only 3.6% less compared to the current ratio set by ITRS 2022 (IEEE 2020). Using the Taguchi method as an optimization process, the CNTFET can be designed to achieve better performance.

Application of the CNTFET in High Performance and Low Power Applications

For high-performance applications, the CNTFET with the optimized Ion was chosen to be applied in the inverter circuit. It was essential to keep Ion at the highest value a higher rate of switching activity of the CNTFET inverter (Ali Usmani and Hasan, 2010; Rongtian Zhang et al., 2001). By choosing the CNTFET with high Ion, the power consumption of the CNTFET inverter also increases, as in Table 7.

Table 7. CNTFET circuit study analysis for high performance and low power application.

<table>
<tr><th rowspan="2"></th><th colspan="2">Delay (ps)</th><th colspan="2">Average Power (uW)</th></tr>
<tr><th>Unoptimized CNTFET</th><th>Optimized CNTFET</th><th>Unoptimized CNTFET</th><th>Optimized CNTFET</th></tr>
<tr><td>High Performance Application</td><td rowspan="2">2.8179</td><td>2.4484
(13% delay reduction)</td><td rowspan="2">1.1840</td><td>1.4961</td></tr>
<tr><td>Low Power Application</td><td>6.2416</td><td>1.0074
(15% average power reduction)</td></tr>
</table>

This is the drawback encountered by the CNTFET inverter for a high-performance application. For the low power device application, the CNTFET with the optimized Ioff was chosen to be applied in the inverter circuit. Since the low power application is usually used in a portable electronic device, the power consumption needs to be at the lowest as possible. Hence, it is

important to keep Ioff small to minimize the power that a circuit consumes when it is in standby mode (Hu, 2009). For this experiment, the power consumption of the optimized CNTFET inverter was reduced from 1.1840uW to 1.0074uW. However, by reducing the average power consumption, the delay of the optimized CNTFET inverter increased as in Table 7.

CONCLUSION

This paper presented an optimized design of CNTFET in terms of on-current, off-current and current ratio performance using the Taguchi method and ANOVA. The performance analysis appears to be highly dependent on the device geometry design, especially the diameter of CNT by more than 50% based on the ANOVA result for the three response variables. The Ion resulted in 1.4 nm of CNT diameter, 5.0 nm of CNT pitch, and 5 tubes in the CNTFET was the optimum performance for current trade-offs. Considering higher Ion provide a shorter delay, it was best to apply it to a high-performance device. As for the Ioff variable, the 1.0 nm of CNT diameter, 3.0 nm of CNT pitch and 1 number of tubes in the CNTFET were the best combination to provide better Ioff performance. A lower Ioff of the transistor was best to be applied into a low power device since it consumes less power. Next, the 1.0 nm of CNT diameter, 5.0 nm of CNT pitch and 3 number of tubes in the CNTFET provide better performance for current trade-offs for current ratio variables.. It can be concluded that the Taguchi method optimization plays an important role in designing for the next technology node in order to achieve continuous transistor scaling development.

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