Novel VDBA based universal filter topologies with minimum passive components

Musa Ali Albrni*,**, Mohammad Faseehuddin*,***, Jahariah Sampe* and Sawal Hamid Md Ali****

*Institute of Microengineering and Nanoelectronics (IMEN), University Kebangsaan Malaysia (UKM), Selangor, Malaysia
**Department of Electrical and Electronics Technology, The Higher Institute for Engineering Technology, Zliten – Libya
***Department of Electronics & Telecommunication, Symbiosis Institute of Technology (SIT), Symbiosis International (Deemed University), Lavale, Pune, Maharashtra 412115, India
****Department of Electrical, Electronic and Systems Engineering, University Kebangsaan Malaysia (UKM), Selangor, Malaysia
*Correspondent Author: jahariah@ukm.edu.my

ABSTARCT

In this research, voltage differencing buffered amplifier (VDBA) is utilized in designing three novel multi-input single output (MISO) topologies of universal filters. The designed filters employ minimum number of passive components and did not require any passive component matching condition. Two of the designed filters can work in dual mode of operation simultaneously. The designed filters have inbuilt tunability property. The nonideal gain analysis and sensitivity analysis of the filters are also carried out to study the effect of process variations and process spread on the filter responses. The complete layout of the VDBA is designed using 0.18μm Silterra Malaysia process design kit (PDK) in Cadence design software. The parasitic extraction is done using Mentor graphics Calibre tool. The postlayout simulations bear close resemblance with the theoretical predictions.

Keywords: Current conveyor; Current mode; Filters; Voltage mode; Voltage differencing buffered amplifier.

I. INTRODUCTION

Analog filters are an integral part of almost every electronic system, and so their synthesis and development remain an ever-evolving field. The filters find a wide array of applications in phase locked loop, FM stereo demodulator, telecommunication systems, speech processing, radar, data acquisition systems, instrumentation systems, etc. (Mohan 2012; Raut and Swamy 2010; Senani et al. 2014). Portable and network connected medical devices for real time monitoring and diagnosis of diseases will be vital in detecting diseases for future medical observation system. To develop such a system, low power and low noise analog circuits, such as amplifiers and filters, are required for physiological signal acquisition and signal processing (Cheng and Li 2015). The filters are also vital parts in biomedical data acquisition systems like sensors for artificial kidney for blood flow and filtration rate detection (Selvarajan et al. 2018; Yunus et al. 2017).

The filters based on active elements are the most attractive in terms of area efficiency, low voltage low power operation, and applicability. Active filters can exhibit high/low impedance levels at the input and the output. They can be designed for any gain easily. The filter circuit using active elements is generally much simpler compared to passive filters especially in higher-order filter implementations. A number of analog building blocks (ABBs) are employed in designing active filters, the most attractive ABBs are current conveyor (CCII) (Garradhi et al. 2018), differential voltage current conveyor (DVCC) (Horng and Jhao 2013), extra x current conveyor transconductance amplifier (EXCCTA) (Faseehuddin et al. 2018), Current backward transconductance amplifier (CBTA) (Sagbas et al. 2010), differential difference current conveyor (DDCC) (Abaci and Yuce et al. 2019), and current differencing transconductance amplifier

(CDTA) (Biolek 2003). The VDBA is another popular ABB (Yeşil et al. 2014) that is simple in design and shown to be versatile in realizing numerous applications. Several variants of the VDBA are also proposed in the literature like the voltage differencing inverting buffer amplifier (VDIBA) (Herencsar et al. 2013), fully balanced voltage differencing buffer amplifier (FB-VDBA) (Biolkova et al. 2009), etc. Given the flexibility of the VDBA, it has not been fully explored in designing filter applications. In this research, the VDBA is utilized in designing three novel filter structures.

The comparison of the filters can be done based on the following numerous criteria, which are important design parameters for comparison: (i) the number of ABBs employed; (ii) the number of passive elements used; (iii) the requirement of passive components matching condition; (iv) the low output impedance in case of VM and TIM filters/ high output impedance in case of CM and TAM filters; (v) inbuilt tunability; (vi) the use of negative or double input voltage for realizing filter responses; (vii) independent control of quality factor and pole frequency; (viii) the number of modes, in which they can work without any alteration in topology. The comparison of some exemplary MISO filter designs from literature with the proposed filters is given in Table 1.

Table 1. Comparative Study of the MISO Filters.

Reference	(i)	(ii)	(iii)	(iv)	(v)	(vi)	(vii)	(viii)
(Sagbas et al. 2010)	1	4	No	No	Yes	Yes	Yes	VM
(Herencsar et al. 2010)	1	4	No	Yes	Yes	No	No	VM
(Pandey and Paul 2011)	1	3	No	No	Yes	No	No	VM
(Myderrizi et al. 2011)	1	6	No	No	No	Yes	Yes	VM
(Tangsrirat and Channumsin 2011)	1	4	Yes	No	No	Yes	No	VM
(Horng and Jhao 2013)	1	4	Yes	No	No	No	No	VM
(Ninsraku et al.2014)	2	2	No	Yes	Yes	Yes	Yes	VM
(Lee 2017)	3	7	No	No	No	No	Yes	VM
(Ranjan 2018)	1	4	No	No	No	Yes	No	VM
(Yuce and Tez 2018)	2	5	Yes	Yes	No	Yes	Yes	VM
(Uttaphut 2018)	1	3	No	Yes	Yes	Yes	No	VM
(Singh and Nagaria 2020)	1	3	Yes	Yes	Yes	Yes	No	CM
(Kumar et al. 2019)	1	2	Yes	No	Yes	Yes	Yes	VM
(Basak 2019)	1	5	Yes	No	Yes	Yes	Yes	VM
Authors Work Figure 4	3	2	No	Yes	Yes	No	Yes	VM, TAM
Authors Work Figure 5	3	3	No	Yes	Yes	No	No	CM, TIM
Authors Work Figure 6	1	3	No	Yes	Yes	Yes (for AP only)	No	VM

It can be deduced from the comparison that the proposed designs hold advantages over the most other designs.

In this research, three novel topologies of VDBA based universal filters are developed. None of the proposed filters require any passive component matching conditions for response realization. Moreover, two of the proposed filters can work in dual mode simultaneously. The complete layout of the VDBA is designed using 0.18μm Silterra Malaysia PDK in Cadence design software. The postlayout results are given for all the designs.

II. Voltage Differencing Buffered Amplifier (VDBA)

The VDBA is a popular ABB that is simple in design and is shown to be versatile in realizing numerous applications. The VDBA consists of an operational transconductance amplifier (OTA) as the input stage and voltage buffer as the output stage. The V-I relations of the VDBA are summarized in Equation 1 and the block diagram is shown in Figure 1.
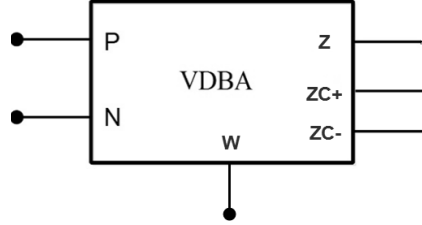

Figure 1. Block Diagram of VDBA.

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ I_{ZC+} \\ I_{ZC-} \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_m & -g_m & 0 \\ g_m & -g_m & 0 \\ -g_m & g_m & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \tag{1}$$

The CMOS implementation of VDBA is shown in Figure 2. It is a six terminal device. It is also worth mentioning that the number of Z terminals can be increased by just adding two additional CMOS transistors without affecting the functionality of the ABBs. The transistors (M1-M14) form the OTA which is the first stage of the VDBA. The output current of the OTA depends on the voltage difference between voltage at terminals *P* and *N*. Assuming saturation region operation for all transistors and equal W/L ratio for transistors M1 and M2 the output current $I_Z = I_{ZC+} = -I_{ZC-}$ of the OTA is given by Equation 2.

$$I_Z = I_{ZC+} = -I_{ZC-} = g_m(V_P - V_N) = \left(\sqrt{2I_{Bias}k}\right)(V_P - V_N) \tag{2}$$

Where, the transconductance parameter $K_i = \mu C_{ox} \frac{W}{2L}$ (i=1, 2), W is the effective channel width, L is the effective length of the channel, C_{ox} is the gate oxide capacitance per unit area and μ is the carrier mobility.

The second stage consists of a voltage follower designed using transistors (M15-M21). The nodes Z, ZC+, ZC- are high impedance nodes, and the W node is the low impedance voltage output node. The negative feedback from M20 and M21 reduces the resistance of the W node making it low impedance.
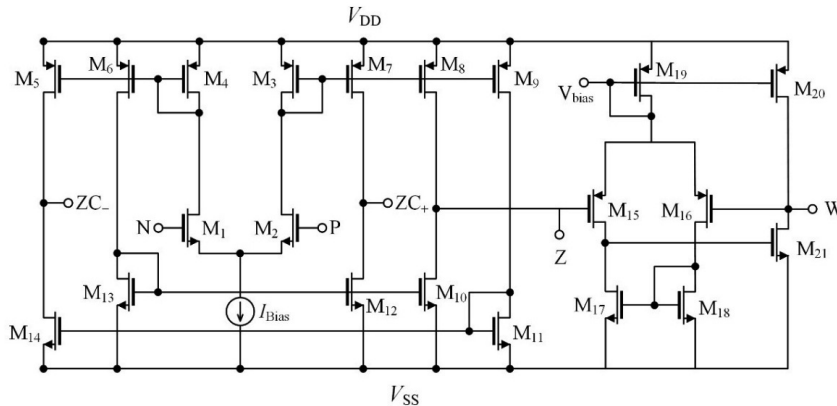

Figure 2. CMOS implementation of VDBA.

III. Layout Design

The complete layout of the VDBA is designed using Silterra Malaysia 0.18µm PDK in Cadence Virtuoso design software. The high performance nhp and php MOS transistors from the Silterra library are used for the design. To minimize the effect of parasitics, the transistors are put as close as possible. Two levels of metal layers are used for the interconnections. The complete layout is presented in Figure 3. The layout occupies an area of 27.68µm*24.25µm.
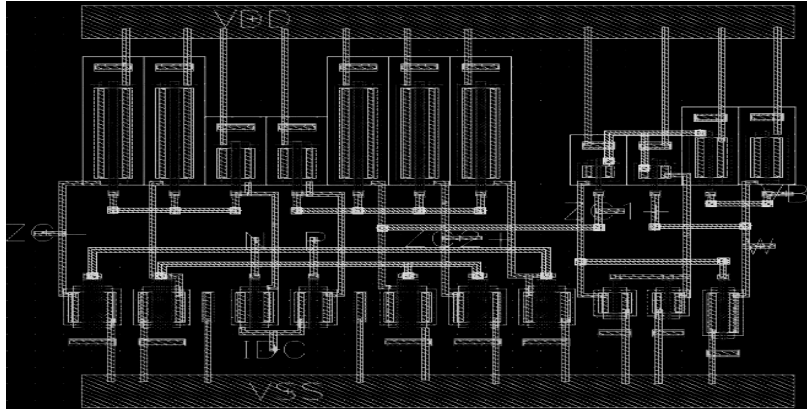

Figure 3. Layout of the VDBA.

IV. Proposed Universal Filters

In this research, three minimum component MISO universal filters are proposed. The proposed filters did not require any passive component matching conditions and provide low output impedance in case of voltage mode output and high impedance in case of current mode output; hence, they are cascadable.

4.1. Dual Mode Voltage Mode and Transadmittance Mode Filter

A dual mode filter employing three VDBAs is presented in Figure 4. The proposed filter is resistor less and utilize only two capacitors as passive elements. In the implementation, one of the capacitors is grounded, which is advantageous for fabrication, as well as for noise cancellation. The filter can work in two modes of operation, namely, VM and TAM, and can provide the VM and TAM output simultaneously. The features of the filter include inbuilt tunability, independent control of quality factor and pole frequency, dual mode of operation, availability of explicit current output from high impedance node and voltage output from low impedance node simultaneously, use of only two passive elements, resistorless implementation and no requirement of negative or double input signals to realize filter responses.
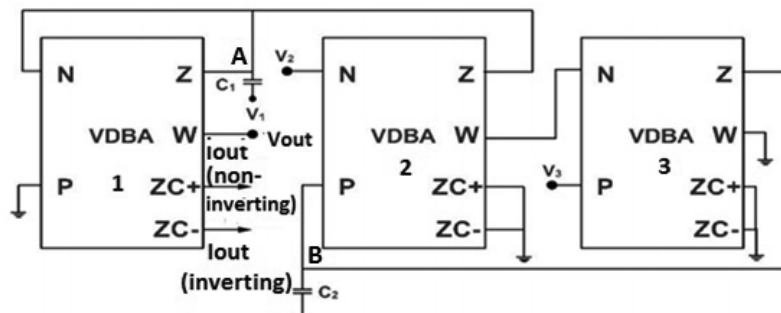

Figure 4. VM and TAM dual mode universal filter.

The filter transfer functions are given in Equations 11 and 13 and expressions for pole frequency and quality factor are summarized in Equations 16-17. The transconductance of the VDBA is represented by g_m (m=1, 2 and 3). The g_m is varied by changing the bias current of the OTA (I_{bias1}, I_{bias2} and I_{bias3}) providing tunability to the filter.

The procedure adopted to evaluate the transfer function of the filter is explained below. According to the V-I relation of VDBA, the following relations are derived.

$$I_Z = I_{ZC+} = -I_{ZC-} = g_m(V_P - V_N) \tag{3}$$

$$V_Z = V_W \tag{4}$$

Applying KCL at node A

$$-V_{out}g_1 + (V_B - V_2)g_2 = (V_{out} - V_1)sC_1 \tag{5}$$

$$V_Bg_2 - V_2g_2 + V_1sC_1 = V_{out}sC_1 + V_{out}g_1 \tag{6}$$

Applying KCL at node B

$$(V_3 - V_{out})g_3 = V_BsC_2 \tag{7}$$

$$V_B = \frac{(V_3g_3 - V_{out}g_3)}{sC_2} \tag{8}$$

Putting the value of Equation 8 in Equation 6, we get

$$\frac{V_3g_3g_2}{sC_2} - \frac{V_{out}g_3g_2}{sC_2} - V_2g_2 + V_1sC_1 = V_{out}sC_1 + V_{out}g_1 \tag{9}$$

Reorganizing the terms to get V_{out} leads to

$$V_{out} = \frac{\dfrac{S^2C_1C_2}{g_2g_3}V_1 - \dfrac{SC_2g_2}{g_2g_3}V_2 + V_3}{\dfrac{S^2C_1C_2}{g_2g_3} + \dfrac{SC_2g_1}{g_2g_3} + 1} \tag{10}$$

$$V_{out} = \frac{S^2C_1C_2V_1 - SC_2g_2V_2 + g_2g_3V_3}{S^2C_1C_2 + SC_2g_1 + g_2g_3} \tag{11}$$

$$I_{out} = I_{ZC+} = I_{ZC-} = g_1V_{out} \tag{12}$$

$$I_{out} = g_1\left[\frac{S^2C_1C_2V_1 - SC_2g_2V_2 + g_2g_3V_3}{S^2C_1C_2 + SC_2g_1 + g_2g_3}\right] \tag{13}$$

$$D(s) = S^2C_1C_2 + SC_2g_1 + g_2g_3 \tag{14}$$

$$D(s) = S^2 + s\frac{g_1}{C_1} + \frac{C_1C_2}{g_2g_3} \tag{15}$$

$$\omega_o = \sqrt{\frac{g_2g_3}{C_1C_2}} \tag{16}$$

$$Q = \frac{1}{g_1} \sqrt{\frac{g_2 g_3 C_1}{C_2}} \tag{17}$$

Table 2 provides the excitation sequence of the filter for response realization.

Table 2. Input voltage excitation sequence.

Response	Inputs		
	V_1	V_2	V_3
LP	0	0	1
HP	1	0	0
BP	0	1	0
NP	1	0	1
AP	1	1	1

4.2. Dual Mode Current Mode and Transimpedance Mode Filter

A dual mode filter employing three VDBAs is presented in Figure 5. The proposed filter utilizes two capacitors and a single resistor as passive element. In the implementation, both the capacitors are grounded, which is advantageous for fabrication, as well as for noise cancellation. The filter can work in two modes of operation namely, CM and TIM, and can provide the CM and TIM outputs simultaneously. The features of the filter include inbuilt tunability, use of grounded passive elements, dual mode of operation, availability of explicit current output from high impedance node and voltage output from low impedance node simultaneously and no requirement of negative or double input signals to realize filter responses.
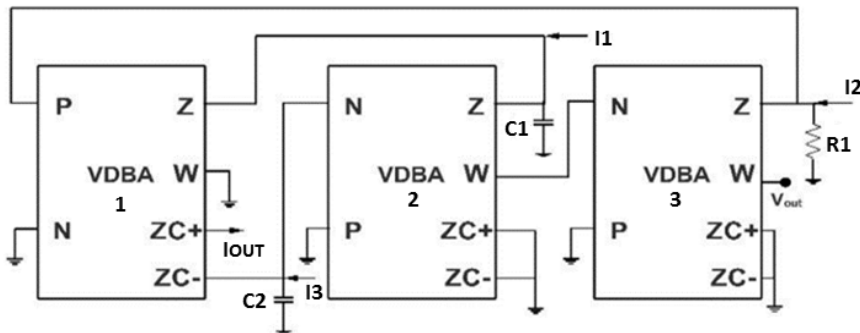
Figure 5. CM and TIM dual mode universal filter.

The filter transfer function and expressions for pole frequency and quality factor are summarized in Equations 18-21. To realize a filter with unit gain, $(g_2 R_1 = 1)$ must be satisfied. The transconductance of the VDBA is represented by g_m (m=1, 2 and 3). The g_m is varied by changing the bias current of the OTA (I_{bias1}, I_{bias2} and I_{bias3}) providing tunability to the filter. To design the filter for unity gain $g_1 = g_2$ is kept and g_3 is varied to change the frequency of operation.

$$I_{out} = g_2 R_1 \left[\frac{S^2 C_1 C_2 I_2 - S C_2 g_1 I_1 + g_3 g_1 I_3}{S^2 C_1 C_2 + S C_2 g_1 g_2 R_1 + g_1 g_3 g_2 R_1} \right] \tag{18}$$

$$V_{out} = R_1 \left[\frac{\left(\frac{S^2 C_1 C_2}{g_3 g_1} \right) I_2 - \left(\frac{S C_2}{g_3} \right) I_1 + I_3}{\frac{S^2 C_1 C_2}{g_3 g_1 g_2 R_1} + \frac{S C_2}{g_3} + 1} \right] \tag{19}$$

$$\omega_o = \sqrt{\frac{g_3 g_1 g_2 R_1}{C_1 C_2}} \tag{20}$$

$$Q = \sqrt{\frac{g_3 C_1}{g_2 g_1 C_2 R_1}} \tag{21}$$

Table 3 provides the excitation sequence for the filter for response realization.

Table 3. Input current excitation sequence.

Response	Inputs		
	I_1	I_2	I_3
LP	0	0	1
HP	0	1	0
BP	1	0	0
NP	0	1	1
AP	1	1	1

4.3. Voltage Mode Filter

The proposed filter using the VDBA is shown in Figure 6. The filter makes use of a single VDBA, two capacitors, and a resistor and can realize all five filter functions by appropriately applying the input signals. The filter did not require any passive components matching condition for response realization. In addition, the filter output is available from low impedance node. A number of variants of VDBA can be found in the literature like VDIBA and FB-VDBA but none of the single active block based filters proposed using them enjoys the feature of low output impedance.
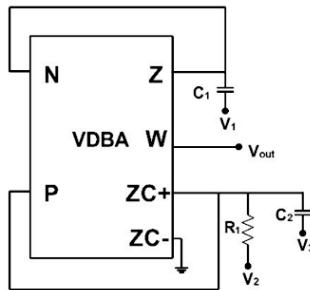
Figure 6. VM universal filter.

The filter transfer function and expressions for pole frequency and quality factor are summarized in Equations 22-24. The input sequence is given in Table 4. The filter requires a simple active matching condition of ($g_1 * R_1 = 1$). This can be easily met by selecting R_1 and then adjusting the bias current of the OTA to satisfy the condition.

$$V_{out} = \frac{S^2 C_1 C_2 R_1 / g_1 \, V_1 + S C_2 R_1 V_3 + V_2}{S^2 C_1 C_2 R_1 / g_1 + S C_2 R_1 + 1} \tag{22}$$

$$\omega_o = \sqrt{\frac{g_1}{R_1 C_2 C_1}} \tag{23}$$

$$Q = g_1 \sqrt{\frac{C_1}{C_2 R_1}} \tag{24}$$

Table 4. Input voltage excitation sequence.

Response	Inputs			Active Matching Condition
	V_1	V_2	V_3	
LP	0	1	0	$g_1 * R_1 = 1$
HP	1	0	0	$g_1 * R_1 = 1$
BP	0	0	1	$g_1 * R_1 = 1$
NP	1	1	0	$g_1 * R_1 = 1$
AP	1	1	-1	$g_1 * R_1 = 1$

V. Non-Ideal Analysis

The nonideal model of the VDBA is presented in Figure 7. As can be deduced from the figure, the various parasitic resistance and capacitance appear in parallel with the input and output nodes of the device. The low impedance X node has a parasitic resistance and inductance in series with it.

The other nonideal effects that influence the response of the VDBA are the frequency dependent nonideal voltage (β) and transconductance transfer (γ/γ') gains. These gains cause a slight change in the current and voltage signals during transfer leading to undesired response. Taking into account the nonideal gains, the V-I characteristics of the VDBA will be modified as follows.

$$I_Z = I_{ZC} = \gamma g_m (V_P - V_N) \tag{25}$$

$$I_{ZC-} = \gamma' g_m (V_P - V_N) \tag{26}$$

$$V_Z = \beta V_W \tag{27}$$

The nonideal analysis considering the effect of nonideal current and voltage transfer gains is carried out for all the proposed filters to see its effect on the transfer function, pole frequency and quality factor of the proposed filters. The modified expressions of filter transfer function, quality factor, and pole frequency for all the three design are presented below. The nonidealities result in deviations from the expected value.
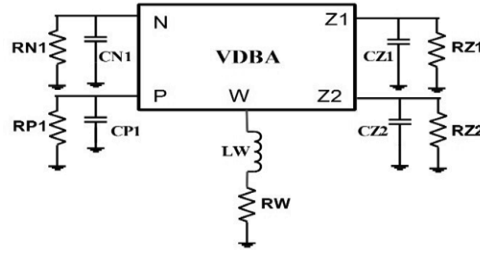
Figure 7. Nonideal Model of VDBA.

Nonideal results for the dual mode VM and TAM filter are given in Equations 28–30. The analysis results for dual mode CM and TIM filter are given in Equations 31–33. The nonideal analysis results for the VM single VDBA filter are presented in Equations 34–36.

$$V_{out} = \frac{S^2 C_1 C_2 V_1 - S\gamma C_2 g_2 V_2 + \gamma^2 g_2 g_3 V_3}{S^2 \beta C_1 C_2 + S\beta\gamma C_2 g_1 + \gamma^2 g_2 g_3} \tag{28}$$

$$\omega_o = \gamma \sqrt{\frac{g_2 g_3}{\beta C_1 C_2}} \tag{29}$$

$$Q = \frac{1}{g_1} \sqrt{\frac{g_2 g_3 C_1}{\beta C_2}} \tag{30}$$

$$I_{out} = \beta g_2 R_1 \left[\frac{S^2 C_1 C_2 I_2 - S\gamma C_2 g_1 I_1 + g_3 g_1 \gamma I_3}{S^2 C_1 C_2 + S\gamma\beta C_2 g_1 g_2 R_1 + \gamma\beta g_1 g_3 g_2 R_1} \right] \tag{31}$$

$$\omega_o = \sqrt{\frac{\beta\gamma g_3 g_1 g_2 R_1}{C_1 C_2}} \tag{32}$$

$$Q = \sqrt{\frac{g_3 C_1}{\beta\gamma g_2 g_1 C_2 R_1}} \tag{33}$$

$$V_{out} = \frac{\left(S^2 C_1 C_2 R_1 \big/ \gamma g_1 + SC_1 \big/ \gamma R_1 g_1 - SC_1 \right) V_1 + SC_2 V_3 + \dfrac{V_2}{R_1}}{S^2 C_1 C_2 \beta \big/ \gamma g_1 + SC_2 \beta + SC_1 \beta \big/ \gamma R_1 g_1 - SC_1 \beta + \dfrac{\beta}{R_1}} \tag{34}$$

$$\omega_o = \sqrt{\frac{\gamma g_1}{R_1 C_2 C_1}} \tag{35}$$

$$Q = g_1 \sqrt{\frac{\gamma C_1}{C_2 R_1}} \tag{36}$$

As a result of component tolerance and nonidealities in VDBA, the response of the practical filter deviates from the ideal one. To get a measure of the deviation, the concept of sensitivity is employed. Mathematically, sensitivity is defined as $S_x^y = \lim_{\Delta X - \infty} \left\{ \frac{\Delta y/y}{\Delta x/x} \right\} = \frac{x}{y} \frac{\partial y}{\partial x}$, where X is the component that is varied, and Y is the filter frequency (ω_P) and quality factor Q in our case.

The sensitivities of ω_o and Q with respect to the nonideal gain and passive elements are given below. The sensitivities for the dual mode VM and TAM filter are given in Equations 37-40. The sensitivity analysis results for dual mode CM and TIM filter are given in Equations 41-42. The sensitivities for the VM single VDBA filter are presented in Equations 43–45. The sensitivities are not more than one, which is desired.

$$-S_{C_1}^\omega = -S_{C_2}^\omega = S_\beta^\omega = S_{g_3}^\omega = S_{g_2}^\omega = \frac{1}{2} \tag{37}$$

$$S_\gamma^\omega = 1 \tag{38}$$

$$S_{C_1}^Q = S_{g_3}^\omega = S_{g_2}^\omega = -S_{C_2}^Q = -S_\beta^Q = \frac{1}{2} \tag{39}$$

$$S_{g_1}^Q = 1 \tag{40}$$

$$S_\beta^\omega = S_\gamma^\omega = S_{g_1}^\omega = -S_{g_2}^\omega - S_{g_3}^\omega = -S_{C_2}^\omega = S_{R_1}^\omega = -S_{C_1}^\omega = \frac{1}{2} \tag{41}$$

$$S_{g_3}^Q = S_{C_1}^Q = -S_{C_2}^Q = -S_\beta^Q - S_\gamma^Q = -S_{g_2}^Q = -S_{g_1}^Q = -S_{R_1}^Q = \frac{1}{2} \tag{42}$$

$$-S_{C_1}^\omega = -S_{C_2}^\omega = -S_{R_1}^\omega = S_\gamma^\omega = S_{g_1}^\omega = \frac{1}{2} \tag{43}$$

$$S_{C_1}^Q = -S_{C_2}^Q = -S_{R_1}^Q = \frac{1}{2} \tag{44}$$

$$S_{g_1}^Q = 1 \tag{45}$$

VI. Post Layout Simulation Results

To examine the designed filters, the VDBA is designed using 0.18μm Silterra Malaysia PDK in Cadence Virtuoso design software. The parasitic extraction was done using the Mentor Calibre tools. The width and length ratios of the VDBA are given in Table 5. The supply voltage is set at ±1.25V, and the OTA bias current was fixed at 100μA. Table 6 gives the performance metrics of the designed VDBA.

**Table 5.** Width and length of the MOS transistors.

Transistor	Width (μm)	Length (μm)
M1-M4	1.8	0.36
M5-M9	5.4	0.36
M11-M14	1.8	0.36
M15-M16	1.8	0.36
M17-M18	1.2	0.36
M21	2.4	0.36
M19-M20	4.8	0.36

Table 6. Performance parameters of the designed VDBA.

Parameters	Silterra 0.18μm (VDD=-VSS=1.25V)
Voltage gain (V_W/V_Z)	0.985
Voltage transfer Bandwidth (V_W/V_Z)	3.0262 GHz
DC Voltage Range ($V_Z - V_W$)	±900mV
Static Power Dissipation	1.618mW
Parasitic Resistance at node (RW)	140.89Ω
ZC+ node resistance	64.4kΩ
ZC- node resistance	64.4kΩ

The dual mode VM and TAM MISO filter presented in Figure 4 is validated first by designing it for -3dB cutoff frequency of 7.213 MHz and quality factor of one. According to Equations 16-17 the passive elements are selected as follows C_1=20pF and C_2=20pF. The OTA bias current for all the three VDBA is set at 100μA to achieve $g_{m(1-3)}$ =906.53μS. The ideal and postlayout frequency response of the filter is given in Figure 8 and the AP response is shown in Figure 9 (a-b). The power dissipation of the filter for bias current of 80μA for all three VDBA is found to 5.47mW.
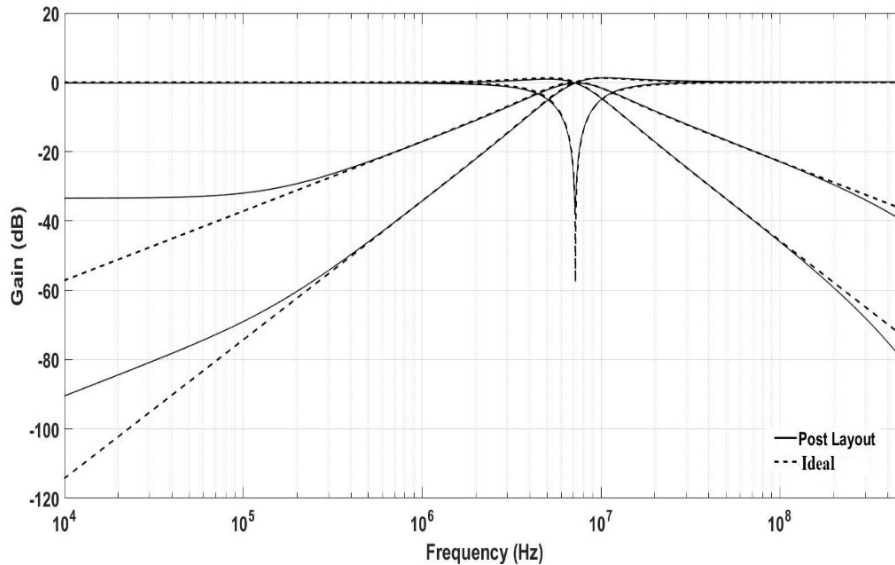
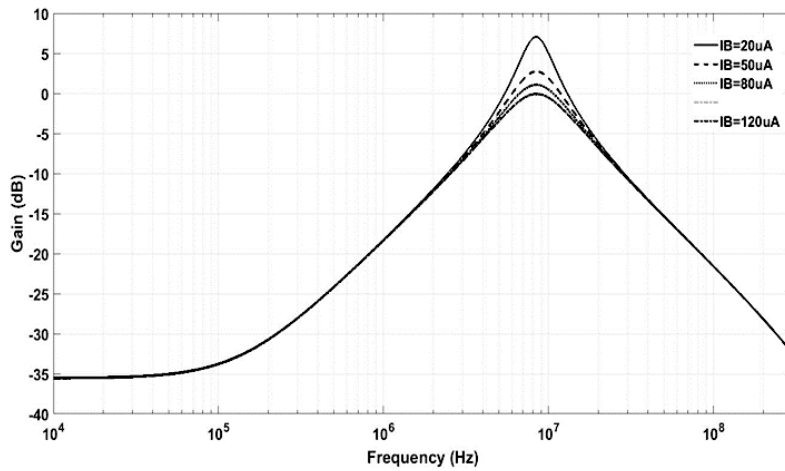**Figure 8.** VM response of the dual mode filter.

(a)

(b)
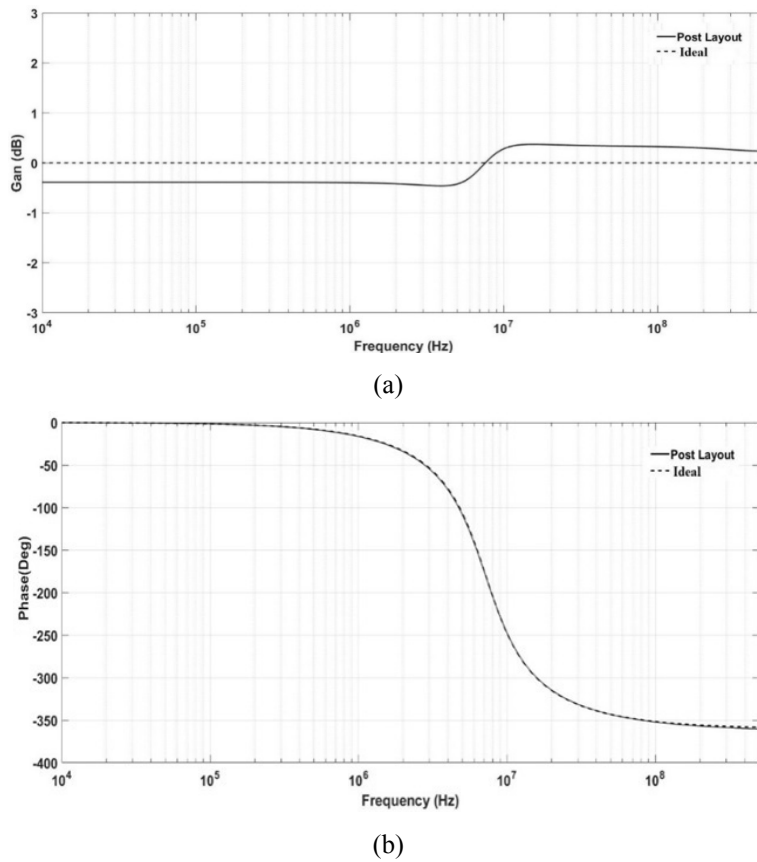
Figure 9. VM all pass response of the dual mode filter (a) Magnitude (b) Phase.

To validate the signal processing capability of the filter, a transient analysis is carried out. A 100mV input signal at 7.21 MHz frequency is applied, and the BP output is observed. It can be inferred from Figure 10 that the filter functions correctly. In addition, the quality factor tuning is tested by varying the OTA bias current of first VDBA of the MISO filter. According to Equations 16-17, the quality factor can be tune independent of frequency as can be observed from Figure 11. The total harmonic distortion (THD) is measured for BP configuration. The THD remains within 6% till 250mV input voltage range.
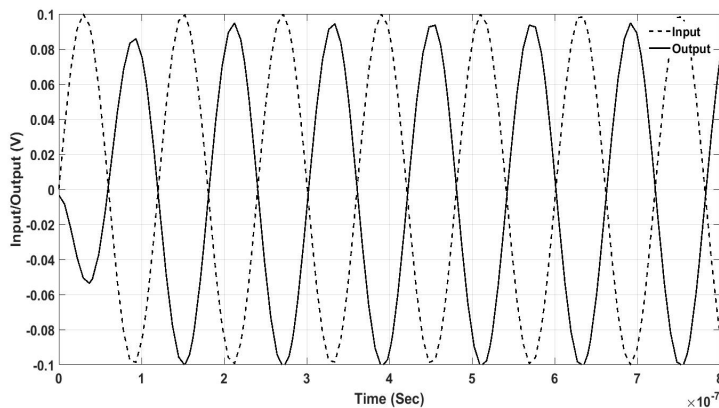
**Figure 10.** Transient analysis of the VM filter.

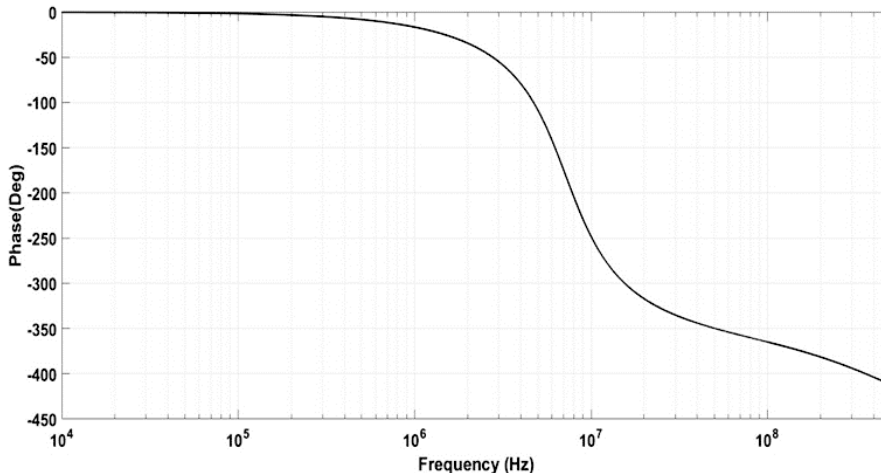**Figure 11.** TAM response of the dual mode filter.

The TAM mode postlayout frequency responses of the filter are presented in Figure 12 and 13 at the designed frequency of 7.213 MHz. These pre- and postlayout results validate that the filter can work in dual mode simultaneously.
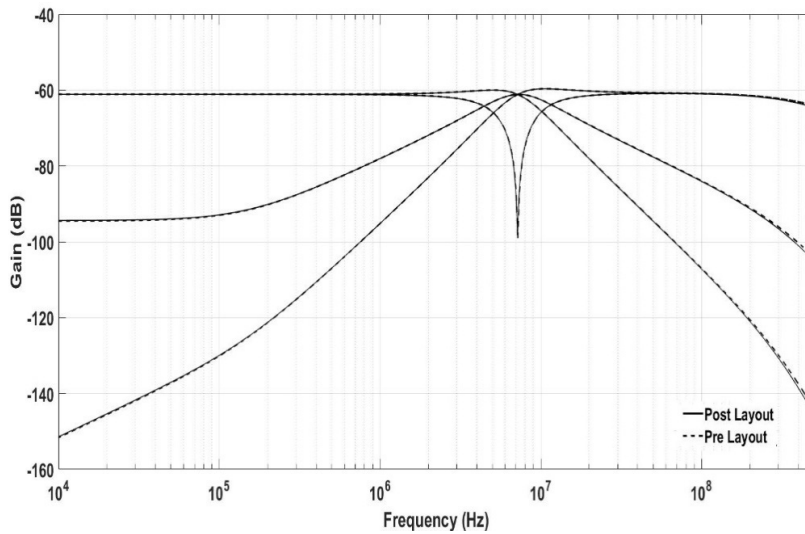
Figure 12. TAM response of the dual mode filter.
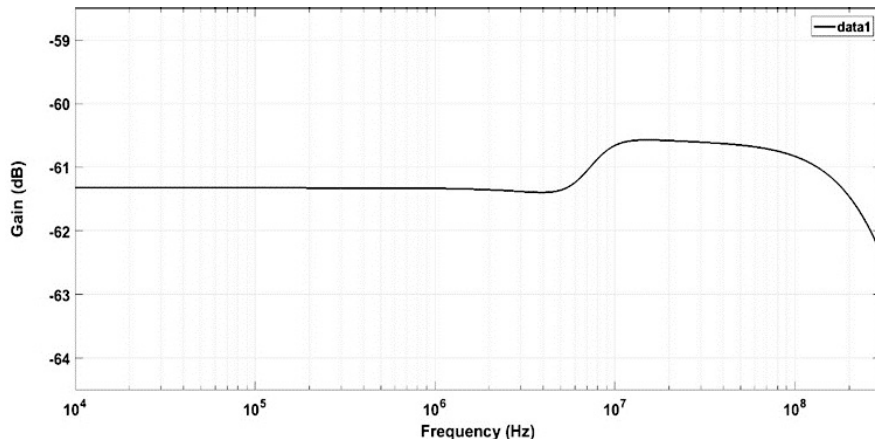
(a)

(b)

Figure 13. TAM all pass response of the dual mode filter: (a) magnitude; (b) phase.

The dual mode MISO CM and TIM filter employing three VDBAs presented in Figure 5 is validated by designing it for -3dB cutoff frequency of 4.562 MHz. According to Equations 20-21, the passive elements are selected as follows: C_1=25pF, C_2 =40pF and R_1=1.1kΩ. The OTA bias current for all three VDBA is set at 100μA to achieve $g_{m(1-3)}$ =906.53μS. To design filter with unity gain, the condition of ($g_{m(2)}*R_1 = 1$) must be satisfied. The ideal and postlayout frequency response of the current mode filter is given in Figure 14, and the AP response is shown in Figure 15. The power dissipation of the filter for bias current of 80μA for all three VDBAs is found to 5.49mW.
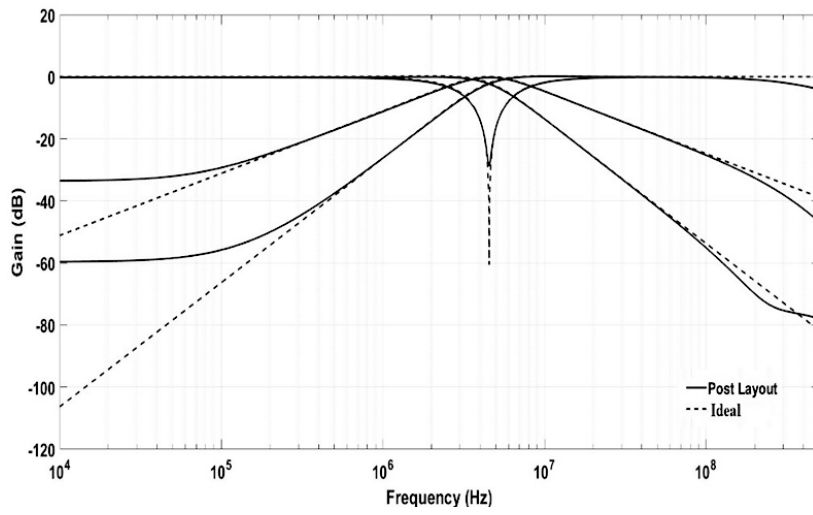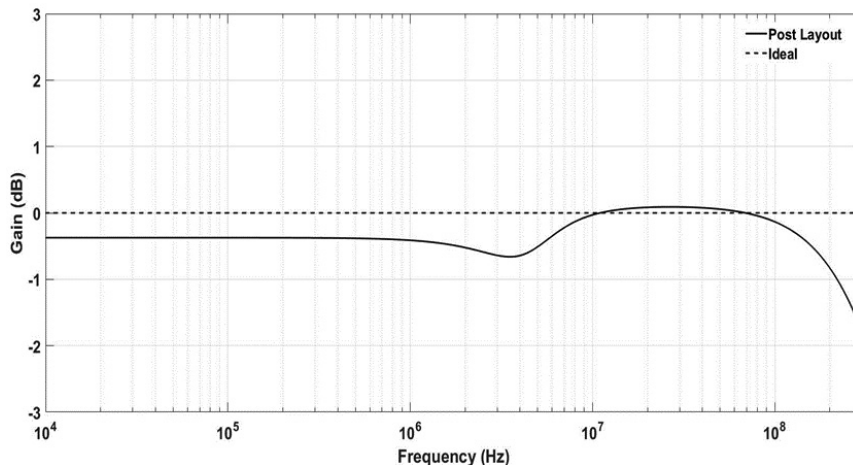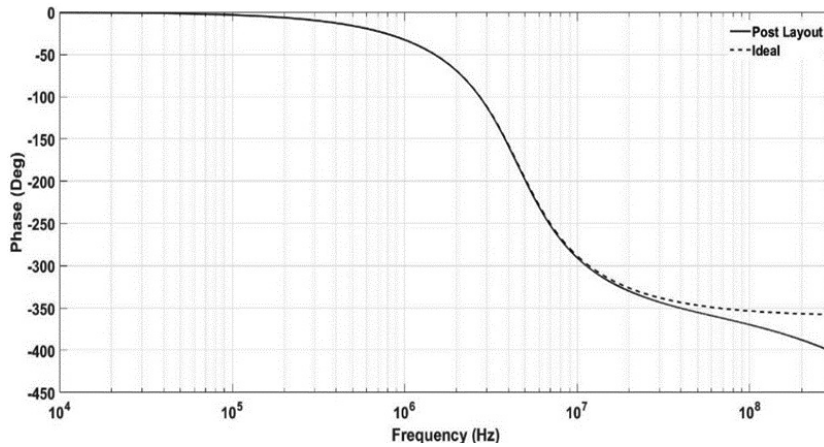
Figure 14. CM response of the dual mode filter.

(a)

(b)

Figure 15. CM all pass response of the dual mode filter: (a) magnitude; (b) phase.

To validate the signal processing capability of the filter transient analysis is carried out. A 100μA input signal at 4.562 MHz frequency is applied and the BP output is observed. It can be inferred from Figure 16 the functions correctly.
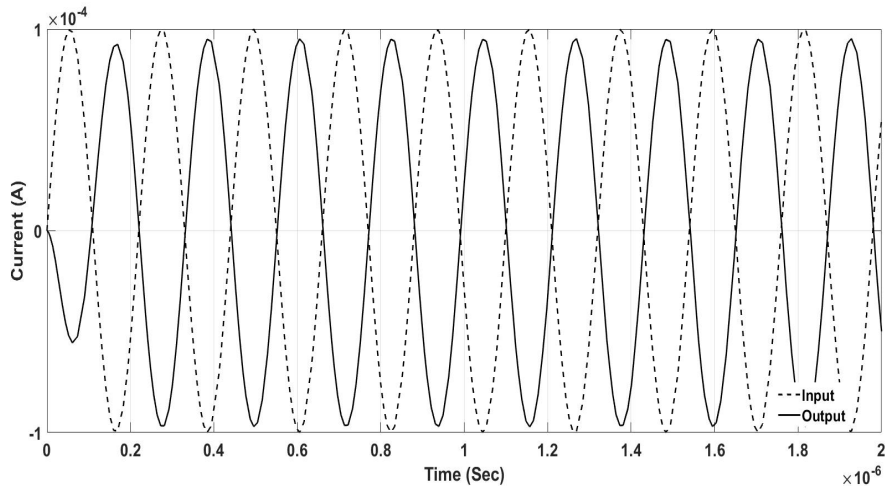

Figure 16. Transient analysis of the CM filter.

The TIM mode postlayout frequency response of the filter is presented in Figures 17-18 at the designed frequency of 4.562 MHz. This validates that the filter can work in dual mode simultaneously.
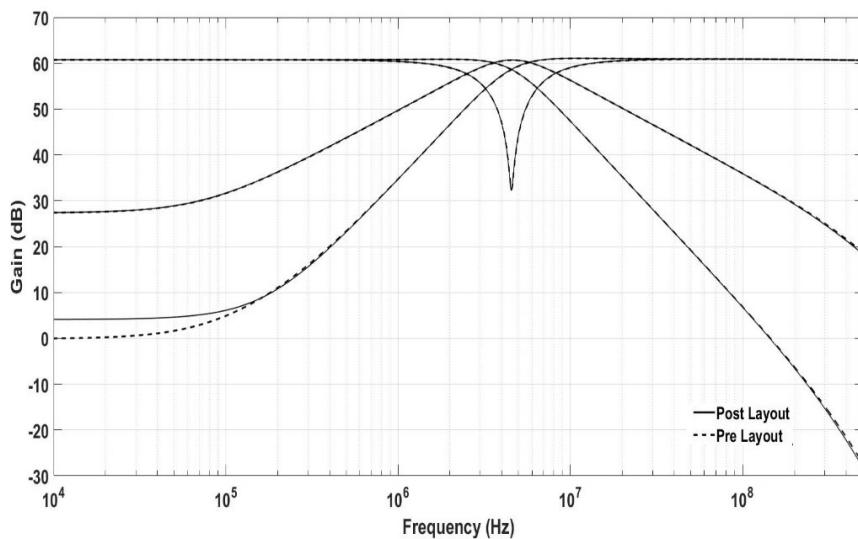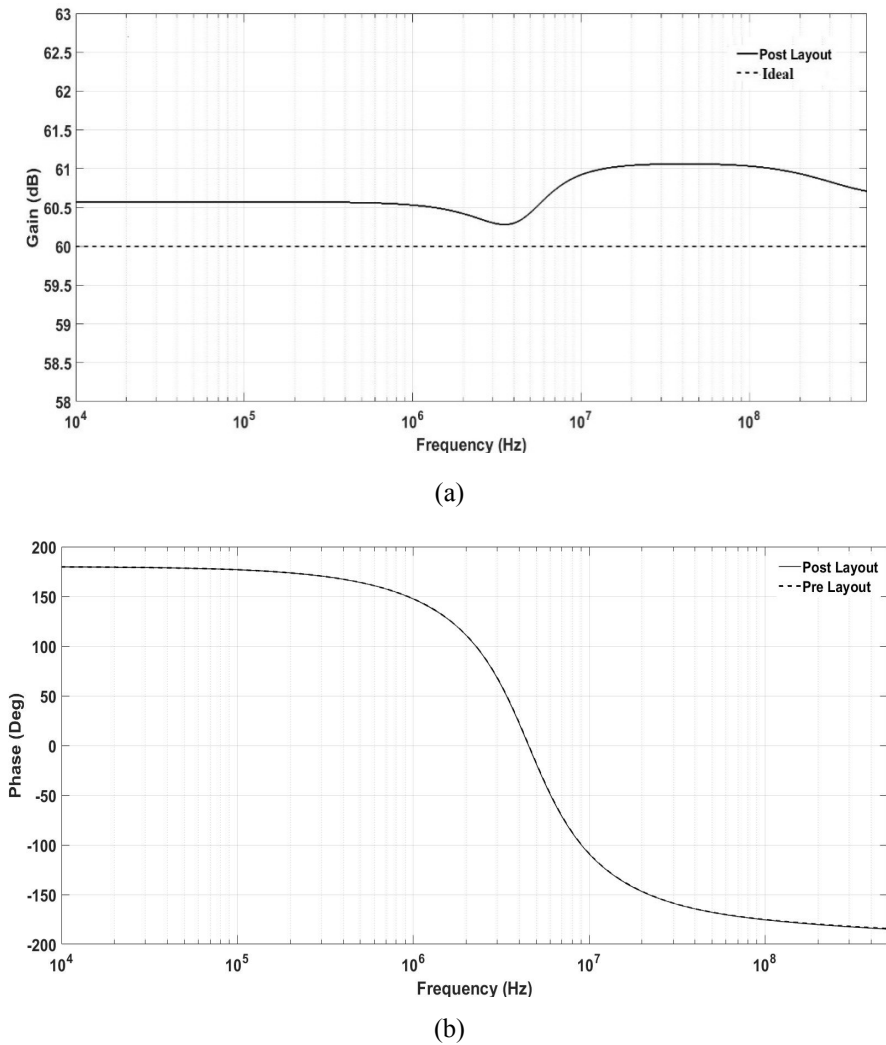

Figure 17. TIM response of the dual mode filter.

(a)

(b)

Figure 18. TIM all pass response of the dual mode filter: (a) magnitude; (b) phase.

The VM MISO filter employing single VDBA presented in Figure 6 is validated by designing it for -3dB cutoff frequency of 7.224 MHz. According to Equations 23-24 the passive elements are selected as follows C_1=20pF and C_2=20pF. The transconductance of the VDBA is set at $g_{m(1)}$ =906.53μS. The value of resistance is selected to be R_1=1.1kΩ to satisfy the condition of ($g_{m(1)}*R_1 = 1$). The ideal and postlayout frequency response of the filter is given in Figure 19, and the AP phase response is shown in Figure 20.
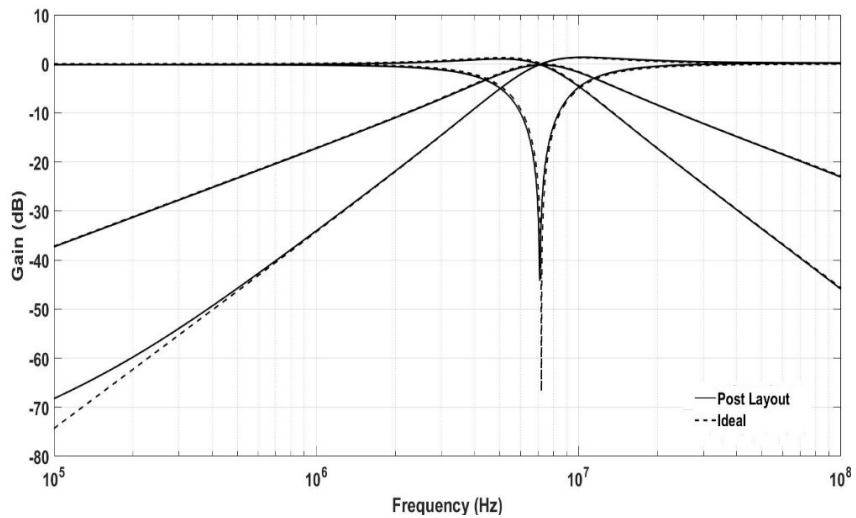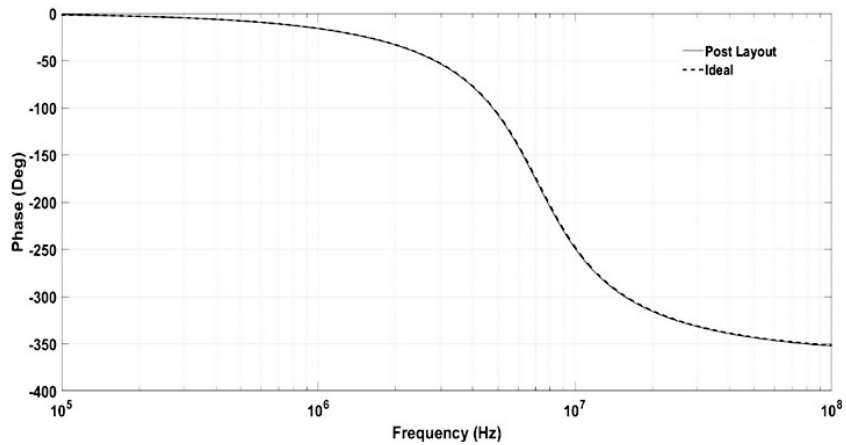
Figure 19. VM filter response.

Figure 20. VM all pass phase response.

In order to bring out the merits of the proposed VDBA based filters they are compared with the other VDBA, VDIBA and VD-DIBA based filters since all of these have VDBA as core ABBs. The comparison is done based on the following criteria (i) Number active blocks employed (ii) number of passive elements used (iii) passive elements matching condition (iv) use of negative input for filter response realization (v) requirement of double input for filter response (vi) availability of output at low impedance node for VM and TIM and availability of output at high impedance node for CM and TAM (vii) number of modes realized (viii) independent control of quality factor and pole frequency (ix) test frequency and (x) can realize all five filter functions (xi) supply voltage (xii) power dissipation. The comparison is presented in Table 7.

Table 7. Comparative study of VDBA based filters.

Reference	(i)	(ii)	(iii)	(iv)	(v)	(vi)	(vii)	(viii)	(ix)	(x)	(xi)	(xii)
(Pushkar et al. 2014)	1	3	No	No	No	No	VM	No	1.34 MHz	Yes	±2V	-
(Gupta et al. 2015)	2	2	No	No	No	Yes	VM	No	12.9 MHz	Yes	±0.75V	2.8mW
(Sokmen et al. 2016)	2	2	No	No	No	No	VM	Yes	1 MHz	No	±0.4V	-
(Herencsar et al. 2013)	1	2	No	No	No	No	VM	No	1.59 MHz	Yes	±0.9V	10.5mW
(Pushkar et al. 2013)	1	3	Yes	No	Yes	Yes	VM	No	kHz Range	Yes	-	10.5mW
(Kaçar et al. 2012)	2	2	No	Yes	No	Yes	VM	No	1.19 MHz	Yes	±1.5V	1.94mW
Authors Work Figure 4	3	2	No	No	No	Yes	VM, TIM	Yes	8.315 MHz	Yes	±1.25V	5.47mW
Authors Work Figure 5	3	3	No	No	No	Yes	CM, TAM	No	5.193 MHz	Yes	±1.25V	5.49mW
Authors Work Figure 6	1	3	No	Yes	No	Yes	VM	No	7.8 MHz	Yes	±1.25V	1.82mW

It is clear from the table that the two dual mode filters proposed are the first ever reported VDBA based filters working in dual mode simultaneously. In addition, all the design provides voltage output at low impedance node and current output at high impedance node, which is an advantage over others.

VII. CONCLUSION

In this research, three novel VDBA based universal filters are proposed. Two of the proposed filters can work in dual mode simultaneously. All the designed filters did not require any passive components matching and are cascadable. The complete layout of the VDBA is designed, and all the proposed filters are validated using the postlayout simulations. Additionally, the effect of nonideal frequency dependent voltage and transconductance transfer gains on the performance of the filter circuits is also studied. Furthermore, the sensitive analysis is also performed. Enough postlayout simulation results are provided to validate the correct functioning of proposed filters.

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