Optical Data Centers Router Design with Fiber Delay Lines and Negative Acknowledgement

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ABSTRACT

Optical packet switch/optical interconnect will be an integral part of high speed switching and datacenter applications. In recent past Arrayed Waveguide Grating (AWG) based designs have shown promising solutions for contention resolution and packet routing. Most of the designs take the advantage of wavelength parallelism and wavelength-based routing nature of AWG. In general, two classes of design have emerged: buffer-less and with buffer. In recent past the concept of All-Optical Negative Acknowledgement (AO-NACK) is introduced in case of buffer-less design. Here, in case of dropping of packet a negative acknowledgement is sent back to the sender to retransmit the packet. The drawback of the scheme is that the numbers of retransmitted packets are huge in buffer-less design. In this paper, a buffer-based design is presented where both buffer and negative acknowledgement areutilized to reduce the number of transmitted packets to 3000 times compared with buffer-less design, in case of transmission of 10^6packets. Moreover, negative acknowledgement hardware design is simplified significantly.

Keywords: Optical packet Switch, TWC, AWGR, Buffer and FDL.

INTRODUCTION

Optical interconnectsare considered as promising solution in data centres and high-speed computing. Various optical interconnect design has been proposed in the past, which provides low latency and very high throughput. Some of the notable projects are DOS (Ye et al., 2004), OSMOSIS (Hemenway et al., 2004), LIONS (Yin et al., 2012), etc. In past Arrayed Waveguide Grating Router (AWGR) based optical switches are investigated heavily as AWGR structure support optical parallelism, and they are non-blocking and scale linearly (Yin et al., 2012, Rastegarfar et al., 2013, Srivastava et al., 2010, Shukla et al., 2016, Shukla et al., 2016,Shukla et al., 2016, Proietti et al., 2012, Niwa et al. 2012). Huge disadvantages in optical switching is the nonexistence of optical RAMs, which makes all-optical solution as a difficult alternative in data enters applications where packet-loss must be avoided. As an alternative to optical RAMs, currently Fibre Delay Lines (FDL) is considered as a viable solution. However, in FDL, delay is limited due to the accumulated noises of the components used to realize the buffer. These FDL can significantly bring down the loss of packets, but they fail to bring down the packet loss to zero. The DOS architecture considers a loopback buffer and flow control mechanism to control the contending packets, thus avoiding packet loss, but overall switch design is very complex and its uses a large number of power hungry components.

The architecture proposed by Proietti et al. 2012 is basically a buffer-less switch and if contention happens then for dropped packets a negative acknowledgement is sent back to the sender and contending packet is retransmitted. In

this paper, an optical switch design for optical data centers is proposed with optical FDL based buffer for the storing of contending packets, along with negative acknowledgement mechanism. The detailed physical and network layer analysis of the switch is performed, and it has been found that the proposed switch design is much superior to earlier design.

OPTICAL DATA CENTERS

In past various optical switch designs for optical data canters are proposed, with their advantages and disadvantages. The major economic scale requirements for data centers are as follows:

- *Lower Cost:* the cost of optical data center is one major issue, and cost of active components is comparatively larger in comparison to passive components. Therefore, recently proposed design relies on passive components to realize data centers design.

- *Scalability:* The scalability of switching ports is another issue, which is to be addressed. Currently optical circuit switches (OCS) based data centers may connect to some thousands of ports. Therefore, optical data centers, which can scale to large number of ports, are desirable.

- *Switching time:* Currently in OCS time of switching is commonly in ms, which is lesser than required for fast switching. The optical packet switching demands a switching time in nanosecond order. Therefore, processors that can meet such speed requirements and fast tunabilityof components are desirable.

- *Insertion loss:* As of now, insertion loss differs and relies on the correct port combination and coupling method. In most of the current data centers the insertion loss varies from 2 to 5 dB.However, with optical technology such low loss designs are not possible; therefore, a loss of less than 10 dB is acceptable, as it can easily compensate optical amplifiers, which supports amplification of more than one signal simultaneously.

RECENT DATA CENTERS DESIGN

The architecture proposed in (Shacham et al., 2009) is buffer-less; however, it uses a physical layer acknowledgment scheme to inform the senders when packet is successfully delivered to correct output port. In the similar context an AWGR based scheme is proposed in (Proietti et al. 2012); here in case of blocking or dropping of packet a Negative Acknowledgement (NACK) is sent to the senders to notify them and senders resend the packet again as shown in Figure 1. In this design a buffer-less AWGR is considered. In the figure, the path between circulators C2 and C3 is used for the label extractor where old label is extracted and after O/E transformation sends to the electronic controller, and a new label is inserted,fed with payload to generate packet with new information. This is done at the output of switch.

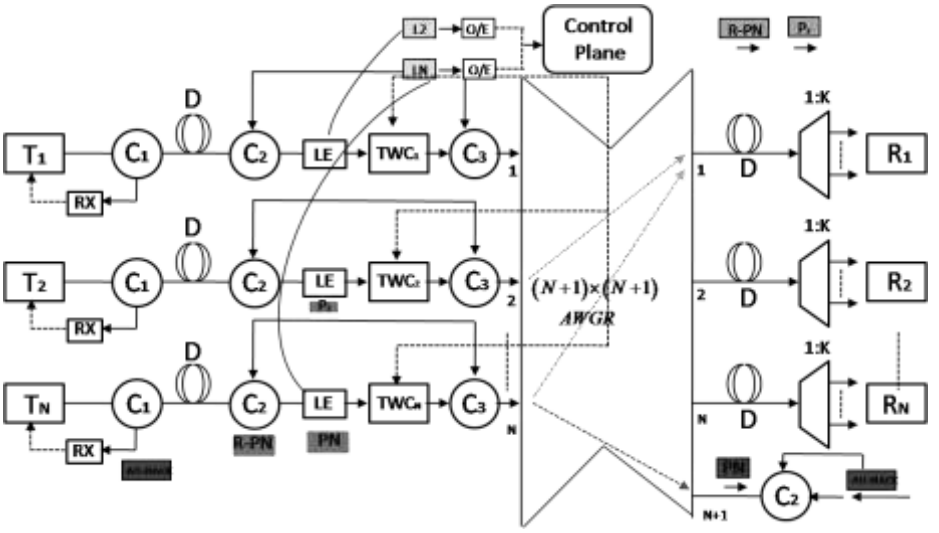

Figure 1. Schematic of the earlier switch (Proietti et al. 2012).

In Fig.1, the architecture proposed by Proietti et al. is shown. Here T_i represnets the i^{th} transmitter, and R_i represnets the i^{th} reciever. Here the generated information first pases through the circulator C_1 and then passes thorugh FDL of length D, and circulator C_2. Overhere, the label is extracted and as per the destination wavelength of the incoming paket is tuned to direct them to the appropiate output port of the AWG. In case of blocking, appropiate branch TWC tunes the wavelength of the packet such that it is blocked by AWG, and the AWG acts as reflecting grating, and reflected information choosing another path appears at circulator C_1 and it is transferred to appropiate transmitter where information is detected with assoicated Rx, and this negative acknowledgement mechanism allows the retransmission of blocked packets.

There are two modifications that should be incorporated in the design to improve its performance as follows:

1. As numbers of components used are large, physical losses of the components will degrade the signal quality; therefore, inclusion of optical amplifier is necessary.
2. To reduce retransmission of large numbers of packets at higher loads, inclusion of buffering mechanism is essential.

PROPOSED DESIGN

In past the authors of the paper (Srivastava et al., 2010) design an AWG based switch for the buffering of the contending packets, where contending packets wavelength selection is done using the AWG routing pattern either to occupy buffer or for direct transfer. In buffer, delay of 1 to B slots is possible; thus depending on the required delays various packets are placed in different delay lines. The delay will depend on the number of packets already placed in the buffer for a selected output. It is noticeable that, in each buffer FDL, only one packet is stored for a particular output; thus the maximum number of packets in each FDL module is equal to the total number of outputs. After the definite amount of delay packets appears on an input port of the scheduling AWG and again using the routing pattern of scheduling AWG, these packets will appear at the different output ports of the scheduling AWG (Shukla et al., 2014). Till this point the wavelengths of the packets will remain the same as tuned by input Tuneable Wavelength Convertors (TWCs). From here, packets will be transmitted to correct output port by tuning their respective wavelengths as per the routing pattern of switching AWG and desired output ports. Detailed description of the switch design can be found in (Srivastava et al., 2010). In this work an FDL based AWGR design, which is a modified version of the

above discussed design, is proposed where first contending packets are stored in FDL, to avoid contention. If packet cannot be stored then they are reflected back to the sender as a NACK. Thus, this scheme avoids retransmission of large numbers of packets by buffering them temporarily. This scheme is very beneficial in optical networks where large numbers of packets move in the connecting fiber links. This ACK/NACK scheme does not affect higher layer acknowledgment scheme.

The schematic of proposed data center switch is illustrated in Fig. 2. The core of the switch is a 2N×2N AWGR, which acts as a scheduling section while a N×N AWGR acts as a switching section, where 'N' is switch radix. The upper N port of scheduling AWGR used for creating FDL buffer, while theleftover lower N ports' ranges fromN+1 to 2N are actual input and output ports. The TWC at the input of each line is tuned in each time slot to assign proper wavelength to incoming packet such that it can either be transmitted directly towards the output or in case of contention it can be stored in the buffer. Packets stored in the FDL buffer will leave the buffer automatically after a definite amount of time depending on the length of the FDL on identical wavelength as in the buffer, from where it can be switched towards the correct output using TWC and AWGR of switching section.

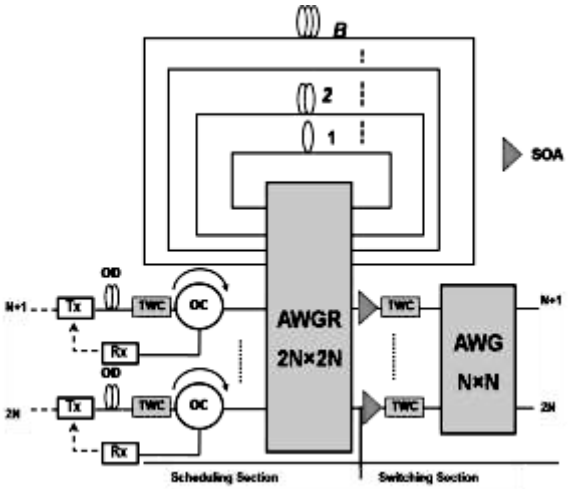

Figure2. Schematic of the proposed switch.

If the contention packet cannot be placed in the FDL buffer due to the unavailability of buffer wavelength or space,it will be considered as lost. But in datacenter this loss should be avoided; thus a mechanism is needed to avoid this loss. Ideally an infinite buffer would be required to avoid any loss, which is impractical. As an alternative solution, retransmission of loss packet is a possible solution.

In the switch design modifications are suggested which would automatically let the transmitter know about the packet loss thatcan be retransmitted again. In the design Tx is transmitter or sender who generates packets. At the switch input the header of the packet is separated and processed electronically and thereafter wavelength of the TWC is tuned appropriately either to direct the packet (payload) towards the output or to place it in the buffer. As AWGR requires 2N wavelengths to connect and input port to any output port. The path as in Fig. 1 will remain the same, and therefore for the simplicity is omitted in the design shown on Fig.2. Thus, a tunable range of TWC would be 2N+1. The additional wavelength (λ_{2N+1}) will be reflected by the AWGR. If a packet can be stored it is assigned wavelength λ_{2N+1} and it will be reflected and after passing through the Optical Circulator (OC) will reach to Rx (a dedicated receiver) which co-ordinated with Tx and Tx re-transmit packet again. The OC separate the forwarding packets and counter-propagating (travelling backwards) AO-NACKs.

The Semiconductor Optical Amplifier (SOA) is placed in each input branch of AWG to compensate the insertion losses of the various devices.

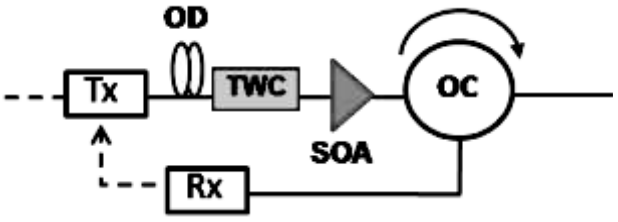

Figure 3. Schematic of SOA placement scheme in second configuration.

The purpose of using Optical Delay (OD) is twofold; first it is used to delay payload till header is processed and control action has been made. Depending on the processing speed of electronic controller length of OD is decided. Current electronic technology can handle data rates of 40 Gbps. Thus, corresponding OD length is negligibly small. Second it can be used to delay the packets depending on the AO-NACK detection scheme.

It can also be used as indicator of distance between the *Tx* and connected port of the AWGR. We will assume the same. Considering packet is of length '*L*'. Then,

Case 1: If $d=L/2OD > 1$, then AO-NACK will reach to the sender before the transmission of the same packet completes. Therefore, simple packet edge detection mechanism is good enough to detect AO-NACK and there will be no ambiguity regarding packet reference number.

Case 2: If $d=L/2OD < 1$, then AO-NACK will reach to the sender when the transmission of the packet is already finished. Then packet sequence number can be used to detect AO-NACK which can be attached ahead of payload in terms of some extra bits.

Finally, if counter running at the host expires, then it is assumed that packet has successfully deliveredto intended output.

PHYSICAL LAYER ANALYSIS OF THE SWITCH

In the previous work the distance form host to port of the AWG is found to be nearly 20 m we also have assumed the same. The length of the packet L which is also equal to the slot duration can be obtained using:

$$L = \frac{cb}{nR_b} \tag{1}$$

The lists of parameters used in above equation and in rest of the paper are detailed Table 1 and 2. In Fig. 4, length of the packet at different bit rates for different number of bits in a packet is shown. Considering Eq. 1, b is shown on X-axis and we consider varying bit-rates Rb in the system as 10, 20, 40, and 160 Gbps. As the number of bits increases, required fiber Length (plotted on Y-axis) at a particular bit rate also increases.

Table 1. Parameters list and value [Shukla et al. 2014].

Parameter	Value
Switch size (N)	16
Population inversion factor (n_{sp})	1.2
Optical amplifier gain (G)	19.5 dB
Speed of light (c)	3×10^{8} m/s
Refractive index (fiber) (n)	1.45
Responsivity (R)	1.28 A/W
Electronic charge (e)	1.6×10^{-19} C
Boltzmann Constant (K_B)	1.38×10^{-23} $m^2Kgs^{-2}K$
Temperature (T)	27^0 C
Load Resistance (R_L)	300 Ω
Electrical bandwidth	20 GHz
Optical bandwidth	40 GHz
TWC insertion loss	2.0 dB
AWG Loss (32 channels)	3.0 dB
Loss of SOA	1.0 dB
Loss of optical circulator	0.5 dB
Reflectivity	0.5

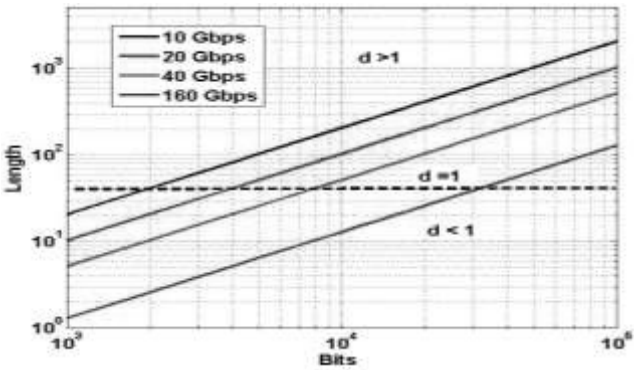

Figure4. Packet length for various bits in packets under different bitrates.

As shown in Fig.4 at 20Gbps, maximum number of bits transmitted at d=1(intersection) is 4000 bits. At 160 Gbps, maximum number of bits transmitted is 30000 bits. Hence, at higher bit rate large amount of information can be send. The black dotted line shows length of 40 m for which $d = 1$. The curve below dotted line has $d< 1$, while above dotted line $d> 1$. For fixed number of bits as the data rates increases the length of the packets in meter decreases. Therefore, $d=L/2OD \geq 1$, will most of the time will be satisfied, as large size packets will at high data rates will propagate in core optical network. Moreover, as we are considering the AO-NACK scenario, we should not worry about packet loss.

It is necessary to measure the performance of the switches both at physical and network layer, to prove hypothesis. In the next section physical layer analysis is presented to know minimum amount of required power for the correct

switch operation. This analysis aim to measures the loss, power, noise and BER for both direct or via buffer information transfer of packets. This analysis is also done for AO-NACK reception on the host side.

Physical layer analysis is essential to know about the minimum power requirement for the correct operation of the switch (Shukla et, al., 2014). In case of direct transfer of packet, the loss suffered by a packet is given by

$$A_T^D = L_{TWC} L_{OC} L_{AWG}^{2N\times 2N} L_{SOA} L_{TWC} L_{AWG} \tag{2}$$

In case of transfer of packet via buffer, the loss suffered by a packet is given by

$$A_T^B = L_{TWC} L_{OC} L_{AWG}^{2N\times 2N} L_{FDL} L_{AWG}^{2N\times 2N} L_{SOA} L_{TWC} L_{AWG} \tag{3}$$

The SOA compensates the loss in signal power, then the power received a the photodetector is

$$P_{out}(b) = bP_{in} + n_{sp}(G-1)h\nu B_o L_{TWC} L_{AWG}^{N\times N} \; b \in [0,1] \tag{4}$$

The gain of the amplifier is equal to the A_T^D or A_T^B depending on how packet is routed form scheduling AWG.

NOISE ANALYSIS

Due to the ASE noise of EDFA, shot and thermal noises various beating terms are present at the receiver as under(Srivastava et al., 2009, Olsson et al., 1990 & Shukla et al. 2016 Shukla et al., 2015):

Shot noise: $\sigma_s^2 = 2qRPB_e$

ASE-ASE beat noise: $\sigma_{sp-sp}^2 = 2R^2 P_{sp}(2B_o - B_e)\dfrac{B_e}{B_0^2}$

Sig-ASE beat noise: $\sigma_{sig-sp}^2 = 4R^2 P \dfrac{P_{sp} B_e}{B_0}$

Shot-ASE beat noise: $\sigma_{s-sp}^2 = 2qRP_{sp}B_e$

Thermal noise:$\sigma_{th}^2 = \dfrac{4K_B T B_e}{R_L}$ (5)

In the above noise expressions, the value of P and P_{sp} will be given by

$$P(b) = bP_{in}$$

$$P_{sp} = n_{sp}(G-1)h\nu B_o L_{TWC} L_{AWG}^{N\times N} \tag{6}$$

The variance of total noises for bit b is

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sp-sig}^2 + \sigma_{s-sp}^2 + \sigma_{th}^2 \tag{7}$$

The Bit Error Rate (BER) is evaluated as

$$BER = Q\left(\frac{I(1)-I(0)}{\sigma(1)+\sigma(0)}\right) = Q\left(R\frac{P(1)-P(0)}{\sigma(1)+\sigma(0)}\right) \tag{8}$$

Where Q(.) is error function:

$$Q(z) = \frac{1}{\sqrt{2\pi}} \int_{z}^{\infty} e^{-\frac{z^2}{2}} dz \quad (9)$$

Using the above formulations and parameters value listed in Table 1, the BER vs. power analysis is presented in Table 2. In the optical communication the acceptable limits of BER is $\leq 10^{-9}$ and correspondingly the minimum required amount of power for successful operation of the switch is 2 micro-watts.

Table 2. BER vs. Power for buffered packets.

Power in micro watts	BER
1.0	2.00×10^{-5}
1.5	1.51×10^{-7}
2.0	1.16×10^{-9}
2.5	9.08×10^{-12}
3.0	7.10×10^{-14}
3.5	5.56×10^{-16}
4.0	4.36×10^{-18}
4.5	3.41×10^{-20}
5.0	2.67×10^{-22}

AO-NACK Analysis

In case of AO-NACK the power received at the dedicated receiver on the host side is

$$P_{RX}(b) = bP_{in}L_{TWC}L_{OC}L_{OC}R_{ef}G + n_{sp}(G-1)h\nu B_o L_{OC}L_{OC}R_{ef} \quad (10)$$

$$P_{RX}(b) = bP + P_{sp} \quad (11)$$

Where R_{ef} is power reflectivity of scheduling AWG and gain is given by equation 4 as above. Againthe noises at the receiver are

Shot noise: $\sigma_s^2 = 2qRPB_e$

ASE-ASE beat noise: $\sigma_{sp-sp}^2 = 2R^2P_{sp}(2B_o - B_e)\frac{B_e}{B_0^2}$

Sig-ASE beat noise: $\sigma_{sig-sp}^2 = 4R^2P\frac{P_{sp}B_e}{B_0}$

Shot-ASE beat noise: $\sigma_{s-sp}^2 = 2qRP_{sp}B_e$

Thermal noise: $\sigma_{th}^2 = \frac{4K_BTB_e}{R_L}$ (12)

where$P$ and P_{sp} are given by equation 11 respectively.

The BER can again be evaluated using the eqn. 8. Using the values (Table 1) the obtained BER is zero. Thus, the AO-NACK is received error free at the host side. Therefore, physical layer analysis suggests that the concept of negative acknowledgement can be implemented error free, and due to physical layer impairments negative acknowledgement will never lost, and will always be correctly detected at the receiver at the host side. However, due to network layer congestion negative acknowledgement can be lost, or in case of deflection routing it can be delayed for long time. Therefore, performance of data center switch at network layer is important and performs in next section.

NETWORK LAYER ANALYSIS

The network layer analysis is aim to obtain packet loss analysis of the switch due to the congestion. In this part packet loss probability is obtained under various loading condition while considering switch with and without buffer. To view the applicability of the buffer simple random traffic model is assumed, and can be modelled as output queued system. The Markov chain structure is shown in Fig. 5. The Markov chain analysis is based on birth and death process. Assuming buffer is of size B, therefore in Markov chain, B states are possible, and depending on arrival of packets states are changed. It is also noticeable that in each time slot, for each output only one packet will be delivered to each output.

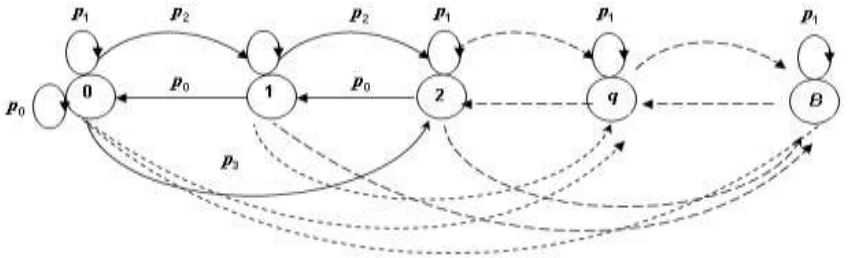

Figure 5. Markov Chain for output queued system.

For traffic generation random traffic model is based on Bernoulli process is considered. This model assumes that in any time slot, with probability *p* packet arrive on an input and with probability *1/N* select any one of the output, where N represents the input/output ports of the switch.

Considering a random variable Ywhich denotes the number of packets arriving for considered output in a given slot as different inputs can generate packet for same output. Probability that particular tagged output has exactly *r* packets in a slot is

$$p_r = \Pr[Y = r] = {}^{N}C_r \left(\frac{p}{N}\right)^r \left(1-\frac{p}{N}\right)^{N-r} \tag{13}$$

The state transition probabilities in Markov chain is given by

$$P_{ab}=Pr[r_a=b|r_{a-1}=a] \tag{14}$$

where '*a*' is previous state and '*b*' is current state, and defined by

$$p_{ab} = \begin{cases} p_0 + p_1 & \text{for } a = 0, b = 0 \\ p_0 & \text{for } 1 \le a \le B, b = a - 1 \\ p_{b-a+1} & \text{for } b - N + 1 \le a \le b - 1,\ 1 \le b \le B - 1 \\ \sum_{m=b-a+1}^{N} p_m & \text{for } b = B,\ 0 \le a \le b \\ 0 & \text{otherwise} \end{cases} \quad (15)$$

$\Psi = [\Psi_0 \Psi_1 \Psi_2 \Psi_3 ---- \Psi_B]$ is the distribution of steady state of the Markov chain is given by

$$\Psi\, p_{ab} = \Psi \quad (16)$$

with vector 'Ψ' satisfying

$$\sum_{a=1}^{B} \psi_a = 1 \quad (17)$$

Considering, ρ as offered loadand normalized throughput as ρ_0, then the probability of packet loss is given by

$$\Pr[\text{Packet loss}] = 1 - \frac{\rho_0}{\rho} \quad (18)$$

Where, $\rho_0 = 1 - \Psi_0 p_0$. (19)

The average buffer utilization is $\overline{B} = \sum_{a=1}^{B} a\psi_a$ (20)

The effect of buffer on packet loss rate is shown in Fig. 6. In the figure B=0 denotes the buffer-less switch.

Similarly, for example B=8, denotes that in case of contention, maximum of 8 packets storage is possible in the buffer for each output port. Here without buffer a large drop in packets can be observed and it is very high at each load. Considering load of '0.2' the probabilistic packet loss is 8.85% which at load of '0.8' it becomes 30%. Similarly, at the load of 0.6 for B=0 the loss rate is 23.75% and for B=4, 8 and 16 the loss rate is 3.35×10^{-3}, 6.06×10^{-5} and 2.01×10^{-8} respectively. Thus, it is evident that buffers have deep impact on the overall packet loss probability and the usefulness of the buffer can't be avoided.

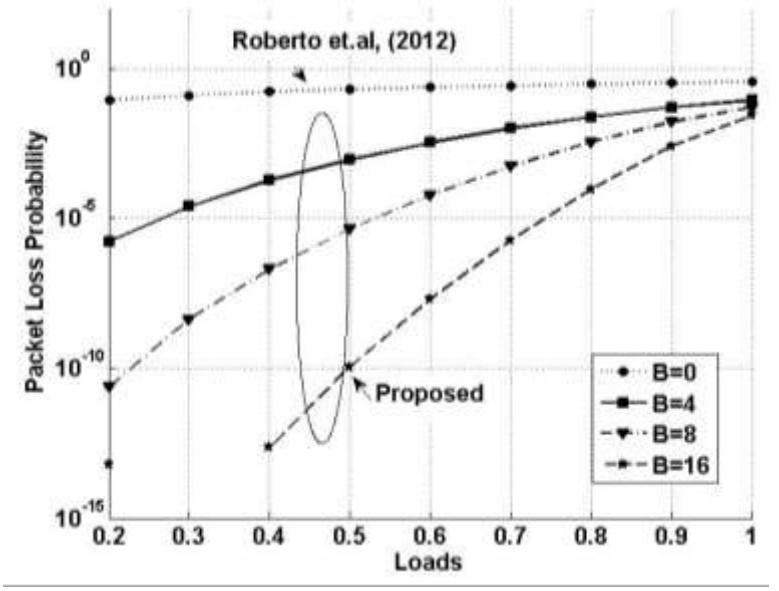

Figure 6. Packet loss probability vs.load under different buffering conditions.

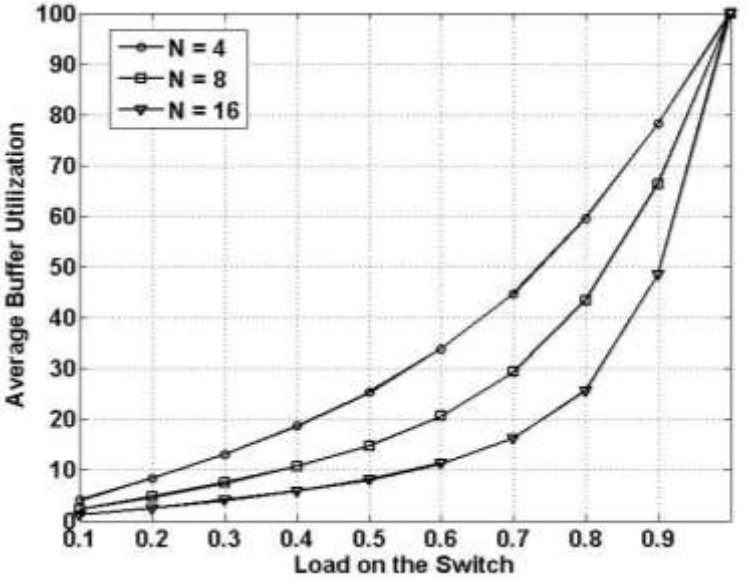

Figure 7. Average buffer utilization vs. load under different switch size.

In Figure 7, average buffer utilization vs. load is shown. In this curve buffer is considered to be equal of buffer size. Here, as the load increases, average buffer utilization decreases. As the size of the switch increases, average buffer utilization at moderate load (0.4-0.8) decreases. In case of N=4, at the load of 0.8, average buffer utilization is 60%, while for N=16, average buffer utilization is less than 20%. By simply multiplying switch size with average buffer utilization i.e., $N\overline{B}$ we can make an estimation of required buffer.

It is clear from the figure that till load of 0.5, 50% of the provided buffer is vacant. Therefore, depending on switch

size and load buffer size can be varied. However, the use of buffer in reducing packet loss rate cannot be avoided. From Fig. 5 and Fig. 6, it is clear that using buffer packet loss rate can be reduced significantly, but size of buffer can be chosen efficiently using buffer utilization.

At a particular load ρ, the total numbers of lost packets are given by

$$N\rho\left(1-\frac{\rho_0}{\rho}\right)S = N(\rho-\rho_0)S \tag{21}$$

where S represents the number of slots of simulation under steady state.

In S slots the numbers of transmitted packets at load ρ are $N\rho S$. Considering that simulation is run for 10^5 slots then at the load 0.8, without buffer 384200 packets will be re-transmitted, this is a huge number and such large number of negative acknowledgement will also introduce some extra delay in re-transmissions.

It can be visualized from the Fig. 8 that as the buffer space for the storage of contending packets increases, the number of AO-NACK send back to host also decreases. Hence, request for re-transmission of packets reduces significantly, and for the buffer space of 8; the number request for re-transmission of packets reduced to 4626. Similarly, for B=16 the request for re-transmission of packets are 117 which is minimal as compared to without any buffering.

Therefore, it is evident that using a small buffer can reduce number of re-transmission of packets significantly. Moreover, in networks when this switch will be placed the traffic due to the re-transmission of packets will be comparatively lesser thus less congestion will be there. This mechanism also reduces the chances of loss of negative acknowledgement.

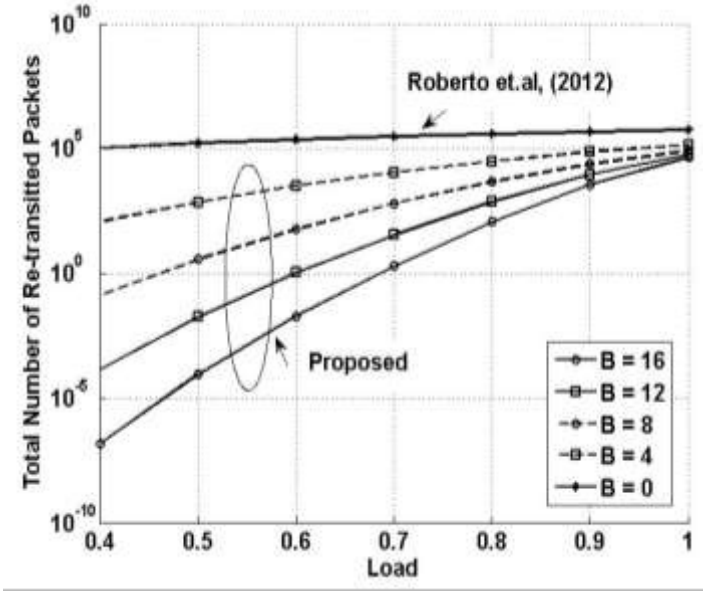

Figure 8. Total number of retransmitted packets vs. load for varying buffer sizes.

CONCLUSIONS

This paper presents an optical interconnect/switch design to resolve contention among packets. The presented design uses optical buffer and AO-NACK to reduce the packet loss to zero, with very few re-transmitted packets. The presented design provides mechanism for fast contention resolution notification and reduces the transmission latency. However, latency will depend on the distance of host form the switch. This design is equally applicable to optical data-center applications for the interconnection of optical racks. Proposed switch can operate efficiently at the power of 2 micro-watts and using buffer the number of transmitted packets can be bring down more than 3000 times in comparison to buffer less design. Finally, it can be concluded that use of buffer can significantly reduce the re-transmission of packets, and moreover also reduces the congestion in the networks due to re-transmission of packets. The proposed mechanism also reduces probability of loss of negative acknowledgement.

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