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Design and analysis of high speed optical routers for next generation data centre network

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ABSTRACT

Advanced optical switching systems are required for connecting next generation high performance data center system. It provides scaling of thousands of ports, and, at the same time, it achieves low communication latency and reduced power consumption. For providing fast optical switching, arrayed waveguide grating (AWG) routers are used in the core of many switches. The AWG is preferred because of its inherent ability to perform wavelength routing of many wavelengths parallelly. In this paper, a physical layer and network layer analysis of two AWG based switches is presented and through this analysis, a comparison is performed between the switches. The simulation results discussed in this paper clearly reveal that the design of our proposed switch is far better than the recently published design. Moreover, our proposed switch is comparatively more cost effective.

Keywords: AWG, BER, Cost Analysis, SOA, Tunable wavelength convertor.

INTRODUCTION

The rise of cloud computing and other emerging web applications has created the need for more powerful warehouse-scale data centers. These data centers comprise hundreds of thousands of servers that need to communicate with each other via high performance and low latency interconnection networks (Kacheris C, 2013). With the rapid growth in Internet applications, data centers have witnessed demands for more and more storage, computation power, and communication bandwidth. In the present day's telecommunication environment, hundreds of thousands of servers are very common in heavy data center systems. In the recent survey report given by Cisco (Cisco Global Cloud, 2011), the yearly worldwide data center traffic is expected to reach several zetta bytes by the end of 2017. The data traffic, which is generated between the data centers and within the data center, is expected to grow extensively. This increase in the traffic generates the need of high performance network technologies and architectures for intra- and inter data center networks. In the present electrical data center network, the major challenge in the design of the data center is the power consumption of the infrastructure mainly due to the associated operational expenditure (OPEX) costs. According to relevant studies, data center networks consume around 10–20 percent of the total IT power consumption of data center sites, and this is expected to increase soon in the near future (Kacheris C, 2013). In optical networks, the bandwidth is utilized effectively, power consumption is very low, cabling complications are very small, and they provide high reliability. These features, discussed above, make optical networks the best available solution for the challenges faced by data center networks. An optical packet switched network has many advantages in comparison to the electronic switched network, but the unavailability of optical RAM is a major challenge in the design of optical switches (Bowers J.,

2006). The best available option for optical storage is the use of fiber delay lines. In FDL lines, packets can be stored in optical domain. If a comparison is performed between electronic and optical storage, then through electronic RAM millions of packets can be stored for longer duration while in FDL lines only hundreds of packets can be stored for very small period (Burmeister E. F., 2007). So, a competent optical switch design is required for low loss structure. In the similar context, a dual loop based optical buffer system was proposed and experimentally demonstrated, where longer delay of the order of some micro-seconds is possible (Tian C. Y., 2008). These designs develop a new optical buffer, which is compact in nature, is easy to read and write, and can be cascaded. In cascaded dual loop buffer, delay time can be dynamically configured in a broad range of 1999- times of the basic unit, and 240ns delay resolution can be obtained (Wang Y., 2009). However, the above designs study is performed for only two wavelengths. In case of WDM signals, scalability of the design can be a major issue.

In this paper, three AWG based optical packet switch designs are presented. In each design, fiber delay lines are used for storing the packets in the optical domain. The first design (A0) presented in figure 1 is a recirculating loop buffer based switch. The other design (A1) presented in figure 2 is an optical packet switch design proposed by the authors of the paper. The third design (A2) presented in figure 3 is another AWG based switch, which is a simplified version of the architecture A0. The detailed descriptions of these three architectures are presented in further subsections of this paper. In this paper, a detailed comparative analysis between two switches, A1 and A2, is performed, and obtained results clearly show that the performance of our proposed switch is much better than the other one in terms of loss, cost, scalability, and crosstalk domain.

The rest part of the paper is organized as follows. In section II, the detailed description of each switch is presented; in section III, a comparative analysis is performed by various parameters; finally, in section IV, the major conclusions of the whole paper are discussed.

WAVELENGTH DIVISION MULTIPLEXING SHARED BUFFER ROUTER

Despite the recent advances in optical technology, the greatest challenge in the realization of optical routers is the lack of a mature solution for buffering optical signals. Fiber delay lines (FDLs) have been proposed to emulate electronic buffering by delaying contending optical packets for a fixed amount of time (Shukla, V., 2016; Rastegarfar, H., 2014). In this paper, three AWG based optical packet switch architectures are presented; each switch uses fiber delay lines for the buffering of contending packets. The first architecture is proposed by Q. Xu (2012) as shown in Figure 1. In this architecture, recirculating FDLs are used for storing the contending packets. Here the buffer is made recirculating, which allows longer duration storage. As represented in Figure 1, it is possible to provide TWCs along FDLs to enable multiple recirculation for contending packets. Imagine a case where the FDLs are empty while three packets contending for the same output port arrive at the switch; then one of these packets is directed to the desired output with no queueing delay. However, the other two losing packets need to be buffered to resolve contention. In the next time slot, one of two buffered packets that have already appeared at the head of their corresponding FDL will be guided toward the destination port by properly tuning the TWC along the fiber delay line. The other packet needs to be delayed for one more time slot to prevent collision. The TWC along the packet will be configured such that the packet is once again mapped to a recirculation

fiber. Eventually, in the next time slot, this recirculating packet leaves the switch without being dropped. In this switch design, in a single time slot only one packet is stored in each module so the main advantage of WDM is lost.

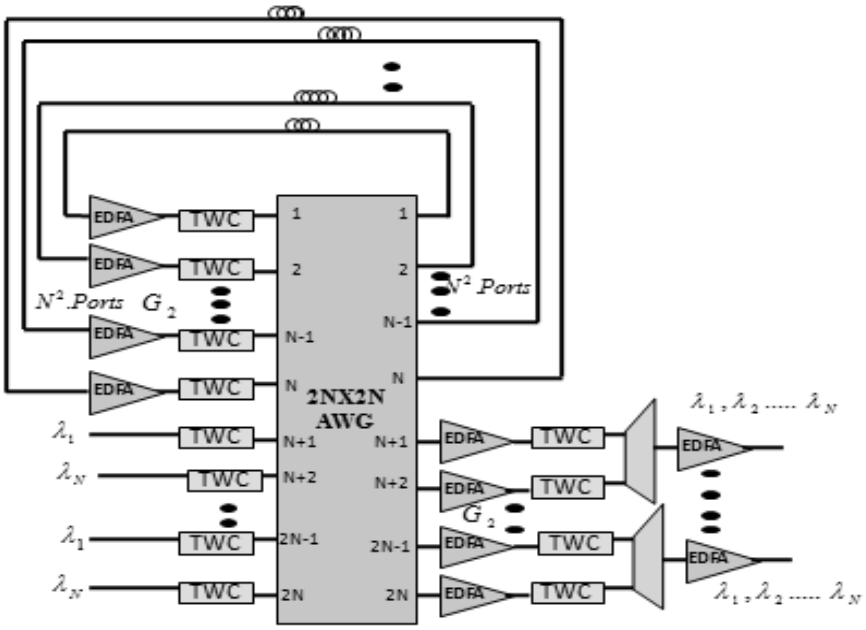

Figure 1. AWG based optical packet switch router (A0) (Xu Q., 2012).

Figure 2 shows another optical packet switch proposed by V. Shukla (Shukla V., 2016; Shukla V., 2014; Srivastava, R., 2010), which is very simple in design; the whole switch is divided into two units, which are scheduling and switching units. The scheduling section contains a set of TWCs that are used to convert the wavelength of incoming packets as per the routing pattern of first AWG router.

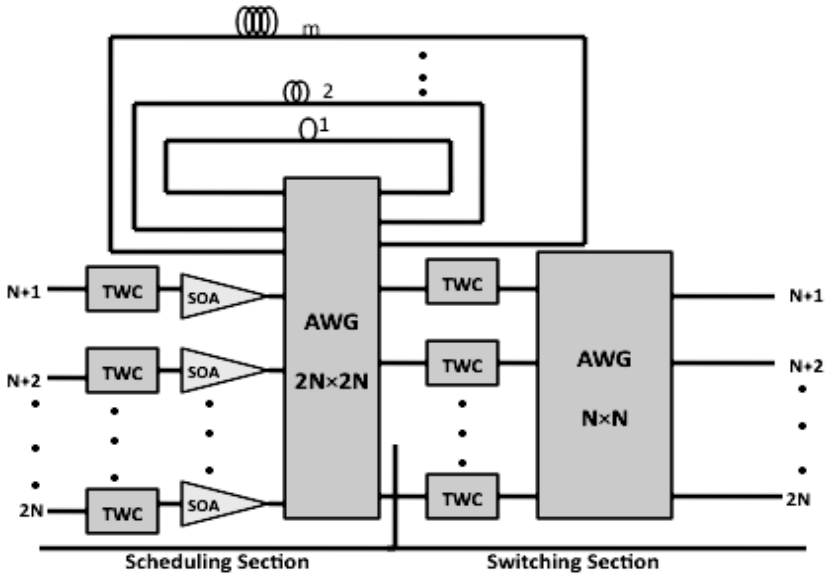

Figure 2. AWG based optical switch (A1) (Shukla V., 2016).

The upper N ports of scheduling AWG are connected with the fiber delay lines, and the lower N ports are connected with appropriate output ports. Here the wavelength division multiplexing is used to store the packets in the buffer that makes the utilization of buffer more effective. In each buffer module, we can store N packets, one on each N wavelength, with only one packet being stored for a particular output port. This packet can be stored on any of the free wavelengths. Thus, at most N packets can be stored in all the modules for a particular output port. Thus, the length of the queue for each output port will be decided by the number of modules with maximum values of N packets. The TWCs at the input of the switch are tuned in each time slot either to place a packet in the corresponding loop buffer module or to direct them for the appropriate output port.

In this paper, the authors performed a comparison between two switches; the first switch is the authors' proposed switch (A1) and the other switch is the simplified version of switch A0. For making the comparison fair, omit the components just before and after TWC of the architecture A0; after doing this, the design of simplified switch (A2) is shown in Figure 3. The results presented in this paper show that the performance of the switch is poor in terms of packet loss, cost, scalability, and crosstalk value.

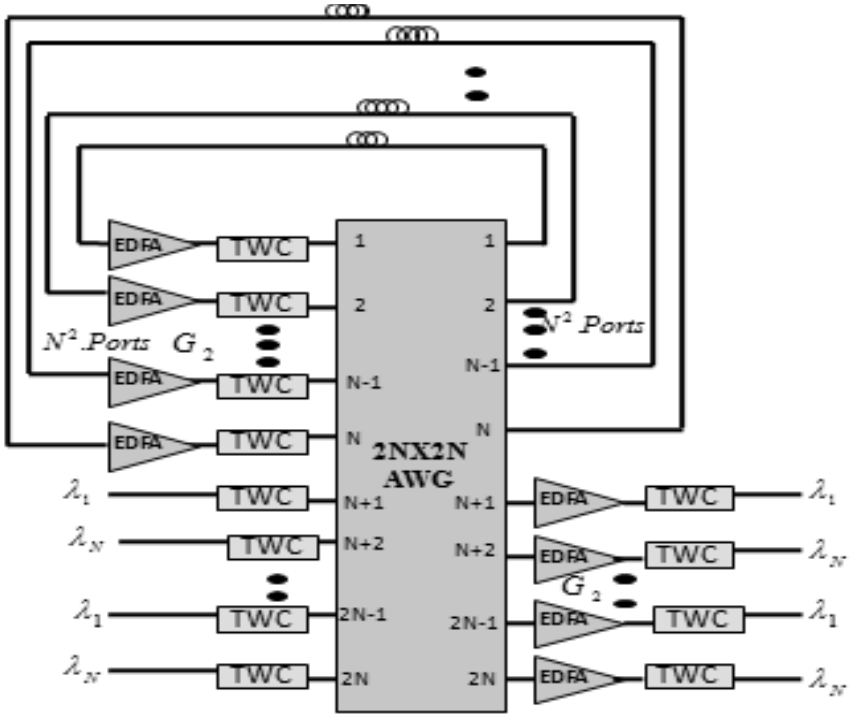

Figure 3. Simplified version of AWG based switch (A2).

1. In the architecture presented in Figure 3, the buffer is made recirculating in nature, and in a single time slot only one packet is stored in each module, so the main advantage of WDM is lost.
2. In the switch presented in Figure 3, we can store a maximum of N packets in the buffer, while in the switch described in Figure 2, a maximum of N2 packets can be stored.
3. The main advantage of recirculating buffer (Figure 3) is that it allows packet priority routing since a lower-priority packet can be preempted by being sent to another loop. This feature is important to provide quality of service in optical networks.

COMPARATIVE STUDY

In this section, a comparative study is performed between the author's proposed switch (A1) and a recently published optical switch (A2). The comparisons between these two switches are performed in terms of loss, cost, power, scalability, and crosstalk parameters. Table 1 shows the description of symbols, which are used in the analysis and in Tables 2 and 3; the list of parameters used in the calculations and their values are defined.

Table 1. Symbols and their descriptions used in the analysis (Shukla V., 2016).

Symbol	***Description***
A_{in}	Input loss
A_b	Buffer loss
A_{out}	Output loss
h	Plank constant
b	Bit
q	Electronic charge
K	Circulations
P_{in}	Power at input
P_{out}	Power at output
P_S	Power enters in to buffer module
K_B	Boltzmann constant
C_{TWC}	TWC cost
C_{FDL}	FDL cost
C_{SOA}	SOA cost
C_{AWG}	AWG cost
ν	Frequency

Table 2. Symbols, parameters, and their values used in the analysis (Srivastava, R. 2007).

Symbol	**Parameter**	**Value**
N	Switch size	4,8
η_{sp}	Population inversion factor	1.2
G_i	Amplifier gain	20 dB
C	Speed of light	$3\times10^8 m/s$
R	Responsivity	1.28 A/W
e	Electric charge	$1.6\times10^{-19} C$
R_L	Load resistance	300Ω
T	Temperature	270 C
B_e	Electrical bandwidth	20GHz
B_o	Optical bandwidth	40GHz
L_{TWC}	TWC insertion loss	2.0 dB
$L_{AWG}^{2N\times2N}$	Loss of scheduling AWG	3.0 dB
$L_{AWG}^{N\times N}$	Loss of switching AWG	3.0 dB
L_{FDL}	Loss of the fiber loop	0.2 dB/km

Table 3. AWG routers description.

Number of channels	40
Channel spacing	100 Ghz
Operating wavelengths	ITU Grid
Insertion loss	3.0 dB
Adjacent channel crosstalk (χ	-25 dB

3.1. Controlling points

The control complexity of switch A1 is very simple in comparison to switch A2. In switch A1, the control points are present only at the input and output ports of the scheduling AWG router. In switch A2, the control points are present at the input, at the output, and in the buffer units so heavy controlling is required at all three places. The major advantage of switch A1 is that no type of controlling is required inside the buffer; this makes the buffer simple in nature. In this design, by using WDM feature, number of packets can be stored in a single piece of fiber (Srivastava, R., 2010).

3.2. Analysis of switches A1 and A2 in terms of loss and power

Equation (1) shows the total power received at the output of switch A2. Here the whole equation is divided into two parts: in the first part, the power entering the loop buffer for bit "*b*" is calculated equal to $bP_{in}A_{in}$, while in the second part, the signal power for the K^{th} buffer unit is calculated equal to $n_{sp}(G_2-1)h\nu B_o\sum_{i=1}^{K}\left(A_bG_2\right)^i + n_{sp}(G_2-1)h\nu B_o$. Here $n_{sp}(G_2-1)h\nu B_o$ is the amplified spontaneous emission (ASE) noise of EDFA. Now finally the total power is received at the output of switch

$$P_{out} = bP_{in}A_{in} + n_{sp}(G_2-1)h\nu B_o\sum_{i=1}^{K}\left(A_bG_2\right)^i + n_{sp}(G_2-1)h\nu B_o \tag{1}$$

where

$$A_{in} = L_{TWC}L_{AWG} \tag{2}$$

$$A_b = L_{EDFA}L_{TWC}L_{AWG} \tag{3}$$

$$A_{out} = L_{TWC}L_{EDFA} \qquad P_{out} = bP_{in} + n_{sp}(G-1)h\nu B_o L_{TWC}L_{AWG}^{2N\times 2N}L_{AWG}^{N\times N} \tag{4}$$

For bits '0' and '1' the value of b is chosen as 0 and 1, respectively.

The parameters used in the above equations (1)–(4) and their values are described in Table 1 and Table 2.

The EDFA is used for compensating the loss of the buffer and output unit, that is, $A_bG_2 = 1$ and $A_{out}G_2 = 1$; then

$$P_{out} = P_{in}A_{in} + n_{sp}(G_2-1)h\nu B_o(K+1) \tag{5}$$

Using the above techniques used in eq. (1) and (5), the total power at the output of switch A1 is given by

$$P_{out} = bP_{in} + n_{sp}(G-1)h\nu B_o L_{TWC} L_{AWG}^{2N\times 2N} L_{AWG}^{N\times N} \tag{6}$$

3.3. Noise analysis

The various noise components at the receiver, for bit "*b*," are presented in eq. (7)–(11):

Shot noise:

$$\sigma_s^2 = 2qRPB_e \tag{7}$$

ASE-ASE beat noise:

$$\sigma_{sp-sp}^2 = 2R^2 P_{sp}(2B_o - B_e)\frac{B_e}{B_0^2} \tag{8}$$

Sig-ASE beat noise:

$$\sigma_{sig-sp}^2 = 4R^2 P\frac{P_{sp}B_e}{B_0} \tag{9}$$

Shot-ASE beat noise:

$$\sigma_{s-sp}^2 = 2qRP_{sp}B_e \tag{10}$$

Thermal noise:

$$\sigma_{th}^2 = \frac{4K_B TB_e}{R_L} \tag{11}$$

The calculated noise variance for single bit b is represented as follows:

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sp-sig}^2 + \sigma_{s-sp}^2 + \sigma_{th}^2 \tag{12}$$

$$BER = Q\left(\frac{I(1)-I(0)}{\sigma(1)+\sigma(0)}\right) = Q\left(\frac{R(P_1-P_0)}{\sigma(1)+\sigma(0)}\right)$$
$$Q(z) = \frac{1}{\sqrt{2\pi}}\int_z^{\infty} e^{-\frac{z^2}{2}}dz \tag{13}$$

In equation (13), the value of I (1) and I (0) is considered as I(1) =*RP*(1) and I(0) = *RP*(0), and is considered as the photocurrent received by a receiver for bit 1 and bit 0, respectively, and the responsivity of the receiver is represented by *R*.

Regarding the noise expression represented in the above equations (7)–(12), the *P* and *Psp* are represented as the signal and noise power, respectively.

Similarly, in the case of architecture A2, signal and noise power are represented as follows:

$$P = bP_{in}A_{in} \tag{14}$$

$$P_{sp} = n_{sp}(G_2 - 1)h\nu B_o \sum_{i=1}^{K} \left(A_b G_2\right)^i + n_{sp}(G_2 - 1)h\nu B_o$$

The calculated signal and noise power for architecture A1 are represented as follows:

$$P = bP_{in} \tag{15}$$

$$P_{Sp} = n_{sp}(G - 1)h\nu B_o L_{TWC} L_{AWG}^{2N\times 2N} L_{AWG}^{N\times N}$$

3.4. Calculations

Based on the above analysis and by using the values of different parameters from tables 1, 2, and 3, the BER analysis of each switch is presented in Tables 4 and 5 when the packet passes through the buffer unit.

Table 4. BER of switch A1 at different power levels.

Power in nW	BER
100	0.0011
200	1.53×10^{-6}
300	6.48×10^{-11}
400	2.18×10^{-12}
500	2.32×10^{-15}
600	2.43×10^{-18}
700	2.56×10^{-21}
800	2.48×10^{-24}
900	2.43×10^{-27}
1000	2.30×10^{-30}

Table 5. BER of switch A2 at different power levels.

Power in μW	BER
5	3.79×10^{-6}
6	4.14×10^{-7}
7	4.57×10^{-8}
8	5.08×10^{-9}
9	5.68×10^{-10}
10	6.39×10^{-11}
11	7.21×10^{-12}
12	8.16×10^{-13}
13	9.25×10^{-14}
14	1.05×10^{-14}

In Tables 4 and 5, the BER analysis of each switch is presented when the packet passes through the buffer unit, as we know that the acceptable range of BER in optical communication is 10^{-9} for proper operation of switch, and from the results represented in the tables, the minimum power required for the correct operation of switch A1 is 300 nW, while the power required for correct operation of switch A2 is of 9μW. So, the power requirement of switch A1 is very low in comparison to switch A2, where μW power levels are required.

3.5. Cost analysis

In this section, the cost analysis of each switch is presented. The cost is also a crucial factor in the selection of switch, because the cost of optical components is too high. The tunability of TWC is a major issue as AWG is a wavelength routing device. However, due to the reuse of wavelengths in AWG, the tunability of TWC is *N* wavelength for an *N*×*N* AWG. According to the past literature, the cost of TWC is considered as $C=aW^b$, where "*a*" and "*b*" are used as normalization constants and *W* is the total number of tunable wavelengths. The value of "*b*" is chosen from the range between .5 and 5, and, for sake of convenience, the value of "*a*" is considered as 1 (Shukla, V. 2015). So, by this discussion, if the size of AWG increases, more tunability is required for TWC and the overall cost of switch increases exponentially. The cost of switches A1 and A2 is presented by eq. (16) and (17).

$$C_T^{A_1} = NC_{TWC}^{Sc} + NC_{SOA} + C_{AWG}^{2N\times 2N} + NC_{FDL} + NC_{TWC}^{Sw} + C_{AWG}^{N\times N} \tag{16}$$

$$C_T^{A_2} = NC_{TWC}^{Sc} + C_{AWG}^{2N\times 2N} + NC_{EDFA}^{b} + NC_{FDL} + NC_{TWC}^{b} + NC_{EDFA} + NC_{TWC} \tag{17}$$

In this cost analysis, the Fiber to Chip Coupling (FCC) (Caenegem, R. V., 2006) model is used and the cost figures of each component are represented in Table 7.

Table 6. Cost of optical components.

Components	Value
SOA	2
EDFA	2
AWG(2N×2N)	4*N*
FDL	1
TWC	aW^b

Finally, the cost of each switch is represented by

$$\begin{aligned} C_T^{A_1} &= Na(2N)^b + 2N + 4N + N + Na(N)^b + 2N \\ &= Na\left[(2N)^b + (N)^b\right] + 9N \end{aligned} \tag{18}$$

$$\begin{aligned} C_T^{A_2} &= Na(2N)^b + 4N + 2N + N + Na(N+1)^b + 2N + Na(N)^b \\ &= Na\left[(2N)^b + (N+1)^b + (N)^b\right] + 9N \end{aligned} \tag{19}$$

In Figure 4, the cost comparison between switches A1 and A2 is presented by the FCC model. In the final calculation, the value of "a" is considered as 1, while the value of "b" varies between .5 and 5. So, from the bar chart shown in Figure 4, the cost of design A1 is less than A2.

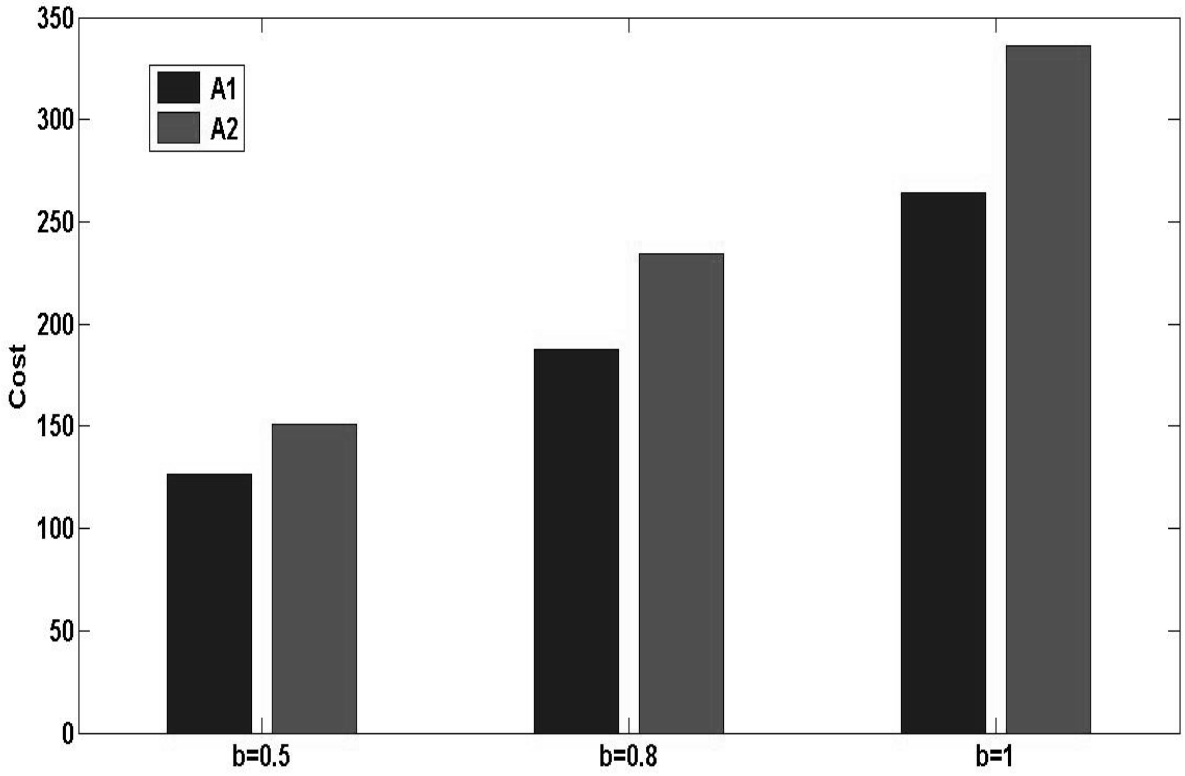

Figure 4. Cost of switches A1 and A2 by the FCC model.

3.6. Scalability analysis

Since each of the switches presented in Figures 2 and 3 uses nearly the same type of components, so a fair comparison is possible between both switches. Table 6 shows the components count for realization of each switch, and it is clear from the Table that design A2 uses more components in comparison to A1. Since the increase in components means more cost and more loss of the switch, the performance of switch A1 is more effective in comparison to A2.

Table 7. Scalability analysis of switches A1 and A2.

Components	Switch A1 (Proposed)	Switch A2(Q. Xu)
Tunable wavelength convertors (TWC)	2N	3N
Amplifiers (SOA and EDFA)	N	2N
Arrayed waveguide grating router (AWG)	2	1
Fiber delay lines (FDL)	N	N

3.7. Number of circulations in the buffer of switch A2

The architecture represented in Figure 3 is the recirculating loop buffer based switch. In the design, if a situation of contention among the incoming packets arises, except one, other contending

packets are forwarded to the loop buffer; after one circulation if the situation of contention still exists, then buffered packets are again directed towards the buffer. This process continues until the contention among packets is resolved. Table 8 shows the minimum power required for the packet circulation in the buffer. The obtained results show that more circulation means that more power is required for correct operation of switch.

Table 8. Packet circulation at various power levels.

Power in μW	Circulations
5	9
6	11
7	13
8	15
9	17
10	19
11	21
12	23
13	25
14	27
15	29
16	31
17	33
18	35
19	37
20	39

3.8. Crosstalk analysis of switch

Nearly all components in the optical communication system introduce crosstalk. This crosstalk is an undesirable effect and should be as low as possible (Srivastava, R., 2008; Pallavi, S., 2015). The crosstalk factor, which is generated through optical component, degrades the system performance. Here, in this paper, both switches are AWG based switches. The AWG introduces crosstalk factor, which degrades the overall performance of each switch. In this section, the detailed crosstalk analysis of each switch is presented when the packet passes through the loop buffer. In the switch, each time the packet passes through the buffer, it passes through the AWG, and the AWG introduces the crosstalk factor.

The crosstalk of switch A1 when the packet passes through the buffer is represented by

$$P_{out} = \left[P_{in} L_{TWC} L_{SOA} G L_{AWG}^{Sc} + P_{\chi} \right] L_{AWG}^{Sc} + P_{\chi} \left] L_{TWC} L_{AWG}^{SW} + P_{\chi} + n_{sp}(G-1)h\nu B_0 L_{AWG}^{Sc} L_{TWC} L_{AWG}^{SW} \right. \quad (20)$$

where P_{χ} represents the crosstalk power of the AWG.

Table 9. The value of BER for switch A1 when the packet passes through buffer.

Power in nW	BER
100	0.0037
200	8.93×10^{-6}
300	1.44×10^{-10}
400	7.76×10^{-12}
500	6.18×10^{-15}

The crosstalk of switch A2 when the packet passes through the buffer is represented by

$$P_{out} = \left[P_{in}L_{TWC}L_{AWG} + P_{\chi}^{1}\right]L_{EDFA}L_{TWC}L_{AWG}G_2 + P_{\chi}^{2}\Big]L_{EDFA}L_{TWC}L_{AWG}G_2 + P_{\chi}^{3}\Big].....L_{EDFA}L_{TWC}L_{AWG}G_2 + P_{\chi}^{K-1}\Big]L_{AWG} + P_{\chi}^{K}L_{EDFA}L_{TWC}G_2 + n_{sp}(G_2-1)h\nu B_o(K+1) \quad (21)$$

Since we know that

$$L_{EDFA}L_{TWC}L_{AWG}G_2 = 1 \quad (22)$$

after inserting the value of eq. (22) in eq. (21), equation (23) is derived for switch A2

$$P_{out} = [P_{in}L_{TWC}L_{AWG} + P_{\chi}^{1} + P_{\chi}^{2} + P_{\chi}^{3}... + P_{\chi}^{K-1}]L_{AWG} + P_{\chi}^{K}L_{EDFA}L_{TWC}G_2 + n_{sp}(G_2-1)h\nu B_o(K+1)$$

$$P_{out} = [P_{in}L_{TWC}L_{AWG} + (K-1)P_{\chi}]L_{AWG} + P_{\chi}^{K}L_{EDFA}L_{TWC}G_2 + n_{sp}(G_2-1)h\nu B_o(K+1) \quad (23)$$

$$P_{out} = P_{in}[L_{TWC}L_{AWG}L_{AWG} + (K-1)\chi L_{AWG} + \chi L_{EDFA}L_{TWC}G_2] + + n_{sp}(G_2-1)h\nu B_o(K+1)$$

Table 10. Maximum circulation count at various power levels when the packet passes through the buffer.

Power in μW	Circulations
5	7
6	9
7	12
8	14
9	16
10	17

3.9. Results discussion

Switch A2 discussed above is a recirculating buffer-based switch, in which the only single packet is stored in each piece of fiber, while switch A1 is a WDM switch, in which N packets can be stored in a piece of fiber. Switch A2 stores a maximum of N packets in the buffer, while, on the other hand, switch A1 stores up to N^2 packets in the buffer.

Let us consider a switch of size 32×32. Now, in this case, the upper 16 ports of the switch are connected with the buffer modules, while the other 16 ports are used as actual input/output ports of the switch. Consider the case when 16 packets have to be stored in the buffer at a time; then from Table 9, the maximum power required for the correct operation of switch A1 is 300 nW, while from Table 10, for performing the same operation in switch A2, a power of 9μW is required. The obtained results clearly show that the performance of switch A1 is much better in terms of power requirements for a correct operation of the switch.

In this section, the crosstalk analysis of each switch is discussed. Let the size of switch be a multiple of 2. Therefore, for a switch of 40 ports, 32 ports are used, while 8 ports are unused. In these 32 ports, the lower 16 ports work as actual I/O ports, while other 16 are used as the buffer modules. From Table 8, a power level of 300 nW is required for the correct operation of switch A1. In the presence of crosstalk of the AWG, the maximum data storage is not affected. Hence, the crosstalk of AWG will not cause any problem.

In switch A2, the buffer is made recirculating in nature; that is why in each recirculation, the packet passes through the AWG router, and the AWG introduces the crosstalk factor. And, as we have discussed, the crosstalk is an undesirable feature introduced by AWG, so a maximum recirculation means a maximum crosstalk value, and this degrades the overall performance of switch A2. So the recirculating buffer is not a better option in the design of switch. The design strategies followed by switch A1 are much better in comparison to A2.

Table 11. Comparison between switches under different functionalities.

Functionality	Architecture (A1)	Architecture (A2)
Loss	Low	High
Power	Low	High
Control points	Low	High
Cost	Low	High
Crosstalk	Low	High
Buffer storage	High	Low
Storage duration	Low	High

Table 11 shows comparative studies of the two switches under different functionalities, and, from the table, the design of switch A1 is more advantageous in comparison to switch A2.

CONCLUSION

In this paper, an AWG based optical packet switch architecture is discussed. The considered switch uses WDM technology through which multiple packets can be stored in a single piece of fiber. The considered architecture is compared with the recently published switch design. Through the analysis of each switch, the following have been found.

1. The power required for the correct operation of switch A1 is 300 nW, while in switch A2, the power requirement is 9μW, so the performance of switch A1 is much better in terms of power requirement.

2. Each of the switches presented in the paper uses nearly the same type of components. The requirements of optical components are high in switch A2 as compared to switch A1.

3. As the cost of the optical components is too high, a detailed cost analysis of each switch is presented in the paper and the obtained results show that at "*a=1*" and "*b=1*," the cost of switch A1 is 2,632 units, while the cost of switch A2 is 3,280 units, so the design of switch A1 is more cost effective.

4. The crosstalk analysis of each switch is presented in the paper; the buffer in architecture A2 is a recirculating buffer and each time the packet is circulated in the buffer, it passes through the AWG, so each time the packet passes through the AWG, an undesired factor crosstalk is added and this degrades the performance of switch A2.

In this paper, a fair comparison is performed between the two switches, and the obtained results clearly reveal that the performance of switch A1 is far better than that of switch A2. So, switch A1 is the best available option for the existing data center applications.

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تصميم وتحليل أجهزة توجيه الشبكة الضوئية عالية السرعة لشبكة مركز بيانات الجيل القادم

فايبهاف شوكلا و أرونا جاين

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الخـلاصـة

إن أنظمة الابتدال الضوئي المتقدمة مطلوبة لربط الجيل القادم بنظام مركز بيانات عالي الأداء. حيث أنها توفر الآلاف من منافذ التوصيل، وفي نفس الوقت، تحقق سرعة في الاستجابة للاتصالات وتقلل من استهلاك الطاقة. ولتقديم ابتدال ضوئي سريع ، يتم استخدام أجهزة توجيه ذات شبكة دليل موجي منظم (AWG) في قلب العديد من المبدلات. ويفضل استخدام AWG بسبب قدرته المتأصلة على توجيه طول موجي من العديد من الأطوال الموجية بشكل متوازي. في هذا البحث، تم عرض تحليل طبقة التوصيلات وطبقة الشبكة لاثنين من المبدلات التي ترتكز على AWG، ومن خلال هذا التحليل تم إجراء مقارنة بين المبدلات. وتُظهر نتائج المحاكاة التي نوقشت بوضوح في هذا البحث أن تصميم المبدل المُقترح أفضل بكثير وأقل تكلفة من التصميم المُعلن عنه حالياً.