The LLCLC resonant converter based pseudo-DC link inverter

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ABSTRACT

Technological advancements in solar power systems necessitate highly reliable power inverters with high efficiency and small size. An LLC resonant converter-based pseudo-Direct Current (DC) link inverters offer these qualities to some extent. The resonant circuits of conventional pseudo-DC link inverters cannot attain a zero gain and cannot handle variable frequency control which in turn requires very large filters to produce pure sinusoidal output voltages for the grid. The usage of these filters consequences in the enhanced price and size of inverters; moreover, the reliability of inverters is also reduced. We propose a novel topology for a pseudo-DC link inverter based on an LLCLC resonant converter. The proposed inverter does not require large filters, because it generates rectified sinusoidal output voltages. An additional parallel LC component is added in series to the resonant circuit, which makes it able to attain a zero gain through an infinite circuit impedance. The 400 W pseudo-DC link inverter with a 40 V input and a 400 V output is designed and simulated on OrCAD PSpice software. The results showed that there is a significant improvement in achieving a zero gain. The possible lowest gain achieved is approximately 0.125. The proposed technique claimed to be more efficient than those formerly used, subsequently contributing to satisfying outcomes.

Keywords: LLC; LLCLC; Multi-elements; Micro-inverter; Pseudo DC link inverter; Variable frequency control.

INTRODUCTION

The depletion of fossil fuels triggered solar panels to become popular in producing electrical energy for years (N. Abas et al., 2015). These power plants have several advantages being easy to use, less overall cost, and environment-friendly operation (F. M. Guangul et al., 2019). Micro-inverters are an excellent choice for these systems as there is only one solar panel connected to each inverter which can provide benefits such as less installment space, no mismatch losses, and failure of one panel or inverter does not affect whole plant performance (S. Narendiran, 2013).

Solar power plants provide a very low voltage (40V approximately) which needs to be increased 5 to 10 times for home appliances. The key design considerations for solar micro-inverters are small size, high efficiency, and reliability. The three main types of micro-inverters include those without any DC link, with a DC link, and with a pseudo-DC link (Y. Xue et al., 2004). The basic block diagram of the Pseudo-DC link inverter is given in Figure 1. The inverter consists of two stages i.e. DC-DC stage and the DC-AC stage. The DC-DC stage provides buck-boost operation and converters convert input DC voltage to rectified AC voltage which is then unfolded in the DC-AC stage. Pseudo-DC link inverters are promising because their secondary side only unfolds the rectified sinusoidal voltage (Q. Li et al., 2008). So, a suitable DC-DC stage can provide all the required qualities.
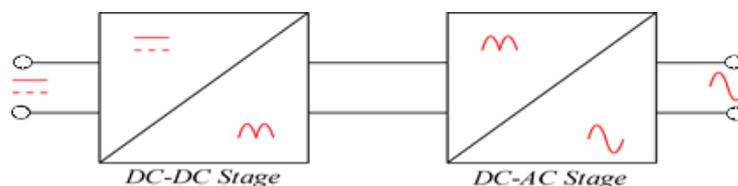
Figure 1. Block diagram of pseudo-DC link inverter.

In the literature, a large number of DC-DC converters for the DC-DC stage are presented. The reliability and high efficiency of an inverter can be achieved through soft switching techniques. Pulse width modulation-based flyback inverters have very small sizes because of fewer switching components but their hard switching operations decrease the overall

efficiency. The hard switching can be reduced by using auxiliary switches, but it complicates the control process and decreases the low switching component advantages (L. mol K Johny et al., 2013). The inverters comprise of resonant converters provide excellent efficiency because of soft switching operations (S. Pervaiz et al., 2013). Their high-frequency operations also reduce the size of energy-storing components which is a key factor for having a smaller size.

The LLC resonant converter-based inverters working on pulse density modulation produce pure sinusoidal output, but large output filters further reduce the reliability and create size issues (Y. Zhao et al., 2015). Inverters with a hybrid control method can provide pure sinusoidal output without any extra-large filter but their control technique itself is very complicated (C. Yeh et al., 2020). The main reason for adopting hybrid control is that LLC resonant converters require a very high switching frequency to achieve zero tank gain which is practically not possible (M. Xingkui et al., 2016). Because of this drawback, inverters based on resonant DC-DC converters do not work completely on variable frequency control.

The LCLC or other four-element resonant converters provide two peak gain values in voltage gain characteristics but achieving zero gain is still not possible (R. Lin et al., 2018). On the other hand, LLCLC resonant converters can achieve approximately zero gain at an achievable switching frequency (R. Mazgut et al., 2016 & J. Koscelnik et al., 2020). These converters consist of LLC resonant components with additional parallel LC components in series on the primary side. The additional components can also be added in series on the secondary side of the converter (H. Wu et al., 2016). The addition of the LC component provides a zero-gain property that can be used in the DC-DC stage of the converters to deliver complete variable frequency control without using a large filter on the output side.

In this paper, a novel LLCLC resonant converter based Pseudo-DC link inverter is proposed. The paper is organized in such a way that after the introduction, the proposed topology of an inverter is presented followed by its analysis and operation. The design consideration is

described next. In the end, the simulation results are discussed, and the conclusion is drawn.

PROPOSED TOPOLOGY

The circuit topology of the proposed inverter is given in Figure 2. The inverter consists of two stages i.e., DC-DC stage and the DC-AC stage. The DC-DC stage consists of a full bridge inverter having four semiconductor switches (S_1 to S_4). The full bridge converts input DC voltage to square wave voltage which is fed to LLCLC resonant tank whose gain changes by input square wave frequency variation. The tank is connected to a high-frequency transformer which can be used for buck-boost operation and isolation purposes. The transformer is further connected to a full wave rectifier for rectification of transformer output. Another full bridge inverter consisting of four switches (S_5 to S_8) is used in the DC-AC stage. This stage unfolds the input rectified voltage to the sinusoidal output voltage. The DC-DC stage of the inverter is operated at a variable frequency to produce rectified sinusoidal voltage at the DC link stage while the DC-AC stage is operated at a constant frequency to unfold rectified sinusoidal voltage.
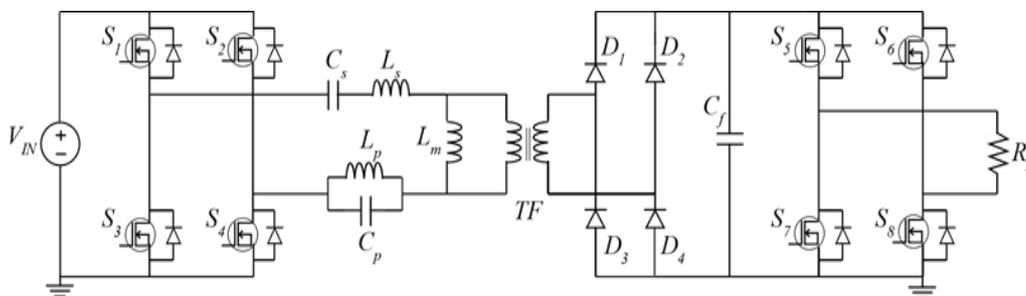

Figure 2. Proposed pseudo-DC link inverter.

LLCLC Resonant Tank Analysis

The resonant tank circuit of the proposed inverter consists of five elements i.e., C_S, C_P, L_S, L_P, and L_m. C_S and L_S are series resonant components while C_P and L_P are parallel resonant components. L_m provides magnetizing inductance for the transformer. The addition of C_P and L_P changes the gain characteristics of the resonant tank helping to achieve zero gain. The gain values for the tank at different Q points are shown in Figure 3. The resonant tank has three main resonant frequencies i.e., f_{R1}, f_{R2}, and f_{R3}. At resonant frequency f_{R1}, the resonant

circuit has a gain value equal to one. Below f_{R1}, the operation of the LLCLC resonant tank is the same as the conventional LLC resonant tank. The gain is always more than one for the converter to have a boost operation. The converter has a buck operation between resonant frequency f_{R1} and f_{R2} because the gain is always less than one in this region. At resonant frequency f_{R2}, the impedance of the resonant tank increases to infinity providing zero gain. At resonant frequency f_{R3}, the gain of the converter is again one and this resonant frequency has a very low impedance for the third harmonic which can reduce the reactive power of the resonant tank circuit. So overall, the buck-boost operation is performed by just changing the input frequency of the converter.
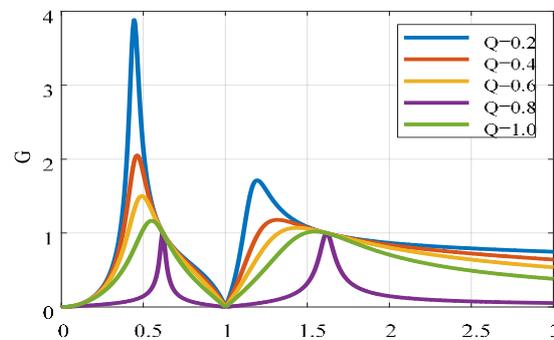
Figure 3. Gain characteristics of LLCLC resonant tank.

The gain of a resonant tank with L as the inductance ratio, Q as the quality factor, and f_N as the normalized switching frequency is given by (R. Mazgut et al., 2016):

$$|G|=n\frac{V_o}{V_i}=\sqrt{\frac{\left[Lk+(QL^2f_N)^2\right]^2+[QL^2f_N(L-k)]^2}{\left[(QL^2f_N)^2+k^2\right]^2}} \quad \text{where,} \quad k=\left(f_N^2-1\right)\left(\frac{1}{f_N^2}+(LQ)^2+\frac{L}{f_N^2-1}\right)-\frac{1+(LQf_N)^2}{f_N^2-1}$$

The resonant frequencies of the LLCLC resonant tank are given as $f_{R1}=\frac{1}{2\pi}\sqrt{\frac{-\sqrt{(A)^2-4B}+A}{2B}}$,

$f_{R2}=\frac{1}{2\pi}\frac{1}{\sqrt{L_pC_p}}$, and $f_{R3}=\frac{1}{2\pi}\sqrt{\frac{\sqrt{(A)^2-4B}+A}{2B}}$ where, $A=L_sC_s+L_pC_p+L_pC_s$ and $B=L_sL_pC_sC_p$.
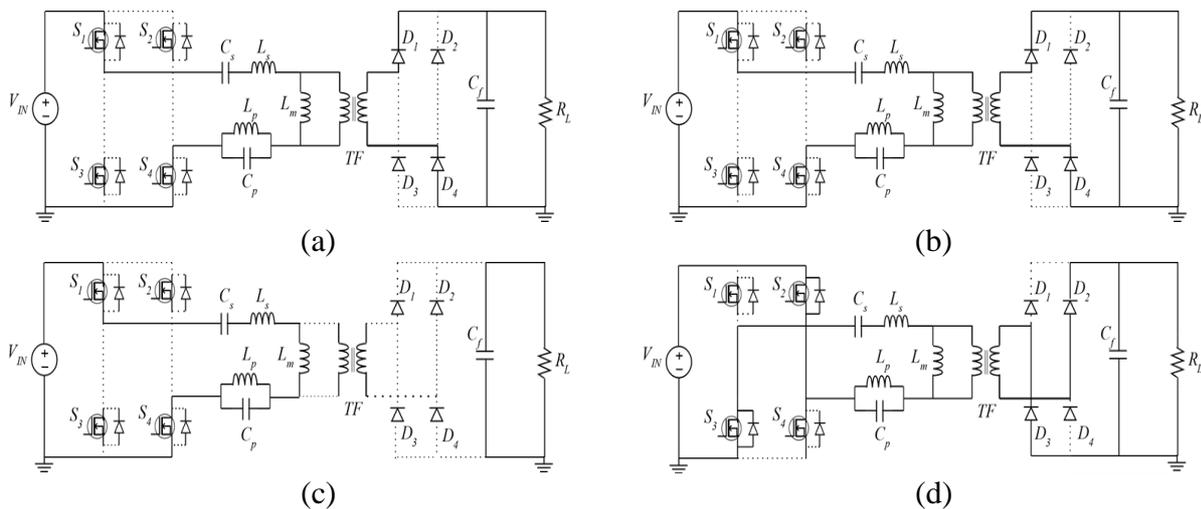
Modes of Operation

One complete switching cycle consists of 8 modes of operation. Firstly, it is assumed that all the switching components are ideal. Secondly, the circuit is already working and is in stable condition. The modes of operation of the LLCLC resonant converter (DC-DC stage) for the

$f_{R1} \leq f_S \leq f_{R2}$ frequency region are as follows:

Mode 1 [t_0-t_1]: At time t_0, the switches S_1 and S_4 are turned ON with ZVS, and diodes D_1 and D_4 conduct as shown in Figure 4a. The series resonant inductor current i_{Ls} is equal to zero and starts to increase in a positive direction. Meanwhile, magnetizing current i_{Lm} increases linearly towards zero from negative value. The primary side transfers energy to the secondary side through the resonance of C_S, C_P, L_S, and L_P.

Mode 2 [t_1-t_2]: At time t_1, the switches S_1 and S_4 are still ON and diodes D_1 and D_4 still conduct as shown in Figure 4b. The current i_{Lm} is equal to zero and starts to increase linearly in a positive direction. The current i_{Ls} still increase in the positive direction. The primary side continuously transfers energy to the secondary side.

Figure 4. Modes of Operation **(a)** Mode 1 **(b)** Mode 2 **(c)** Mode 3 **(d)** Mode 4

Mode 3 [t_2-t_3]: At time t_2, the switches S_1 and S_4 are turned off. The currents i_{Ls} and i_{Lm} are equal to each other and start to decrease. The current i_{Ls} flow through the body diodes of S_2 and S_3 which creates ZVS conditions for them. The primary side does not transfer power to the secondary side and all five components resonate.

Mode 4 [t_3-t_4]: At time t_3, the switches S_2 and S_3 are turned ON and diodes D_2 and D_3 start to conduct. The current i_{Ls} reach zero value while i_{Lm} continues to decrease linearly from positive value towards zero. The primary side transfer power to the secondary side through the resonance of C_S, C_P, L_S, and L_P.
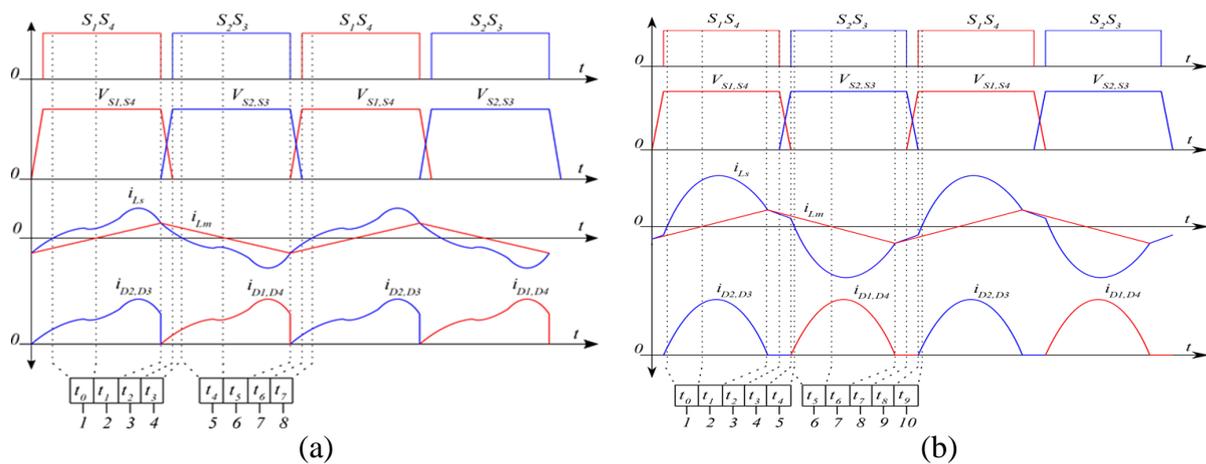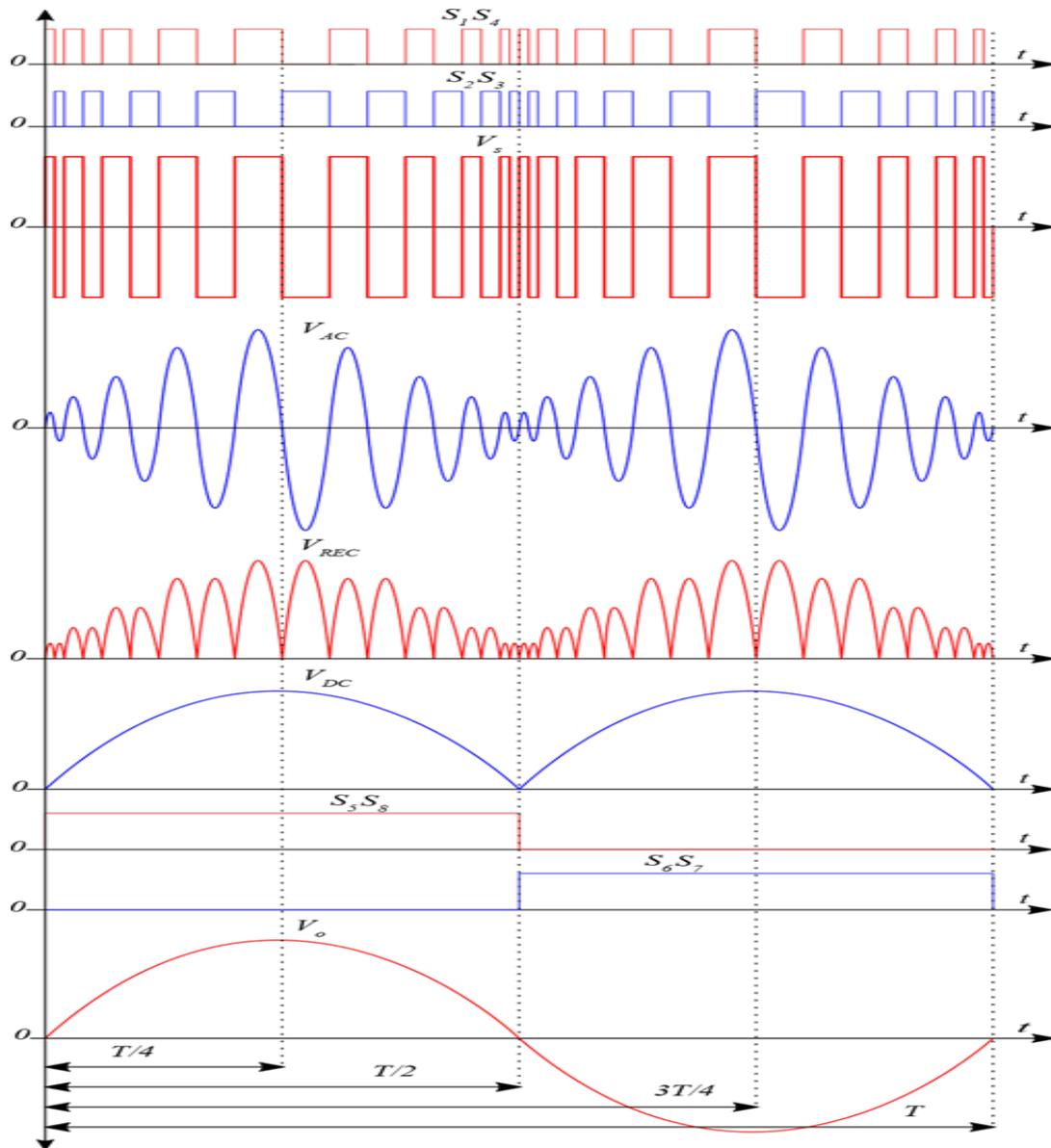
Figure 5. Graphical representation for modes of operation **(a)** for $f_{R1} \leq f_S \leq f_{R2}$ **(b)** for $f_S < f_{R1}$

Physically, when the secondary side is separated from the primary side, the components C_S, C_P, L_S, L_P, and L_m resonate together. When the primary side transmits power to the load, only C_S, C_P, L_S, and L_P resonate together. The successive modes of converter repeat the same way as described above. During the $f_{R1} \leq f_S \leq f_{R2}$ region, the converter injects a third harmonic to the load, so the resulting shape of the series resonant current is like a square wave. The graphical representation of modes of operation in the regions $f_{R1} \leq f_S \leq f_{R2}$ and $f_S < f_{R1}$ are given in Figure 5a and Figure 5b respectively. The converter works on discontinuous conduction mode and has two more modes in one complete switching cycle.

Working Operation of Inverter

The working principle of the proposed inverter with different stages is shown in Figure 6. A complete AC voltage cycle is divided into four stages. It is assumed that all the switching components and input power sources are ideal. In Stage 1 [0-T/4], the switching frequency of S_1 & S_4 changes from f_{R2} to f_{R1} regulating tank gain from 0 to 1. The voltage at the DC link stage continuously changes from zero to peak amplitude value. The switches S_5 & S_8 are always ON, so the DC link voltage appears on the output of the inverter. In Stage 2 [T/4-T/2], the switching frequency changes from f_{R1} to f_{R2} regulating gain from 1 to 0. Similarly, the DC link voltage changes from peak amplitude value to zero. The switches S_5 & S_8 are still on, thus appearing the DC link voltage to the output side. In Stage 3 [T/2-3T/4] and

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Stage 4 [3T/4-T], only the switches S_5 & S_8 are OFF while S_6 & S_7 are ON and other processes remain the same as in earlier stages.


Figure 6. Graphical representation of working operation.

In one complete AC output voltage cycle, switches (S_5 & S_8) are on for the first two cycles while switches (S_6 & S_7) are ON for the next two cycles. A similar switching pattern repeats in the next AC voltage cycles.

DESIGN CONSIDERATION

For designing the primary side variable switching frequency, firstly the secondary side constant switching frequency is considered because it occurs when the rectified voltage at

the pseudo-DC link stage is approximately equal to zero. The following factors are considered during the primary side variable frequency control design: (1) The primary side switching frequency should be f_{R2} when switches (S_5 & S_8) are ON. (2) During the half-ON time of secondary side switches (S_5 & S_8), the switching frequency should be less than f_{R2}. (3) During OFF time of switches (S_5 & S_8) and ON time of switches (S_6 & S_7) the primary side switching frequency again should be f_{R2}. A similar switching pattern repeats during the ON time of switches (S_6 & S_7). For this purpose, the control circuit is designed according to Figure 7. The input voltage frequency of the control circuit has the same frequency as the required output voltage frequency of the inverter. This voltage is rectified by a full wave rectifier. The full wave rectifier voltage is given to voltage-controlled oscillator (VCO). The voltage control is designed in such a way that it changes its output frequency according to the input voltage amplitude. The output pulse frequency of VCO at the lowest input voltage is f_{R2} and at the highest input voltage amplitude is less than f_{R2}.
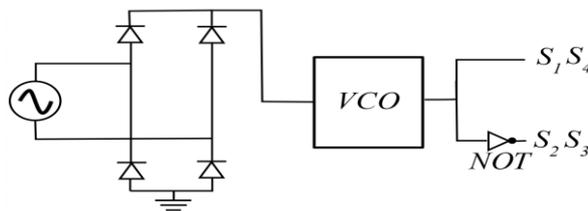

Figure 7. The control scheme for the primary side.

The maximum switching frequency of the resonant tank is f_{R2}. The lower switching frequency can be of any value in the ZVS region. It is preferred to use a switching frequency range between f_{R1} and f_{R2} because in this region the gain is evenly divided and below f_{R1} the gain changes exponentially. The design of C_P and L_P provides zero gain resonant frequency f_{R2}. So, there should be a proper distance between resonant frequencies so that f_{R2} is too close to f_{R1} or f_{R3}. For that purpose, if $C_S=C_P=C$ and $L_S=L_P=L$, f_{R1} is 61.8% of f_{R2} while f_{R3} is 161.8% of f_{R2}. The corresponding frequencies become $f_{R1}=0.618f_{R2}$ and $f_{R3}=1.61f_{R2}$.

Reactive Components Design

A 400W pseudo-DC link inverter is designed on our proposed topology. The input voltage is 40V while the maximum output voltage is 400V. The load resistance R_L is $\frac{V_o^2}{P_o}$=400Ω, n=G$\frac{V_i}{V_o}$=0.1 and R_{eq}=$\frac{8}{\pi}n^2\frac{V_0^2}{P_o}$=10.19. The Q point is 0.25 and the inductance ratio (L) is 3. The switching frequencies for the primary and secondary sides are selected as 200 kHz and 50 Hz respectively. The switching frequency range is f_{R1}<f_S<f_{R2} as the gain is evenly divided in this region. We consider C_S=C_P= $\frac{1}{2\pi f_{R2}QR_{eq}}$ = 310nF and L_S=L_P=$\frac{QR_{eq}}{2\pi f_{R2}}$ = 2uH, so that f_{R1} is 61.8% of f_{R2} while f_{R3} is 161.8% of f_{R2}. The f_{R1}=0.618*f_{R2}=123 kHz and f_{R3}=1.618*f_{R2}=323 kHz. The magnetizing inductance L_m is L*L_s=3*2=6uH. The remaining components used in the inverter are given in Table 1.

Table 1. Components and their parameters.

| Components	Parameters
Primary Switches (S_1 to S_4)	IRF1404
Full Wave Rectifier Diodes (D_1-D_4)	D1N1190
Transformer	TN33_20_11_2P90
DC link Capacitor	C_f=1.2uF
Secondary Switches (S_5 to S_8)	IRF840
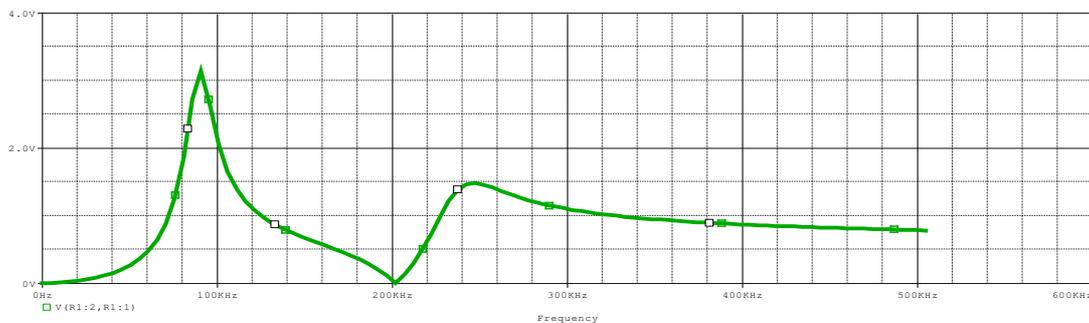
Figure 8. AC sweep of the designed tank.

To verify the component's design and resonant frequencies of the LLCLC resonant tank, the AC sweep characteristics of the designed resonant tank are determined and shown in Figure 8. The resonant frequencies f_{R1}, f_{R2} and f_{R3} are 123kHz, 200kHz and 323kHz respectively.

SIMULATION RESULTS

The working of our proposed inverter is verified by simulating our designed inverter on OrCAD PSpice software. The simulated graphs of inverter voltage analysis at different

stages are shown in Figure 9. The output of the resonant tank and full wave rectifier are depicted in red and blue respectively as shown in Figure 9a. Similarly, the output of the DC link and finally the inverter is depicted in red and blue respectively as shown in Figure 9b.


(a)   (b)
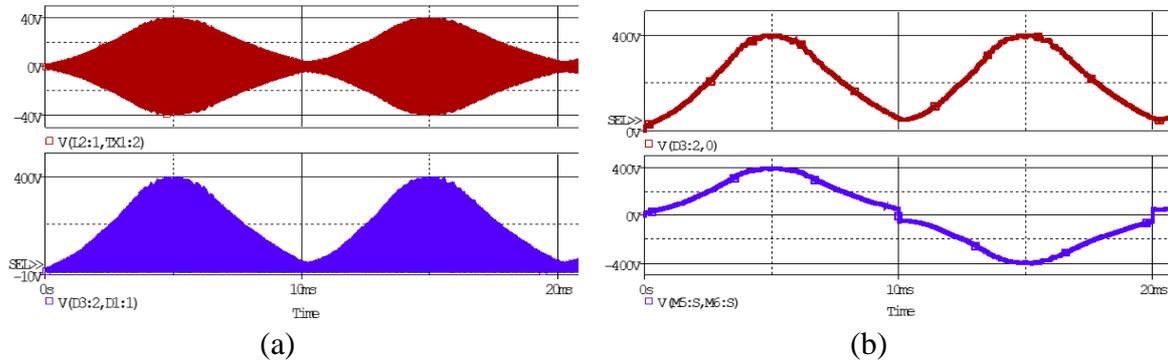
Figure 9. Inverter voltage analysis at different stages **(a)** LLCLC tank (red) & full wave

rectifier (blue) **(b)** DC-link (red) & inverter (blue).

The variable input voltage frequency of the resonant tank is between f_{R1} and f_{R2}. At f_{R1} the output is approximately equal to the input, so the gain is one. But at f_{R2}, the tank output is approximately 5V, therefore the minimum possible gain is 0.125 which is still much less than conventional LLC resonant tanks. The peak output voltage is approximately 400V for the rectifier and the DC link stage. The inverter voltage output has a peak value of 400V and an inverted peak value of -400V in a full AC sinusoidal voltage cycle.

DC-DC Stage Analysis

The simulated graphs of DC-DC stage analysis for current and voltage at different frequency regions are illustrated in this part and shown in Figure 10 to Figure 12. The output of drain to source voltage of switches (S_1, S_4 & S_2, S_3) w.r.t series resonant inductor current (I_{Ls}) of LLCLC resonant converter at different regions of f_S is shown in Figure 10.
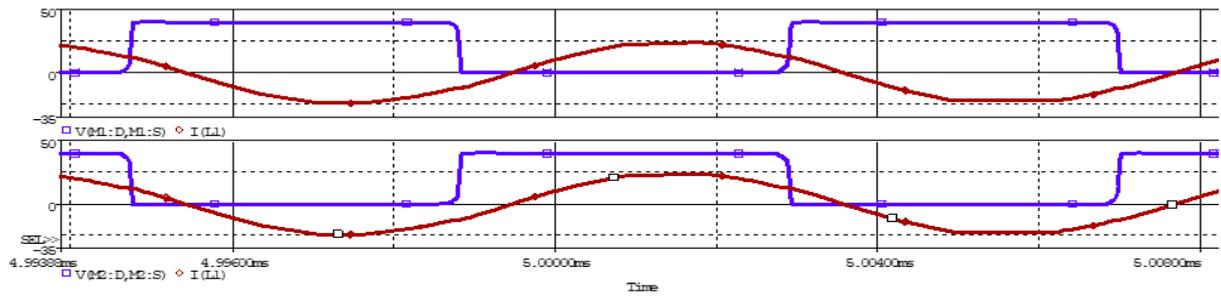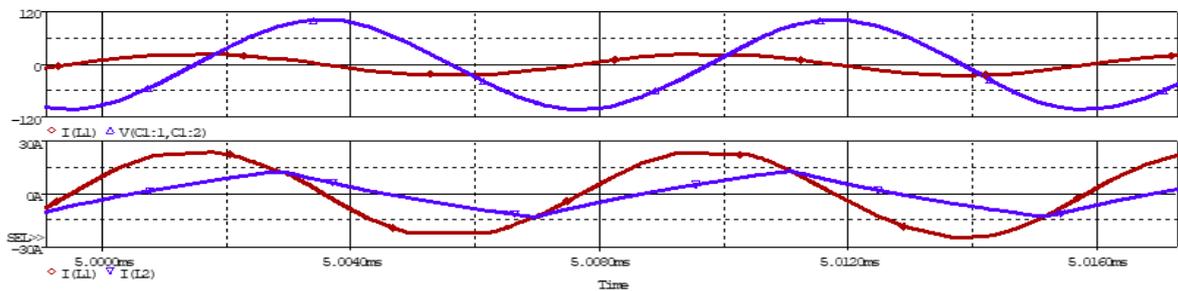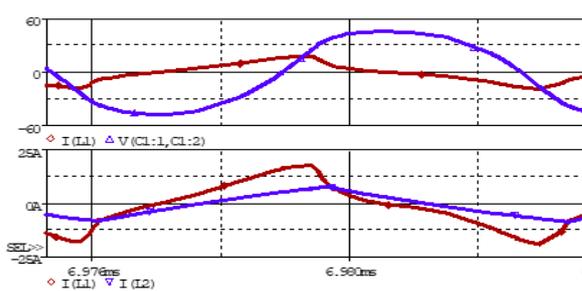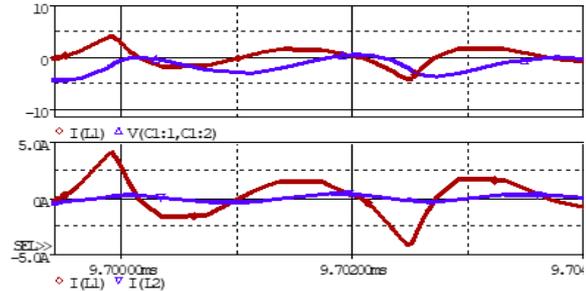
(a)
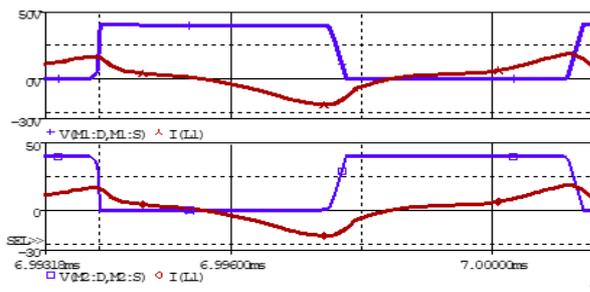
(b)
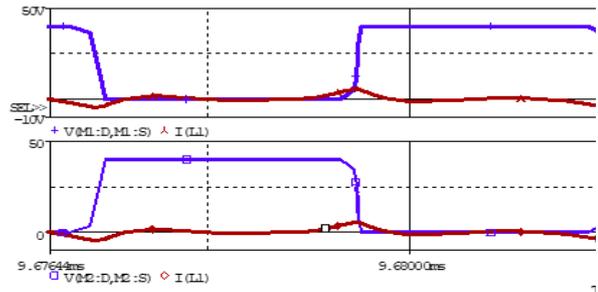
(c)

Figure 10. Current (I_{Ls}) w.r.t Voltage at S_1, S_4 & S_2, S_3 **(a)** $f_S=f_{R1}$ **(b)** $f_{R1}<f_S<f_{R2}$ **(c)** $f_S=f_{R2}$


(a)

(b)

(c)

Figure 11. Current (I_{Ls}) vs Voltage (V_{Cs}) & Current (I_{Lm}) **(a)** $f_S=f_{R1}$ **(b)** $f_{R1}<f_S<f_{R2}$ **(c)** $f_S=f_{R2}$

The voltage is reduced to zero before the resonant current achieves ZVS through inverter operation. The third harmonic is added to the resonance current when operating below f_{R1}. The resonant current is approximately zero at the f_{R2} switching frequency. The relation of

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series resonant capacitor voltage V_{Cs} versus I_{Ls} and I_{Ls} versus I_{Lm} at different regions of f_S are depicted in Figure 11. The current I_{Ls} lag the voltage V_{Cs} confirming ZVS in these regions. Also, the magnetizing current I_{Lm} increases and decreases linearly with the resonant current I_{Ls} in every cycle. The amplitude values became less for $f_S > f_{R1}$ but the behavior remains the same.

(a)

(b)

(c)
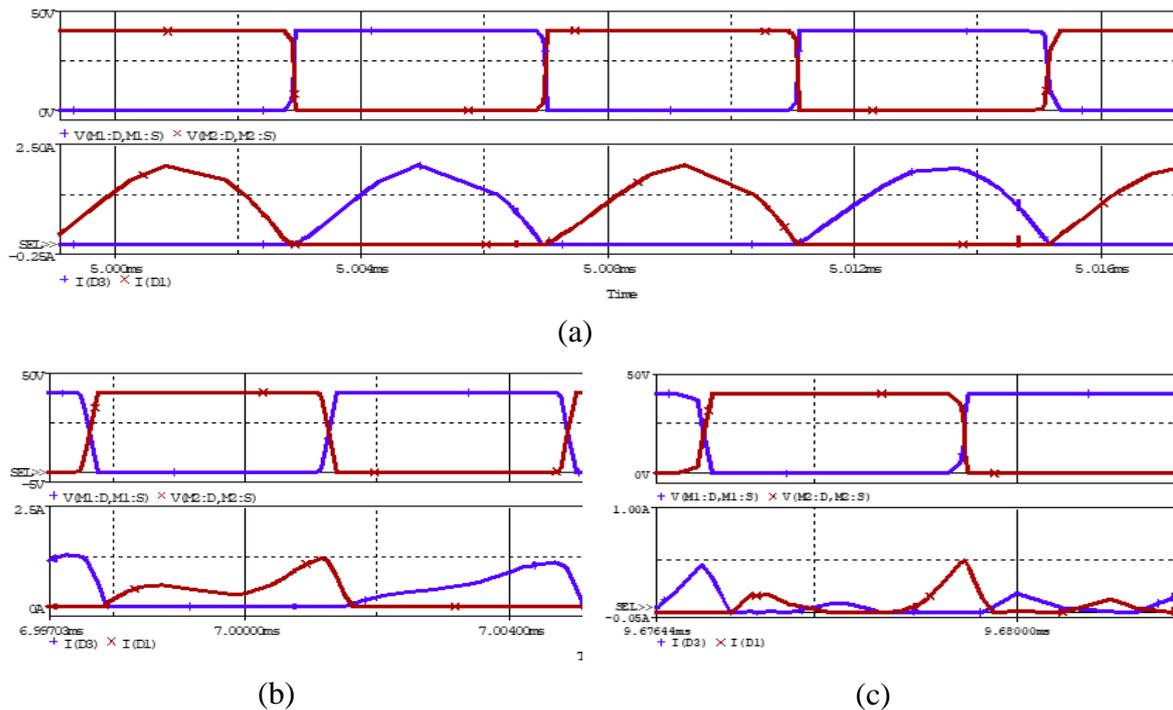
Figure 12. Rectified Current vs Voltage at S_1, S_4 & S_2, S_3 **(a)** $f_S = f_{R1}$ **(b)** $f_{R1} < f_S < f_{R2}$ **(c)** $f_S = f_{R2}$

The secondary side diodes (D_3 & D_1) current according to the primary side voltage at $f_{R1} \leq f_S \leq f_{R2}$ are given in Figure 12. Here, the voltage across diodes is proportional to the primary side switch's voltage. The currents through diodes (D_1 & D_3) at $f_S = f_{R1}$ are following the voltage waveform of primary side switches (S_1 & S_2). The diodes turn off at zero current achieving ZCS across them. For $f_{R1} < f_S < f_{R2}$ region, the behavior of output is the same as discussed above but with low amplitude values because the gain is higher near f_{R1}. At $f_S = f_{R2}$, the current through the diodes is very small because the gain is approaching zero.

CONCLUSION

An LLCLC resonant converter based pseudo-DC link inverter topology is proposed. The

inverter uses LLC resonant DC converter with an additional LC component providing 0.125 gain at resonant frequency f_{R2} by increasing the impedance of the tank to infinity. The inverter regulates the output voltage by changing the switching frequency of the primary switches. The inverter provides rectified DC voltage at the DC link stage which is unfolded to a sinusoidal voltage by the full bridge inverter. The performance of a 400W, 40V input, and 400V output pseudo-DC link inverter is evaluated by simulation on OrCAD PSpice.

REFERENCES

C. Yeh, C. Chen, M. Lee and J. Lai 2020. A Hybrid Modulation Method for Single-Stage Soft-Switching Inverter Based on Series Resonant Converter. J. IEEE Transactions on Power Electronics 35(6):5785-5796. doi:10.1109/TPEL.2019.2948122.

F. M. Guangul & G. T. Chala 2019. Solar energy as renewable energy source: SWOT analysis. 4th MEC International Conference on Big Data and Smart City (ICBDSC) 1-5 doi:10.1109/ICBDSC.2019.8645580.

H. Wu, X. Jin, H. Hu & Y. Xing 2016. Multielement Resonant Converters With a Notch Filter on Secondary Side. J. IEEE Transactions on Power Electronics 31(6):3999-4004. doi:10.1109/TPEL.2015.2507263.

J. Koscelnik, R. Mazgut, S. Kascak & M. Prazenica 2020. Review of Selected Multi-Element Resonant Topologies. J. Transactions on Electrical Engineering 4(4):86-90.

L. mol K Johny & T. K. Jose Sebastian 2013. A flyback DCM DC-AC converter for PV applications. Annual International Conference on Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy 1-6. doi: 10.1109/AICERA-ICMiCR.2013.6576018.

M. Xingkui, H. Qisheng, K. Qingbo, X. Yudi, Z. Zhe & M. A. E. Andersen 2016. Grid-connected photovoltaic micro-inverter with new hybrid control LLC resonant converter. IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society 2319-2324. doi:10.1109/IECON.2016.7793632.

N. Abas, A. Kalair & N. Khan 2015. Review of fossil fuels and future energy technologies.

J. Futures 69:31-49.

Q. Li & P. Wolfs 2008. A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations. J. IEEE Transactions on Power Electronics 23(3):1320-1333. doi:10.1109/TPEL.2008.920883.

R. Lin & L. Huang 2018. Efficiency Improvement on LLC Resonant Converter Using Integrated LCLC Resonant Transformer. J. IEEE Transactions on Industry Applications 54(2):1756-1764. doi:10.1109/TIA.2017.2771728.

R. Mazgut, M. Galad, S. Kascak & P. Spanik 2016. Analysis of multi-resonant LLCLC converter. ELEKTRO 192-195. doi:10.1109/ELEKTRO.2016.7512063.

S. Narendiran 2013. Grid tie inverter and MPPT - A review. International Conference on Circuits, Power and Computing Technologies (ICCPCT) 564-567. doi: 10.1109/ICCPCT.2013.6529017.

S. Pervaiz, M. Ur Rehman, A. B. Asghar & N. Zaffar 2013. A novel single-phase soft switching microinverter for photovoltaic applications. 3rd International Conference on Electric Power and Energy Conversion Systems 1-5. doi:10.1109/EPECS.2013.6713003.

Y. Xue, L. Chang, S. B. Kjaer, J. Bordonau & T. Shimizu 2004. Topologies of single-phase inverters for small distributed power generators: an overview. J. IEEE Transactions on Power Electronics 19(5):1305-1314. doi:10.1109/TPEL.2004.833460.

Y. Zhao, T. Wei, H. Hu and Y. Xing 2015. A high-efficiency pv grid-tied micro-inverter with soft switching for dc/ac stage. IEEE 10th Conference on Industrial Electronics and Applications (ICIEA) 1150-1154. doi:10.1109/ICIEA.2015.7334280.