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Low Voltage High Performance Floating Gate and Quasi Floating Gate CDTA

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ABSTRACT

A low voltage and low power current differencing transconductance amplifier (CDTA) based on Floating gate MOSFET (FGMOS) and Quasi-floating gate MOSFET (QFGMOS) is presented. The use of QFGMOS eliminates confined in the floating gate, degraded gain-bandwidth product, silicon area etc. The proposed circuits have been simulated using spice simulation software 180nm technology of analog devices LtSpice XVII and supply voltage used for this is ±1V.

Keywords: Current differencing transconductance amplifier, Floating gate, Quasi floating gate

INTRODUCTION

Reduced voltage and near to the ground power operation brings analog circuits design complications in them. Scaling of supply voltage degrades the steady functioning of the circuit. Due to this analog circuit designers have to meet various difficulties to preserve this. The growing request for smart and proficient portable biomedical and different electronic equipment's having extended battery life has enforced the VLSI trade to practice consistent and dependable methods for formulating efficient analog, capable mixed type circuits working at near to the ground voltage, low power in profound submicronic technology [1]. This demand has increased the popularity of many current mode circuits like second generation current conveyor (CCII) [2], operational transconductance amplifier (OTA) [2], current differencing buffered amplifier (CDBA) [3], current differencing transconductance amplifier (CDTA) [4] etc. The unconventional low voltage and low power (LVLP) CMOS methods are: circuits with end-to-end operative range [5], MOSFETs in weak inversion region [6], level shifter operating technique [7], bulk-driven (BD) technique on self-cascode MOSFET [8], floating gate (FG) approach, quasi floating-gate(QFG) approach, Bulk driven floating-gate (BDFG) MOSFET, and Bulk driven quasi floating gate (BDQFG) MOSFET [9].

Circuits with low supply voltage can be implemented by applying FGMOS technique which offers the capacity to adjust the effective threshold voltage [10]. With the capability to adjust and reduce the actual threshold voltage, the essential supply voltage to operate the circuit can be decreased [11]. Another gain to use FGMOS technique is that it is well-matched with CMOS circuit design. A range of latest publications describe numerous interesting applications of the quasi floating gate method in LVLP signal processing applications. Numerous dynamic low voltage essentials have been considered those utilizing the QFG technique, like current mirror (CM) [12], differential amplifier [13], transconductor amplifier [14], current conveyor second generation [15], and others.

The organization of this paper is as follows: principle and features of FG and QFG are presented next. Afterwards the internal structure of proposed FG and QFG CDTAs has been described. Then simulation results using ltspice software has been presented; Finally, conclusion settles the work done.

FLOATING GATE MOSFET(FG MOSFET)

FG MOSFET is mainly an altered form of conventional MOSFET where additional capacitances have been added between the conventional gate and the multiple input extra gates. One can reduce value of threshold voltage of FG MOSFET with the help of bias voltage connected to secondary gates. Extra input terminals are placed above the FG which are electrically insulated from it but connected capacitive [16]. For numerous dc operations, FG node acts as floating type because floating gate is entirely enclosed by highly resistive material. In order to program FGMOS charge is introduced on floating gate that helps in shifting threshold voltage and thus, device functionality can be controlled. The equivalent schematic for an n-channel FGMOS having N-input is shown in Figure 1 [16].

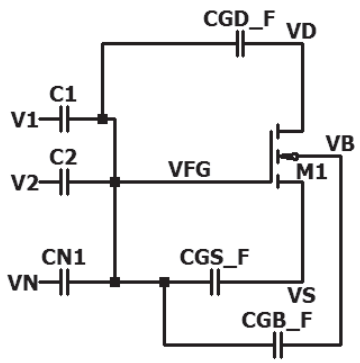

Figure 1. Equivalent schematic for an n-channel FGMOS having N-input

QUASI-FLOATING-GATE MOSFET (QFG MOSFET)

In QFG MOSFET, the FG is weakly coupled with the suitable supply voltage utilizing a larger resistance that can be realized using diode connected MOSFET in reverse bias mode, thus, removing the necessity of using large value capacitor as essential in FG MOSFET [16].This results in the improvement of frequency response and reductions in required chip area in QFG MOSFET. The large valued resistor connected at the gate terminal of QFG MOSFET to any of the supply voltages removes the confined charge problem of floating gate and also, reduces the supply voltage requests in a MOSFET based circuit. The equivalent circuit of the N-type and n-channel QFG MOSFET is shown in Figure 2 [16]. Authors in [17] demonstrates QFG and FG based multiple input operational transconductance amplifiers (MI-OTA) that shows by changing the biasing voltage we can vary the transconductance of the circuit. This paper shows increase in gain of the proposed circuits by applying FG and QFG techniques to differencing unit of CDTA instead of OTA unit. Also 3dB bandwidth of the proposed circuits has greater value.

In QFG MOSFET, a large biasing capacitor is not required; rather floating gate voltage is connected using a very large resistance to either of the supply. For practical determinations, the QFG of n-channel MOSFET is tied to VDD with the help of diode-connected PMOS working in reverse bias mode that acts as a large value resistor.

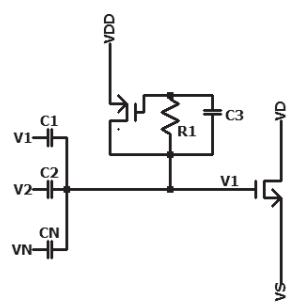

Figure 2. Equivalent circuit of N-type, n-channel QFG-MOSFET

While in case of p-channel MOSFET it is tied to VSS with the help of diode-connected NMOS working in reverse bias mode. This phenomenon eliminates the difficulty arises because of fabrication process results in collected charge trapped on floating gate as well as decreases the requirement of supply voltage. Additionally, the larger valued resistance usage makes the quasi floating gate efficiently floating for signals having low frequency, thus, not disturbing the ac operation of these signals. Furthermore, the limitations get removed as there is no requirement to use large biasing capacitor and thus results in lesser area requirement for chip designing and better frequency response.

A Current Differencing Transconductance Amplifier (CDTA) comprises of two units: Current Differencing Unit (CDU) and a transconductance unit where either single output OTA or multiple output OTA may be used. CDU utilizes the difference of input current and OTA produces the equivalent current of the voltage established at the node Z. CMOS based complete circuit diagram of conventional CDTA is shown in Figure 3. In CDTA, input stage derives the difference of input current signals and transfers this difference to the intermediate Z terminal, where this current is converted to a voltage via externally applied impedance. It is clear that the QFG MOSFETs offer better parameters than the FG MOSFETs. In this paper, the FG and QFG techniques have been selected to design low voltage CDTA.

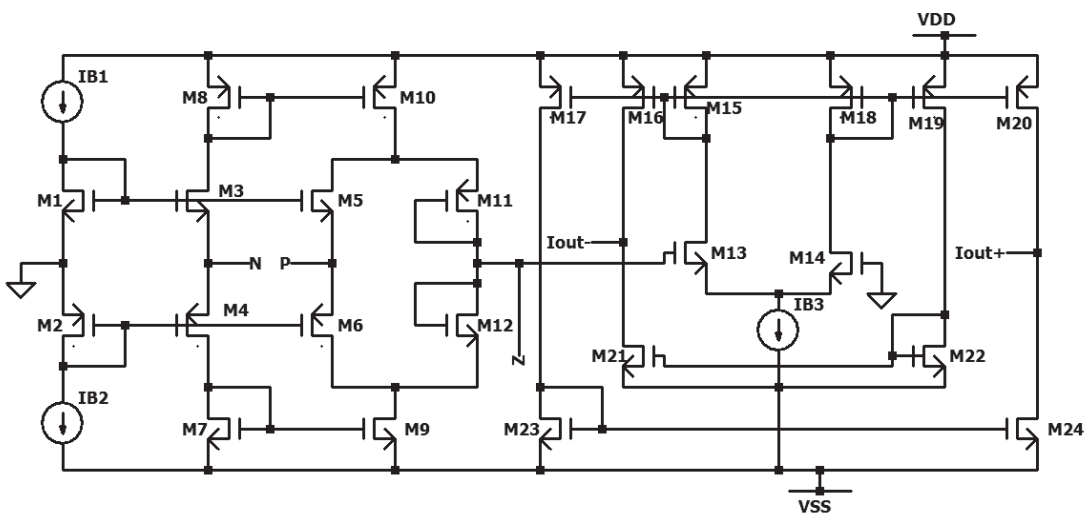

Figure 3. Circuit diagram of conventional CDTA

PROPOSED FG-CDTA

The circuit of conventional 2-stage CDTA is shown in Figure 4. Here 1st stage constitutes a current differencing unit (CDU) and 2nd stage forms an operational transconductance amplifier (OTA). To design a FG-MOSFET based CDTA, conventional MOSFETs M1 and M2 of 1st stage are replaced by FG-MOSFETs. Here, the floating gates consisting M1-M2 are tied to parallel combination of resistance and capacitance and bias voltage applied to one of floating gate terminals while the second gate terminal is connected to gate terminal of other MOSFET. Circuit of this proposed FGMOS based CDTA has been shown in Figure 4. This proposed FG-CDTA operates at low supply voltage of ±1V. It offers high linearity range and reduces power consumption. However, this CDTA degrades the AC performance and reduces bandwidth.

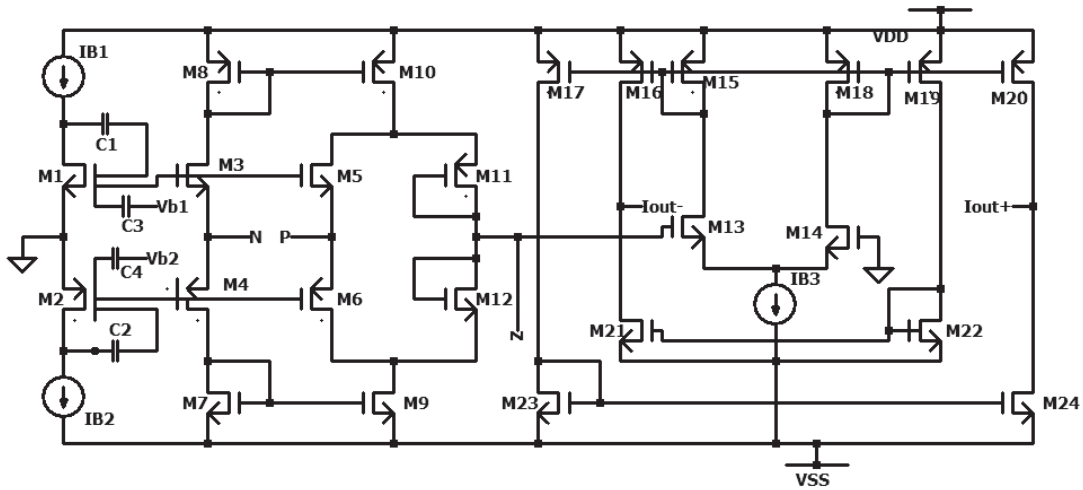

Figure 4. Circuit of proposed FG-CDTA

The FGMOS CDTA presented in [18] applied low power technique (FGMOS) on two PMOS of OTA, therefore operated with reduced biasing current of OTA. It worked at supply voltage of ±1.4V and had power dissipation of 2.60mW. The proposed FG-CDTA in this paper works low power technique on CDU, therefore worked with compact biasing currents of CDU. Proposed FG-CDTA works at ±1V and power dissipation of 1.1mW.

PROPOSED QFG-CDTA

The circuit comprising proposed QFG-CDTA is displayed in Figure 5. Here, QFG technique is applied to 1st stage MOSFETs M2 and M1. The floating gate terminals of M2 and M1 are tied to the positive supply (VDD) and negative supply (*V*SS) respectively through very high valued resistance created by transistors M2a and M1a. The input terminals of M2 and M1 are capacitive coupled to the quasi-floating-gates via C2 and C1 respectively from one side and connected to gate terminals from the other side. This proposed QFG-CDTA functions using low supply voltage of ±1V with minimized energy usage. This CDTA has better AC response and wider bandwidth as compared to proposed FG-CDTA. After adding a very high valued resistor in form of diode connected MOSFETs, another low voltage CDTA with QFG technique has been designed.

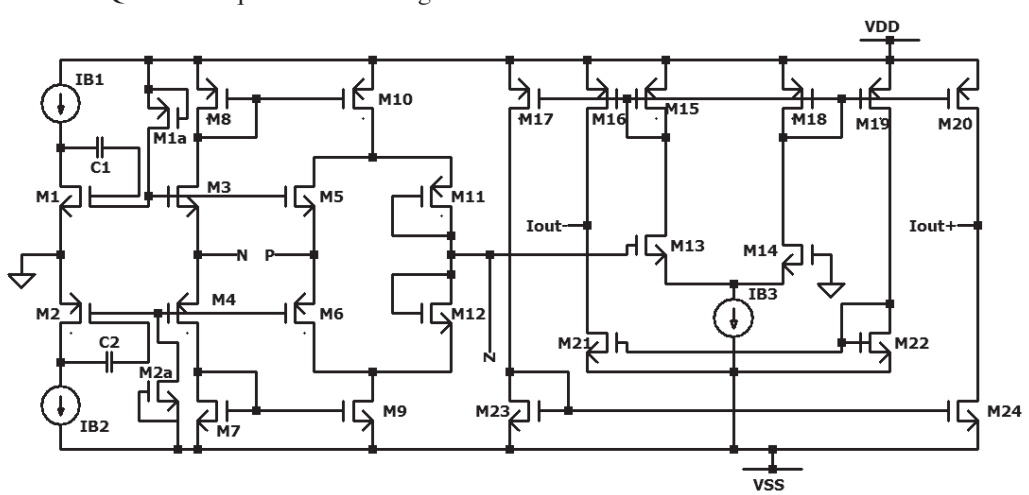

Figure 5. Circuit of proposed QFG-CDTA

Table 1. Design parameter Table

Parameter Name	Parameter Value
M1- M6	L = 1µm W = 8µm
M7-M10	L = 1µm W = 5µm
M11-M12	L = 2µm W = 20µm
M13-M14	L = 1µm W = 16µm
M15-M20	L = 1µm W = 6µm
M21-M24	L = 1µm W = 4µm
Technology	0.18 µm
Supply Voltage	±2.5V (Conventional CDTA) ±1 V (Proposed CDTAs)
IB1 and IB2	20µA
IB3	100µA
C1, C2	100fF

SIMULATION RESULTS

LTspice XVII has been used to simulate all the circuits discussed in the paper. Technology file of CMOS 0.18μm has been used for the simulation purpose. A supply voltage of ±2.5V has been used to simulate conventional CDTA while ±1V has been used for simulation of the proposed CDTAs. A variation in output current has been observed over an input current range of -100μA to 100μA. A load of 100Ω is used to obtain the output current in the circuits. Transistor aspect ratios and various design parameters for the circuit have been summarized in Table 1.

DC ANALYSIS

The output currents (Iout+ and Iout-) obtained for the specified biasing currents, in case of conventional CDTA, proposed FG CDTA and proposed QFG CDTA have been shown in Figures 6, 7 and 8 respectively. These figures show a linear relationship for all the 3 circuits between output current with respect to variation in input current in the range of -100μA to 100µA.

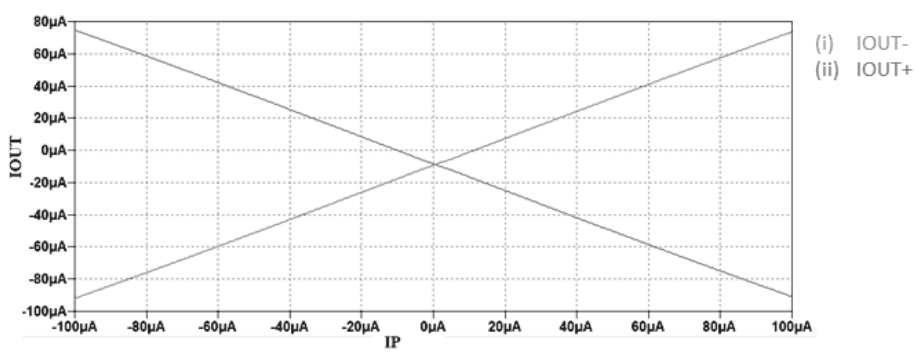

Figure 6. Output currents of conventional CDTA with variations in input current (Ip)

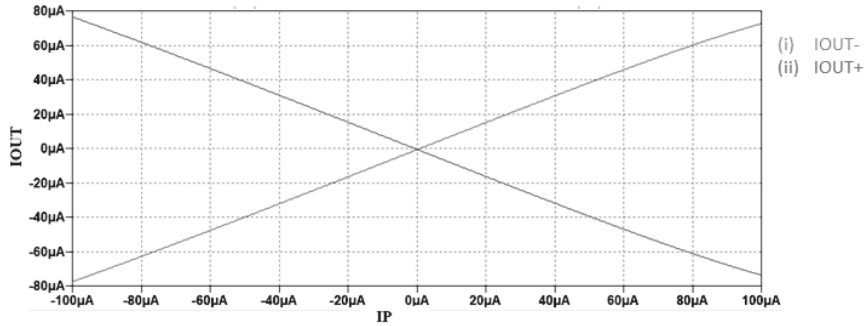

Figure 7. Output currents of FG CDTA with variations in input current (Ip)

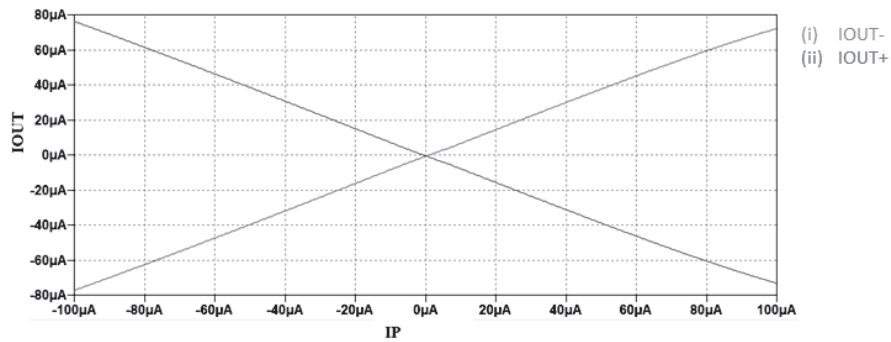

Figure 8. Output currents of QFG CDTA with variations in input current (Ip)

AC ANALYSIS

Frequency response curves showing current transfer characteristics of FG CDTA for input being applied at p terminal (Iout+/Ip; Iz/Ip) and for input being applied at n terminal (Iout+/In; Iz/In) are represented in Figures 9 and 10 respectively. Similar curves for QFG CDTA have been plotted in Figures 11 and 12 respectively. These curves show that -3dB bandwidth for FG CDTA is 52 MHz and 32 MHz for Iz/Ip and Iz/In respectively. While these parameters get enhanced significantly in QFG CDTA and shows increase by approximately 3 to 4 times. Similar enhancement in bandwidth is observed for Iout+/Ip and Iout+/In of QFG CDTA as compared to FG CDTA. This occurs due to reduction in parasitic capacitances in case of QFG CDTA as compared to that in FG CDTA. All these simulated results have been tabulated in Table 2.

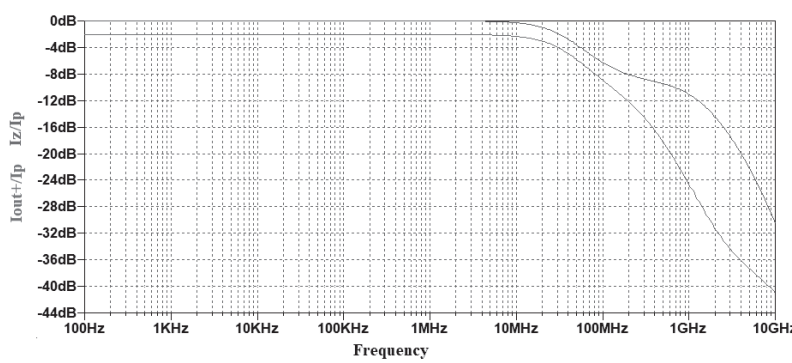

Figure 9. Iout+/Ip and Iz/Ip vs frequency for FG CDTA.

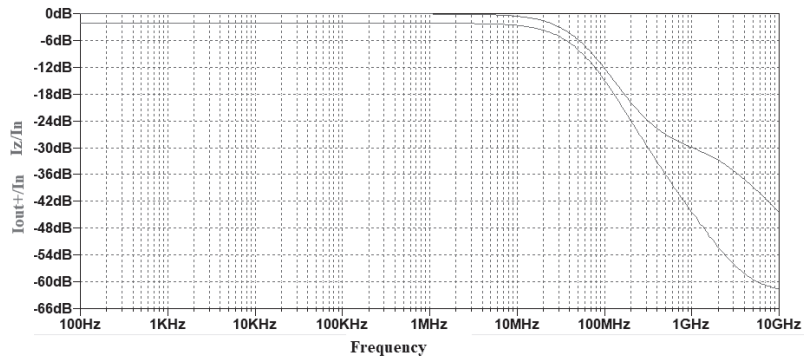

Figure 10. Iout+/In and Iz/In vs frequency for FG CDTA.

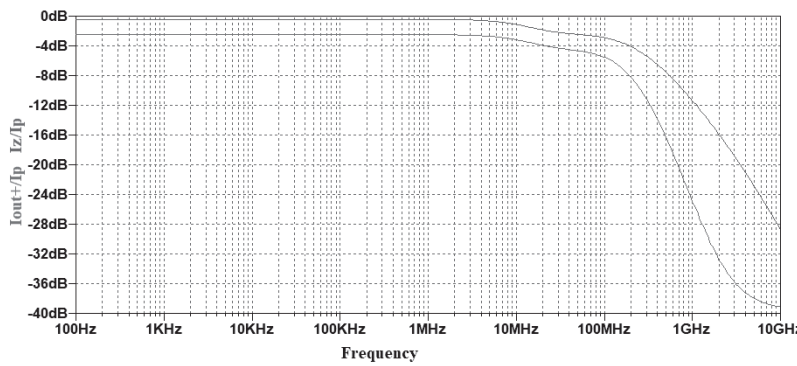

Figure 11. Iout+/Ip and Iz/Ip vs frequency for QFG CDTA.

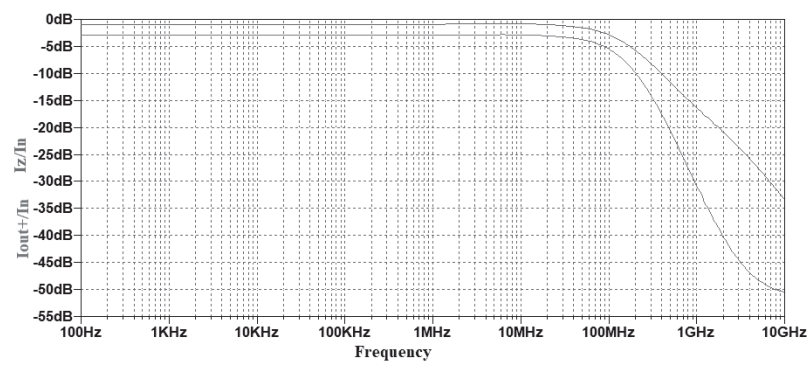

Figure 12. Iout+/In and Iz/In vs frequency for QFG CDTA.

CONCLUSION

In this paper, two high performance CDTAs based on FGMOSFET and QFGMOSFET technology have been proposed. These proposed CDTAs function at paticularly low supply voltage of ±1V and consumes extremely less power. Proposed FG-CDTA has witnessed to show degradation in parameters like 3dB bandwidth and gain. However, in QFG-CDTA their values improved significantly. The operation of proposed CDTAs have been presented at supply voltage of ±1V, the circuits have been simulated with the help of BSIM3 model for 0.18 μm CMOS technology using LtSpice. It has been apparent that both the proposed CDTAs works well for low power applications and are valuable for low voltage analog signal processing applications. Also, QFG based CDTA offers higher bandwidth. The performance assessment of both the proposed CDTAs shown in the paper, relate that they are relatively good choice for designers working at low supply voltages.

Table 2. Implementation contrast of conventional CDTA and proposed FG CDTA & QFG CDTA.

Parameters	Conventional CDTA	Proposed FG CDTA	Proposed QFG CDTA
Current Range(μA)	-78μA to 78μA	-78μA to 78μA	-75μA to 75μA
M1a, M2a added	No	Yes	Yes
Iz/Ip Bandwidth	104 MHz	52 MHz	112 MHz
Iz/In Bandwidth	55 MHz	32 MHz	110 MHz
Iout+/Ip Bandwidth	102 MHz	33 MHz	108 MHz
Iout+/In Bandwidth	54 MHz	28 MHz	105 MHz
Supply Voltage	±2.5 V	±1 V	±1 V
Power (mW)	0.12	0.11	0.10

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