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Comparative Analysis of Preamplifiers for Comparators

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ABSTRACT

In low power electronics technology, a lot of new technology has already been introduced to reduce the power consumption of comparator. This paper presents the comparative study of preamplifier circuit on power consumption and delay prospects. The preamplifiers are explained to make the clear difference in the state-of the art. Every circuit has their own importance in the different application such as analog-to-digital converter and comparator. The general trend to design an efficient preamplifier is that it should have low power consumption in their operation. Operating region of preamplifier circuit is observed as sub threshold and saturation. A small modification has been performed in preamplifier in comparator circuit and compared the power and delay with the reported comparator circuits. All the preamplifier circuits are implemented on 180nm CMOS technology node. The voltage supply used 1.2 V in implemented circuit.

Keywords: Low Power, Differential amplifier; Preamplifier; Comparator; Sub threshold; CMOS.

INTRODUCTION

Comparators are very important blocks for any analog to digital converter. Power dissipation and speed are major issues for the last few years for any analog to digital conversion. This paper presents the performance comparison of preamplifier circuits. The preamplifier is the first stage of a comparator which amplifies the input signals that can be detected at second stage of comparator. Since a comparator circuit comprises two basic stages, preamplifier and latch circuits as first and second stages respectively. The primary goal of latch stage is to compare two input signals and convert the output either "0" (logic low) or "1" (logic high). Latch stage can make comparison between input signals only when these input signals are detectable. Normally latch inputs should have strong enough voltage which can drive the latch stage. Therefore to ensure input of latch stage strong enough, preamplifier stage is employed as a first stage in comparator. The preamplifier is basically a differential amplifier in addition to this, it removes the kickback noise and dc offset voltage from the comparator circuit as well. Hence preamplifiers have number of applications from Analog to Digital Converter (ADC) and many other converter circuits also. In the view of preamplifier performance analysis few preamplifiers application configurations are presented. The blue colored inverter shows the change in circuit w.r.to conventional comparator circuit.

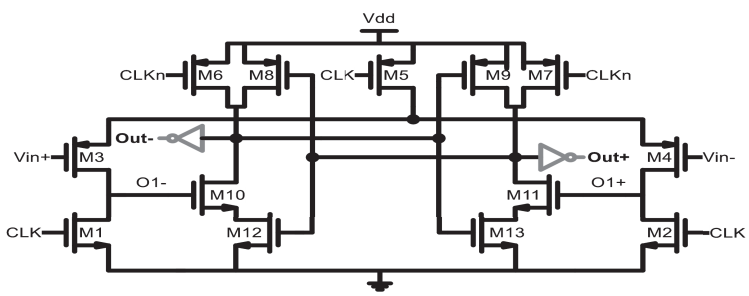

Figure 1. Dynamic Comparator (Conventional)(A. Khorami & M. J. E. L. Sharifkhani, 2016)

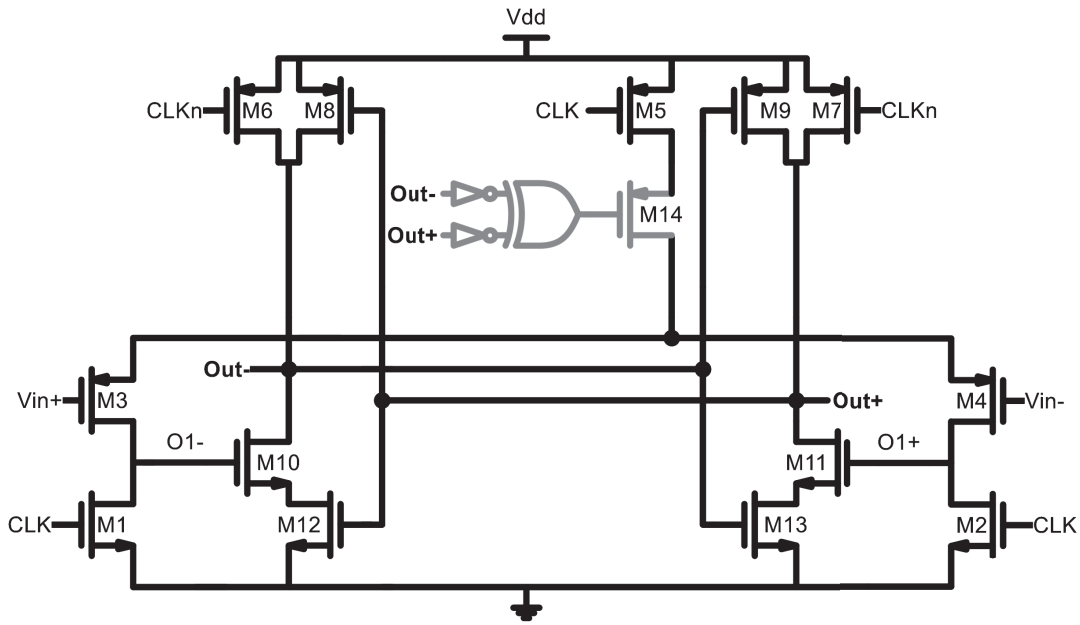

Figure 2. Reported comparator circuit (A. Khorami & M. J. E. L. Sharifkhani, 2016)the blue colored component shows the change in circuit w.r.to conventional comparator circuit

Figure 1 and 2 are the reported comparator circuit in (A. Khorami & M. J. E. L. Sharifkhani, 2016) uses to stop the pre amplification phase while dynamic comparator behavior remains unaltered. Since the preamplifier is the main stage so it consumes major portion of entire power dissipation of the comparator circuitto amplify preamplifier output up tothe threshold level of latch's input. So that preamplifier output can drive the latch stage properly. The preamplifierworking is just to activate latch stage once only by providing (O1+) and (O1-) voltagesat leastthe threshold voltage of M_10 and M_11 transistors of the latch stage because once latch isswitched on it attains output large enough for low and high logics as V_dd and ground respectively, after that the preamplifierturns-off, which is due to positive feedback employed in latch circuit. In case of Fig. 2 in between latch and preamplifier a small circuit is used to make feedback path, which is power gating circuit Ex-OR logic gate with minimum delay almost tobe having negligible delay. After latch is activated, there is no need of preamplifier which consumesmajorportion of power of comparator circuit. So preamplifier is needed to be turned-off once latch is activated. Reported technique (A. Khorami & M. J. E. L. Sharifkhani, 2016)reduces power consumption by more than 50% at 0.5GHz on 180nmC-MOS and moreover the area occupied by Ex-OR logic gate is less than 8% of the entire comparator circuit.

The reported work in (Khorami, Sharifkhani, & Communications, 2016)in Fig. 3, authors have explained about the delay and power contribution by the particular part of the circuit. As the power dissipation of the comparator circuit halves. The voltage swing of preamplifier stage is kept at V_dd/2. Since preamplifier stage is responsible for power consumption and latch stage is responsible for the delay of the comparator circuit. HigherV_ddoffersmore power consumptionwith less delay andlowerV_dd offersmore delaybut low power consumption.Therefore, in case of circuit in Fig. 3 value ofsupply voltage isoptimized andchosensuch that the response of preamplifier stagecan generate itsoutput as O1+ and O1-that can drive or turned-on the latch stage. By halving the value of supply voltage aboutV_dd/2power consumption of preamplifier get halved while delay of the comparatorremains unchanged. It is observed that half of supply voltage is the minimum voltage level required at the input of latch stage to just turn-on latch stage.Once latch is turned-ondue to its positive feedback is provided in latch circuitry.Therefore, the output voltage swingof preamplifiercan be minimizednot lesservaluethan half of supply voltage of aboutV_dd/2. Once latch acknowledgesthe initiation of the comparison process, preamplifier is turned-off, in order to overcome the

unnecessary power dissipation from the preamplifier stage of the comparator circuit since preamplifier consumes the major portion of total power consumed by the comparator circuit. The circuit in (Khorami, Sharifkhani, et al., 2016) consumes 0.42mW at 0.5GHzand occupies 453μm2 area operating at 4.54GHz frequency on 180nm CMOS technology

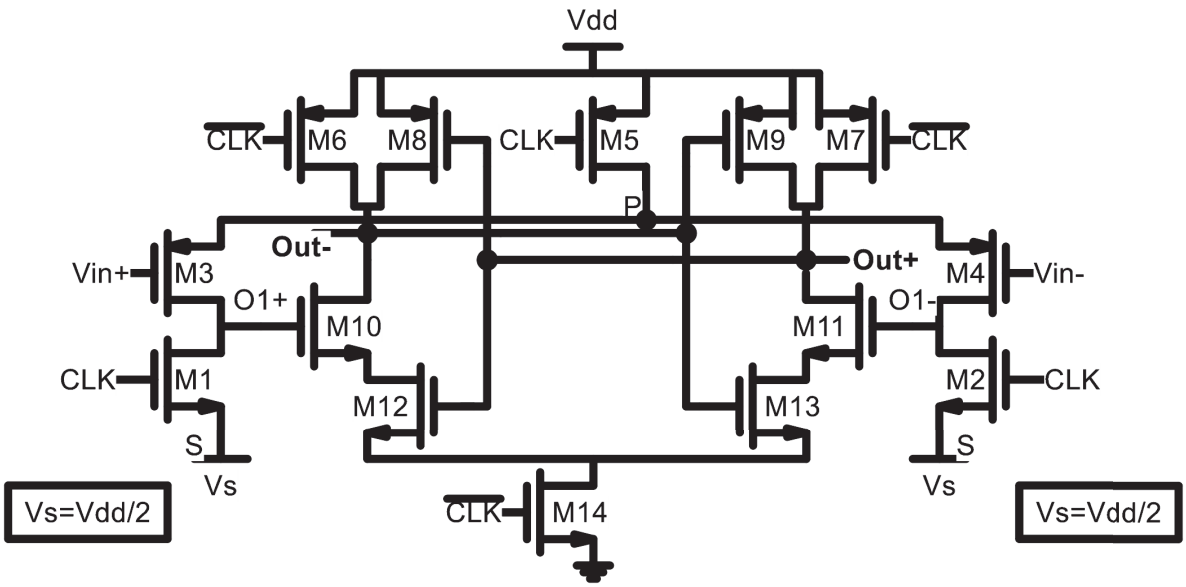

Figure 3. Comparator Circuit reported in (Khorami, Sharifkhani, et al., 2016).

node. The comparator circuit in Fig. 4 is reported in paper (A. Khorami & M. Sharifkhani, 2016), in which researcher have explained mainly about comparison of the comparator. The comparison time of latch circuit is made half by keeping preamplifier voltage swing just aboveV_dd/2, since V_dd/2is the minimum input voltage needed to make latch circuitry to turn-on. Thus it has to drivesthe latchstrongly at the same time delay is made halved.

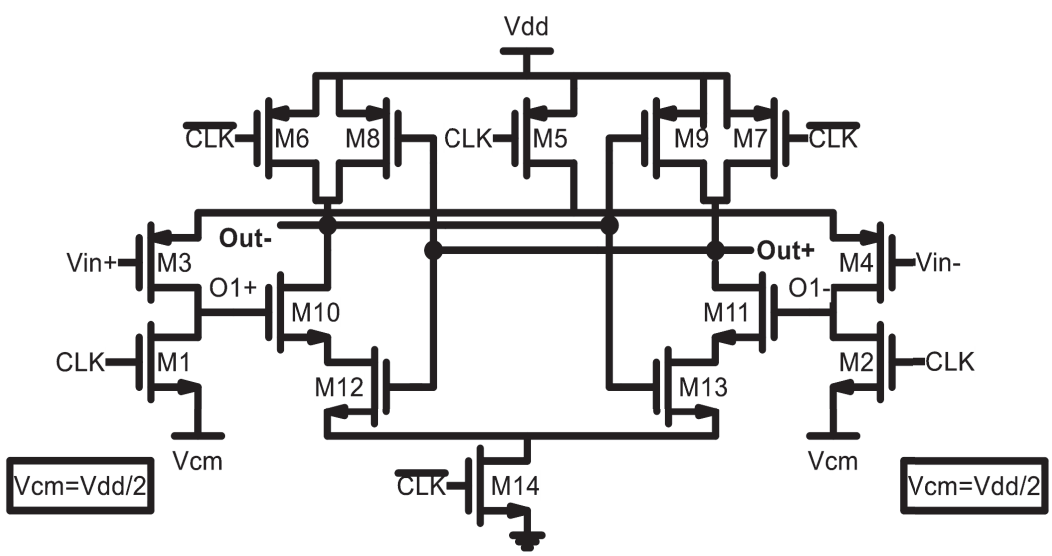

Figure 4. Comparator Circuit reported in (A. Khorami & M. Sharifkhani, 2016).

The speed of circuit in (A. Khorami & M. Sharifkhani, 2016) is double than the conventional circuit and the conversion time of latch circuit is being 255ps when the operating frequency is 0.5GHz and occupies 52.6μm^2 area and consumes 420μW at offset voltage of 2.6mV with 0.94V_dd is (V_cm)max.Input. Conversion time of the latch is governed by:

Comparison Time:

$$T_{latch} = T_1 + t * ln\left\{\frac{0.5(V_{dd} - Gnd)}{\Delta V_{in}}\right\}$$

$$T_1 = \left\{\frac{C}{\frac{1}{2}\mu_n C_{ox}\left(\frac{w}{l}\right)\left(V_{cmp} - V_{thn}\right)^2}\right\} * V_{thp}$$

The reported circuits in (Khorami, Dastjerdi, & Ahmadi, 2016) is presented in Fig. 5 and 6, in this paper (Khorami, Dastjerdi, et al., 2016) author discussed about the optimizing the comparison time delay. There are two stages in the high speed and low power comparator. First preamplifier stage is made turned-off after second latch stage is activated, so that power dissipation of comparator circuit is minimized. Since preamplifier circuit is the major power consuming part of comparator. Transistors M_3 and M_4 are kept sufficiently large for enhancing gain of preamplifier. In order to minimize the delay of the latch stage, control signals are utilized. This controls the delay of latch stage, which is implemented usingdelaytime-based controller.

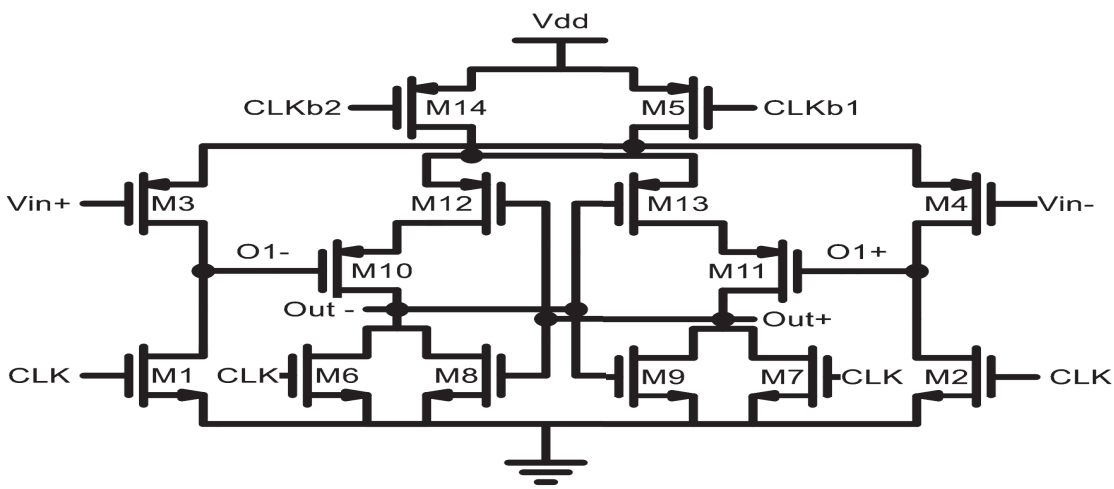

Figure 5. Reported circuit in (Khorami, Dastjerdi, et al., 2016).

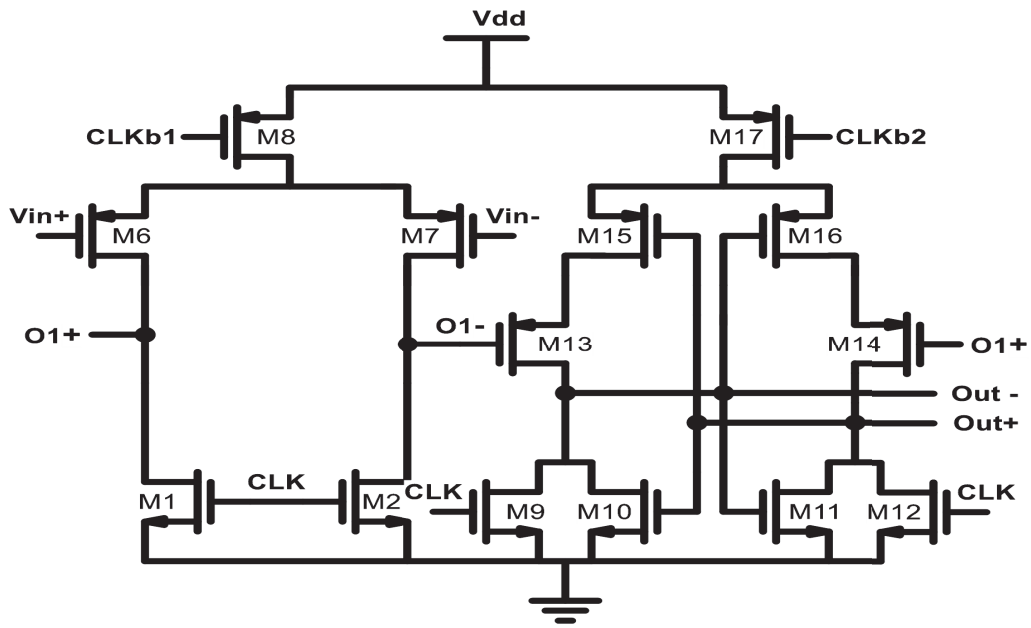

Figure 6. Reported circuit in (Khorami, Dastjerdi, et al., 2016)

At the same time Vcmat output nodes of preamplifier are kept small enough so that output of the preamplifier stage can activate PMOS strongly in the latch stage. It dissipates 230μW which is nearly halves the power dissipation, with the comparison time 210ps operating at 3.7GHz on 180nm technology nodewith the speed 76.2% improved than conventional circuit.

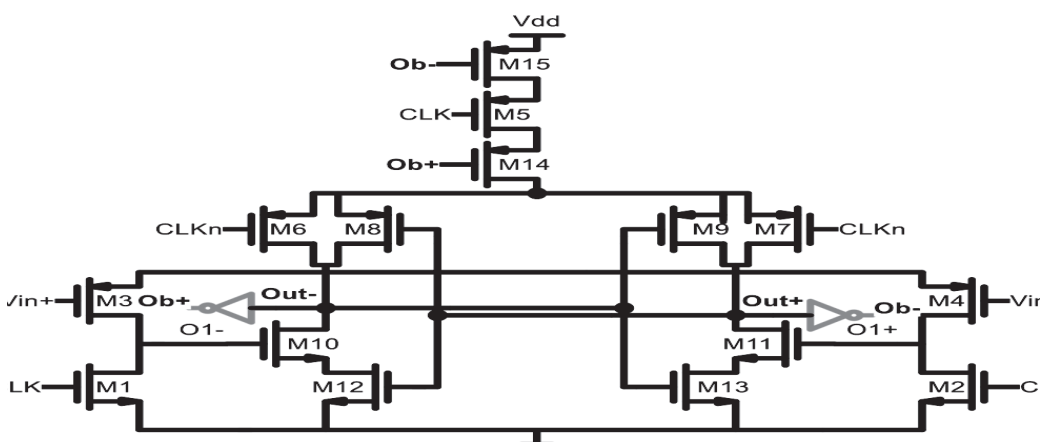

Figure 7. Reported circuit the blue colored inverter shows change in circuit w.r.to conventional comparator circuit

Figure 7 from the paper (Khorami & Sharifkhani, 2017) emphasized on reduction of power of two stage comparator. As we know that the preamplifier and latch circuits are the first and second stage respectively. The latch circuit ensures the initiation of comparison process. There after the power prevention method applies on comparator circuit. The preamplifierstage turns-off after confirming output of the latch and then latch stage finishes comparison. To minimize the power dissipation of the preamplifier stage, power gating circuit is employed in (Khorami & Sharifkhani, 2017). Switch transistors M_14and M_(15)are employed to turn-ON and turn-OFF the preamplifier stage accordingly as shown in Fig. 7. Ongettingbothequal inputs i.e. (ob+) = (ob-) from latch output confirming comparison ends by latch stage.(ob+) = (ob-) =1 at High (Vdd), these exception makes preamplifier to switched-on. Since at identical inputs, power gating circuit must make the preamplifier stage switched-on. This phenomenon must be repeated if identical outputs of latch circuit are generated. To overcome exceptional case an Ex-OR logic gate may be employed instead of using the transistors M_14 andM_15 as presented in preceding work. The Power consumption minimizes by 30%-58% when compared to the conventional comparator circuit by using supply voltage is V_dd/2at 0.5GHz operating frequency on 180nm CMOS technology node. Hence this work reduces power dissipation of the comparator circuit.

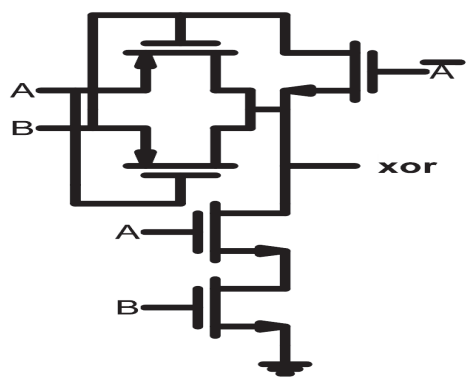

Figure 8. Reported circuit in (Naseri & Timarchi, 2018).

To shrink the area and dissipation of power through Ex-OR power gating circuit, minimization of number of transistor in Ex-OR logic gate circuit is necessary. Author in (Naseri & Timarchi, 2018) have presented an Ex-OR logic gate with 5 transistors (5T) only called as 5T XOR logic gate is presented in Fig. 8. It overcome large number of transistors in Ex-OR logic gate circuit as utilized in previously designed Ex-OR logic gate hardware. The 5TEx-OR-logic gate offers the best 3 parameters that are Power, Delay and PDP.It consumes $4.14*e^{-6}$W with the delay of 26.4ps and provide the PDP as 109.3aJ, which are obtained with the supply voltage of 1.2V and operated at 1GHZ on 65nm CMOS technology (Savani & Devashrayee, 2018).

The reported work in (Wang et al., 2019) described about the transconductance enhancement at the latching stage shown in Fig. 9 and 10. Dynamic comparator is a key unit of analog to digital converter and other analog to digital interfacing circuits and vice-versa. Those are highly desirable with low power and high-speed portable devices world. Speed or delay of latch decides operating frequency of comparator which depends upon the total transconductance offered by the latch stage. Latch is made of two cross-coupled inverters with positive feedback configuration.

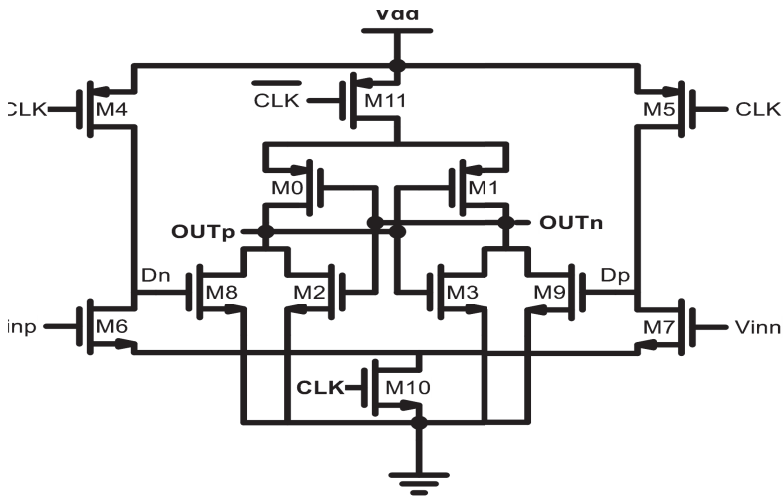

Figure 9. Reported circuit in (Wang et al., 2019)

In order to minimize Trans conductance of latch stage conventional latch uses zero gate-to-source voltage with two transistors, whereas latch stage in (Wang et al., 2019) uses separate gate biasing with cross-couples transistor inverter circuit (Almansouri, Alturki, Alshehri, Al-Attar, & Fariborzi, 2017). Dynamic comparator presented in (Wang et al., 2019) operates at 1.2V, 2GS/s utmost sampling speed and 110fJ energy per comparison. This circuit provides the high speed latch and reduces energy consumption. Energy consumption is another desirable constraint of dynamic comparator circuit design(Shinde & Sharma, 2017)(Al-Qadasi, Alshehri, Almansouri, Al-Attar, & Fariborzi, 2018; Filippini, Taskin, & Briefs, 2019).

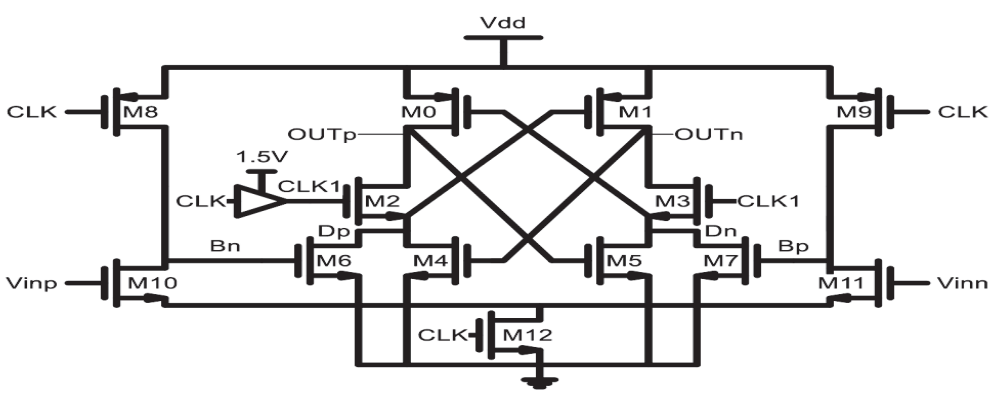

Figure 10. Reported circuit in (Wang et al., 2019)

MODIFIED PREAMPLIFIER CIRCUIT

This work presents the comparative analysis of parameters of preamplifier circuit which is used in comparator circuit. The modified preamplifier circuit presented in Fig. 11 in order to enhances the performance parameters of the circuit than the exciting circuit. The minimization in power consumption and delay with optimum offset voltage of the preamplifier circuit is carried out under. The voltage variation across output arms of Voutp and Voutn is to be made as higher as possible, since these two outputs have to be strong enough to operate the latch stage of the comparator circuit. Each arm of modified preamplifier circuit as shown in Fig.11is entirely depends upon biasing of each transistor. Supply is minimized up to the minimum and fixed around the optimum level and it can operate the circuitry only not in excess level. When modified preamplifier generated perfect response, operating regions of transistor M3 in linear, M1a and M1b are both in saturation region, M2a and M2b are in cutoff or sub threshold region while tests are carried out. All calculations of power dissipation, delay and offset are carried out usingcalculation function of cadence EDA tool as depicted in Tables 1 and 2. In order to measure the qualitative data obtained through tests carried out in comparison to earlier work, performance of modified preamplifier circuit is better on power consumption and delay with optimum offset voltage grounds.

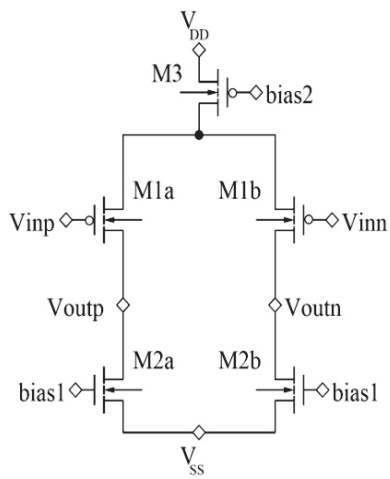

Figure 11. Preamplifier Circuit (A. Khorami & M. J. E. L. Sharifkhani, 2016) with modified aspect ratio of PMOS

RESULTS AND DISCUSSIONS

The modified preamplifier is suitable for lower frequency in oversampled ADC's applications as it consumes less power, so its sensitivity rises at the same time when the weakest signal is also detectable. In comparison of modified preamplifier with the preceding published work and (Wang et al., 2019) improved results are reflected in comparison Table 2.The modified preamplifier circuit achieves 210.345μW and 226.72 μW power consumption with 224ps and 156.036ps delay respectively at 2.67mV offset voltage and 1.2 V supply voltage which is very less among previous work carried out (Hassanpourghadi, Zamani, & Sharifkhani, 2014).

Table 1.Performance analysis with the conventional circuit

S.No.	Parameters	Conventional [1]	This work Test 1	This work Test 2
1	**Power consumed (μW)**	345.437	210.34	226.72
2	**Delay (ps)**	294.132	224	156.03
3	**V_{offset} (mV)**	2	2.67	2.67
4	**% Change in Power than Conventional [1]**	-	33.81%	34.36%
5	**% Change in Delay than Preamplifier [1]**	-	23.84%	46.96%

Table 2. Power comparison of this work with the reported and conventional circuits

S. No.	Parameter	[2]	[3]	[4]	[6] @ 65nm	[7]	Conv. [1]	This work Test 1	This work Test 2
1	**Power consumed (μW)**	420	420	230	4.14	230	345.4	210.34	226.72

CONCLUSION

In this paper, the comparative analysis has been done to understand the different types of preamplifiers which are the primary circuit part of the comparator. Moreover a small modification in the width has been performed in PMOS transistor in the preamplifier circuit in order to optimize the power consumption and delay with respect to a conventional and existing preamplifier circuits as well. The simulation is performed using virtuoso design environment by using cadence EDA. The preamplifier is implemented using 180nm CMOS technology node. The power saving of this circuit is about 46.96% when compared with the conventional circuit. Thus, modified preamplifier reflects a high speed, low offset and low power circuit is an effective application in latch-based comparator circuits significantly.

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