Optimizing CNTFET design parameters using the Taguchi method for high-performance and low-power applications

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ABSTRACT

The features of Nanotube Carbon (CNT) are fascinating to study due to their unique structural and electrical capabilities. The small structure of CNT in Field-Effect Transistor technology can produce a smaller device with a better performance. This work implemented the Taguchi method to optimize the Carbon Nanotube Field-Effect Transistor (CNTFET). The Minitab 19 software was used to carry out the Taguchi method analysis. Three design parameters (CNT's diameter, pitch, and the number of CNT) with three sizes were chosen to improve the CNTFET capabilities. L27 orthogonal array and signal-to-noise (SNR) were used to collect and analyze the data. The result from the Taguchi method was validated using ANOVA. The analysis results displayed the best combination of the three design parameters that produced the optimum performance in terms of high-power and low-power application. The most dominant design parameter that affected the CNTFET's current characteristics was the CNT diameter with 59.93%, 96.15% and 99.14% towards on-current (Ion), off-current (Ioff) and current ratio (Ion/Ioff), respectively. The device can be further optimized by identifying the most dominant structure in CNTFET. Eventually, the CNTFET devices can be enhanced in terms of high-power and low-power applications.

Keywords: Carbon Nanotube; Field-Effect Transistor; Optimization; Taguchi Method; Inverter.

INTRODUCTION

There have been numerous obstacles in developing electronic circuits due to the rapid advancement in electronics manufacturing technologies. Several nanoelectronics devices were introduced to replace Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) technology to reduce these limitations, e.g., Carbon Nanotube Field-Effect Transistor (CNTFET). CNTFET uses the Carbon Nanotube (CNT) as a channel material instead of bulk silicon like in MOSFET technology. Ijiima founded CNT in 1991. It was made of a rolled-up single-layer graphene sheet, as shown in Fig. 1.

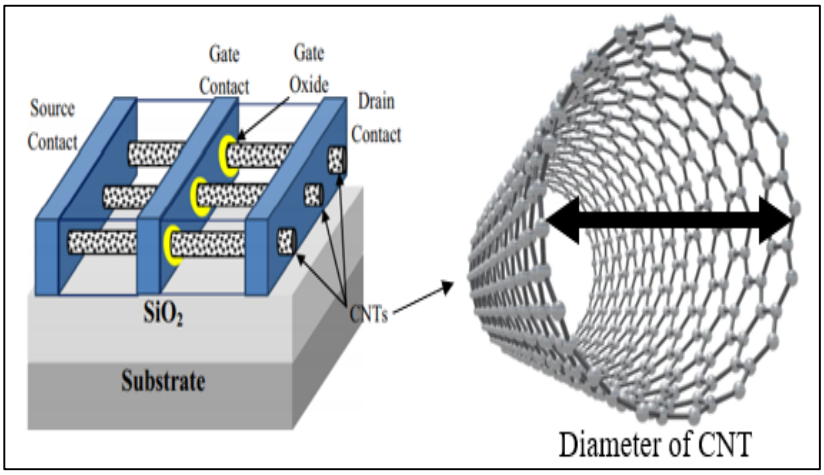

Figure 1. The structure of CNTFET (Vidu et al., 2014; Saiphani Kumar et al., 2018).

Many aspects can be improved to have an optimum CNTFET performance. One of the improvements was made by changing its geometric architecture (Shimaa, Sayed et al., 2016; Shimaa. Sayed et al., 2017; Prakash et al., 2017). Changing the CNTFET's geometric structure affected its performance.

A method to optimize the geometric structure was needed to achieve the best device performance. Shimaa. I. Sayed et al. (2016) used a trial-and-error-based search to optimize the CNTFET's design parameter. However, this technique was time-consuming because many experimental trials were set to simulate the CNTFET model. Another study by Shimaa. I. Sayed et al. (2017) used an optimization technique called Genetic Algorithm Parameter. This optimization found the best CNTFET's Power-Delay product (PDP) by varying the design parameters, such as the CNT diameter, pitch and number of CNT. Even so, this technique could not identify which design parameter significantly affected CNTFET's performance. Another optimization technique was Particle Swarm Optimization (PSO) (Monica et al., 2016) and Whale Optimization Algorithm (Prakash, Sundaram, and Bennet, 2017). Both optimization methods found the optimal design parameter for CNTFET. However, this technique was also unable to provide any information about the influence of design parameters on the CNTFET performance.

Hence, an optimization technique, i.e., Taguchi Method, was applied to find the best combination of CNTFET design parameters that provide the optimum performance in terms of Ion, Ioff and Ion/Ioff. In addition, this method can also determine the contribution factor of each CNTFET's design parameters towards the response variables (Ion, Ioff and Ion/Ioff). Therefore, the optimization process can focus on the targeted design parameter to improve performance by identifying the most significant contributing factor.

METHODOLOGY

HSPICE tools were used to simulate the Stanford University CNTFET model, as shown in Fig. 2 (Lin et al., 2009). This model can be simulated with the lowest channel length of 10 nm. The CNTFET's channel length was fixed to 32.0 nm with a metal gate of width 6.4 nm. The oxide thickness that separated the gate from the channel was set to 4.0 nm. The dielectric constant was set to K=16.

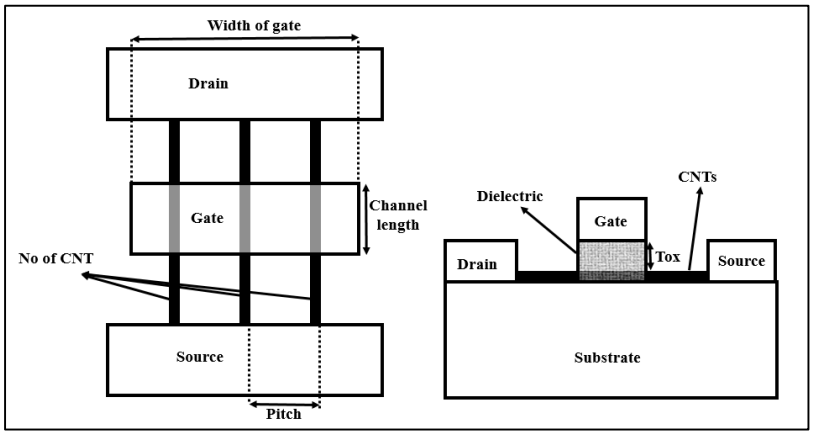

Figure 2. Structure of CNTFET and related parameters

Three parameters were chosen to optimize CNTFET performance: CNT diameter, pitch and the number of CNT in the transistor. These parameters were commonly used by previous studies to optimize CNTFET performance. The manipulated range value of CNT diameter was selected according to the previously fabricated CNTFET of 1.2 nm (Bishop et al., 2020). The pitch size was varied based on the previous simulated model by Moaiyeri et al. (2017) and Almudever et al. (2015), with 3.0 nm and 4.0 nm, respectively. Finally, the number of CNT in the transistor varied according to the previous model (Chen et al., 2007). Table 1 summarizes the model's scope.

Table 1. Device structure parameters and values

Parameters	**Fixed Values**	**Manipulated Ranged**	**References**
Diameter of CNT, nm	-	1.0-1.4	(Albert Lin et al., 2009; Bishop et al. 2020)
Pitch, nm	-	3.0-5.0	(Albert Lin et al., 2009; Moaiyeri et al., 2017; Almudever et al., 2015)
Number of CNT	-	1-5	(Albert Lin et al., 2009; Chen et al. 2007)
Channel length, nm	32.0	-	(Albert Lin et al., 2009)
Oxide thickness, nm	4.0	-	(Albert Lin et al., 2009)
Dielectric Constant, K	16	-	(Albert Lin et al., 2009)
Width of the metal gate, nm	6.4	-	(Albert Lin et al., 2009)

Fig. 3 shows the procedure for applying the Taguchi method to optimize the CNTFET design parameters and demonstrates the influence on inverter circuits for high-performance and low-power applications.

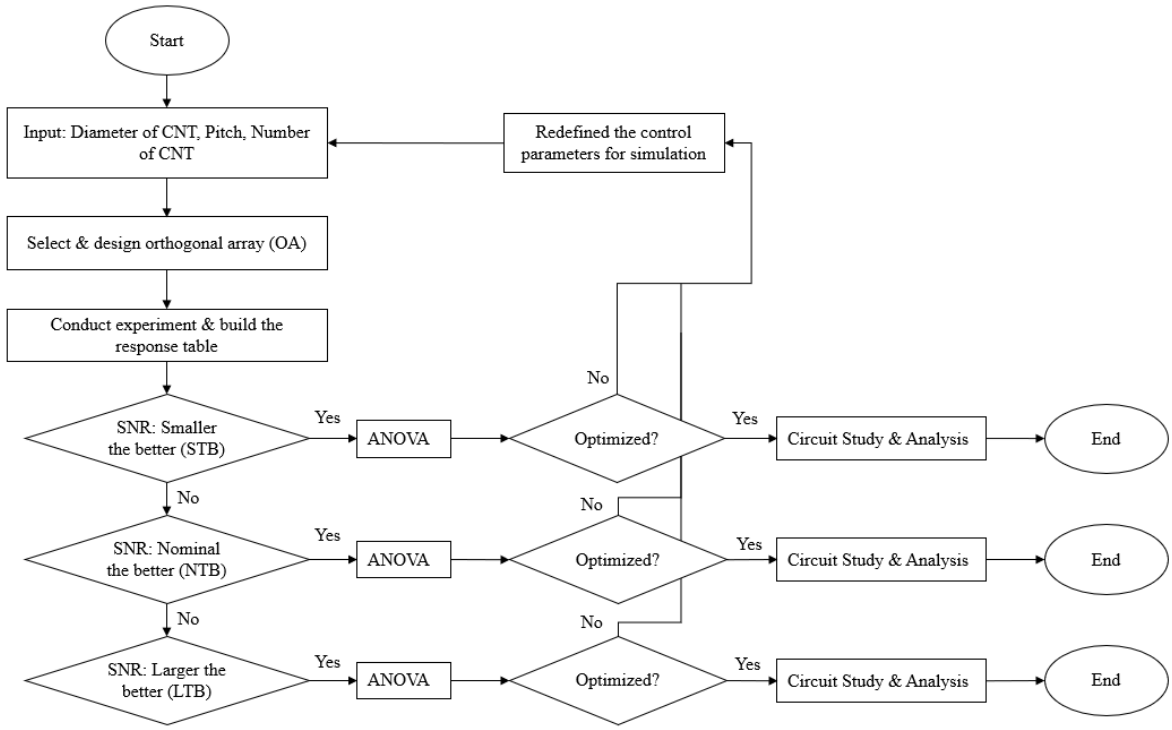

Figure 3. Block diagram for the Taguchi method.

Three parameters influencing the CNTFET performance were chosen for this simulation: CNT diameter, pitch and the number of CNT in a transistor assigned as A, B and C, as shown in Table 2. Each parameter was set into three levels: 0, 1 and 2. Level 0 defines the smallest parameter values, while level 2 is the largest.

Table 2. Experiment design for the Taguchi method

Symbol	Parameters	Level		
		0	**1**	**2**
A	Diameter of CNT, nm	1.0	1.2	1.4
B	CNT pitch, nm	3.0	4.0	5.0
C	Number of CNT	1	3	5

Taguchi Method

The Taguchi method used SNR to determine the CNTFET's quality characteristic (Ashwni et al., 2021). Three types of SNR were selected according to the response characteristic. The type of SNR is shown in Equations 1-3. If the response variable had to be maximized, the LTB was chosen. STB was chosen if the response variable had to be minimized. NTB was chosen when the target value for the response variable needs to be specified (Yusoff, 2008; Salavaravu et al., 2021). The goal for NTB is to minimize variability around the target.

Larger the better (LTB):
$$\frac{S}{N} = -10 \log \frac{1}{n}\left(\sum \frac{1}{y^2}\right) \quad (1)$$

Smaller the better (STB):
$$\frac{S}{N} = -10 \log \frac{1}{n}\left(\sum y^2\right) \quad (2)$$

Nominal the better (NTB):
$$\frac{S}{N} = 10 \log \frac{1}{n}\left(\frac{\hat{y}^2}{s_y^2}\right) \quad (3)$$

RESULTS AND DISCUSSION

The Taguchi method uses an L27 orthogonal array to simulate all parameter combinations. The orthogonal array used for the simulation included the simulated value of Ion, Ioff and the current CNTFET ratio. Only 27 experimental trials were required for the L27 orthogonal array.

Signal-to-Noise Ratio Analysis

The SNR was calculated for each response variable from the orthogonal array (Ion, Ioff & Ion/Ioff) according to its SNR type. The SNR analysis aims to select the highest SNR among the response variables. The design parameter with the highest SNR value indicates a higher signal than the noise factor and provides a better CNTFET performance.

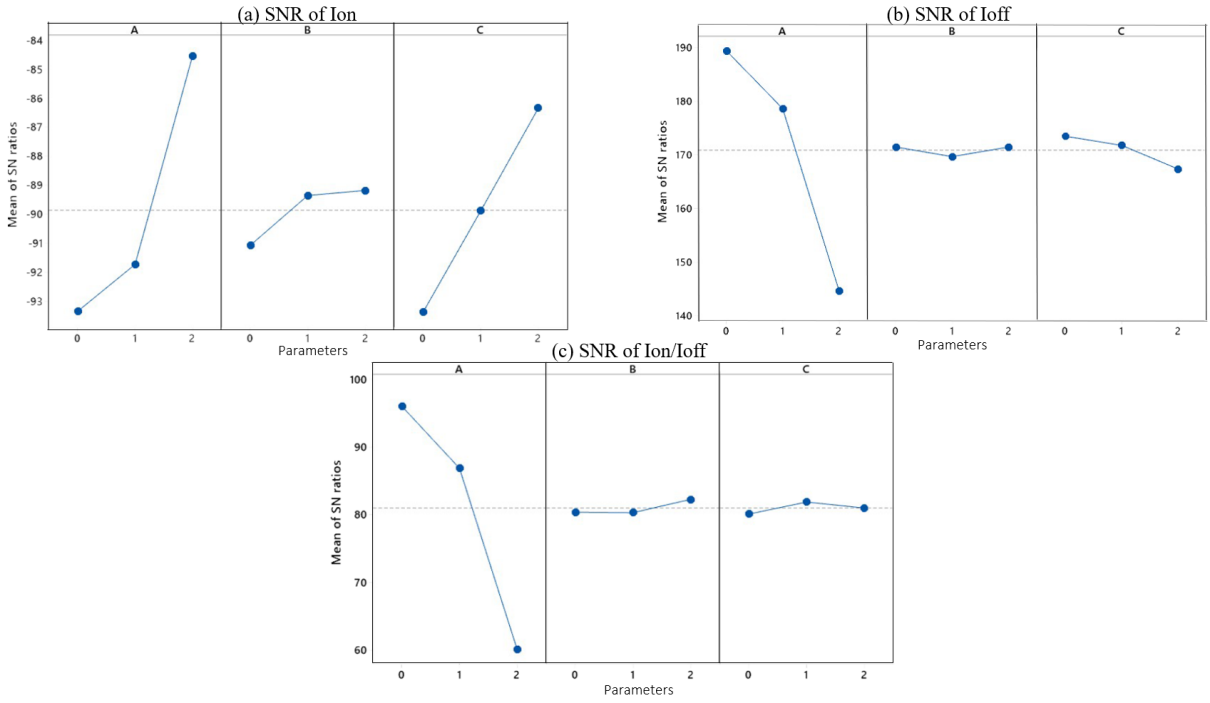

Figure 4. The result for SNR for (a) Ion, (b) Ioff, and (c) current ratio.

For Ion, the value must the highest possible to produce better CNTFET performance. The LTB SNR had to be applied for this response variable using Equation (1). The result for the SNR ratio was analyzed and plotted, as displayed in Fig. 4 (a). The A2B2C2 combination factors produced the highest Ion. This was the best combination to produce the optimum Ion for CNTFET, representing 1.4 nm of CNT diameter, 5.0 nm CNT pitch and 5 tubes in the CNTFET. The SNR graph determines the most significant process parameters towards Ion. This was calculated by observing the slope of each process parameter, which was the difference between the SNR value at the highest and lowest points. For the Ion response variable, the most significant contribution parameter is the CNT diameter, followed by the number of CNT and CNT pitches.

For Ioff, the target value had to be the lowest possible to produce better CNTFET performance. Therefore, STB SNR had to be applied using Equation (2). The result for the SNR ratio was analyzed and plotted, as displayed in Fig. 4 (b). The technique to determine the best SNR for STB was the same as LTB, where the larger SNR between the parameters was chosen. The A0B0C0 combination factors produced the lowest Ioff, representing the 1.0 nm of CNT diameter, 3.0 nm of CNT pitch, and 1 tube in the CNTFET. The highest value difference between the SNR at the slope's highest and lowest points is the CNT diameter, followed by the number of CNT and CNT pitches, indicating that the CNTFET Ioff was influenced the most by the CNT diameter.

A similar method was applied for the Ion/Ioff ratio performance to determine the best parameter combination for CNTFET. The Ion/Ioff ratio had to be high enough to perform better. Hence, LTB SNR was chosen. The A0B2C1 combination factors produced the optimum Ion/Ioff ratio performance, as displayed in Fig. 4 (c), representing the 1.0 nm of CNT diameter, 5.0 nm of CNT pitch, and 3 tubes in the CNTFET. The most significant contribution was the CNT diameter, followed by CNT pitch and the number of CNT in the CNTFET.

The best combination for each response variable was determined by applying the Taguchi method. However, the relative significance of the process parameter towards each response variable had to be validated. The next section explains the validating process using ANOVA.

Analysis of Variance (ANOVA)

ANOVA was conducted to determine the most significant process parameter for the response variables. For this study, the F-ratio was 95% of confidence level. Table 3 shows the ANOVA results for Ion. Factor A (CNT diameter) and factor C (number of CNT) were the most dominant process parameters that influenced Ion due to their highest factor effect on SNR, 59.93% and 33.81%, respectively. On the other hand, factor B (CNT pitch) had a less significant influence, with a 2.99% contribution. This result corresponds to the previous SNR analysis for Ion in Section 3.1.

Table 4 shows the ANOVA results for Ioff. The CNT diameter greatly affects the Ioff performance by contributing a 96.15% factor effect on SNR, followed by factor C (number of CNT) and factor B (CNT pitch) with a factor effect on SNR 1.78% and 0.19%, respectively. This ANOVA result fits the previous SNR analysis for Ioff in Section 3.1. The CNT diameter had to be small to achieve the lowest value of Ioff.

Table 3. ANOVA for Ion

Source	**DF**	**Seq SS**	**Contribution**	**Adj SS**	**Adj MS**	**F-Value**	**P-Value**
A	2	5.2487	59.93%	5.2487	2.62435	183.26	0
B	2	0.2615	2.99%	0.2615	0.13076	9.13	0.002
C	2	2.9611	33.81%	2.9611	1.48057	103.39	0
Error	20	0.2864	3.27%	0.2864	0.01432		
Total	26	8.7578	100.00%				

Table 4. ANOVA for Ioff

Source	DF	Seq SS	Contribution	Adj SS	Adj MS	F-Value	P-Value
A	2	130.209	96.15%	130.209	65.1047	510.97	0
B	2	0.255	0.19%	0.255	0.1276	1	0.385
C	2	2.413	1.78%	2.413	1.2064	9.47	0.001
Error	20	2.548	1.88%	2.548	0.1274		
Total	26	135.426	100.00%				

Table 5. ANOVA for Ion/Ioff

Source	DF	Seq SS	Contribution	Adj SS	Adj MS	F-Value	P-Value
A	2	0.030708	99.14%	0.030708	0.015354	1949.39	0
B	2	0.000075	0.24%	0.000075	0.000038	4.78	0.02
C	2	0.000034	0.11%	0.000034	0.000017	2.13	0.145
Error	20	0.000158	0.51%	0.000158	0.000008		
Total	26	0.030974	100.00%				

Table 5 shows the ANOVA result for Ion/Ioff. Similar to the results for Ioff, the CNT diameter contributes the most to the Ion/Ioff ratio performance with a 99.14% factor effect on SNR. On the other hand, the CNT pitch and the CNT number were less significant, with 0.24% and 0.11% contributions, respectively. This result corresponds to the previous SNR analysis for Ion/Ioff in Section 3.1. Therefore, based on the three response variables, it can be deduced that the CNT diameter greatly affects the CNTFET performance. Therefore, to optimize the CNTFET design parameter, the CNT diameter is an essential variable.

Electrical Characterization of CNTFET

Two data analysis techniques were used to optimize and validate CNTFET: the Taguchi method and ANOVA. Both techniques produce the same results regarding the parameters that affected the on-current, off-current and current ratio the most. Moreover, a preferable value for the CNTFET response variable can be achieved according to the type of SNR using the Taguchi method.

This response variable used SNR LTB for the on-current performance to achieve a higher value when the CNTFET design parameters had been optimized. Fig. 5 shows that the on-current of the optimized CNTFET was enhanced. Table 6 shows that the on-current increases from 57.9 uA to 110 uA. A higher on-current produced a higher-performance device. The Ion of the optimized CNTFET is also higher than the previous model, but the value is still far from ITRS 2022, which is 912 uA (Moaiyeri et al., 2017**;** IEEE 2020).

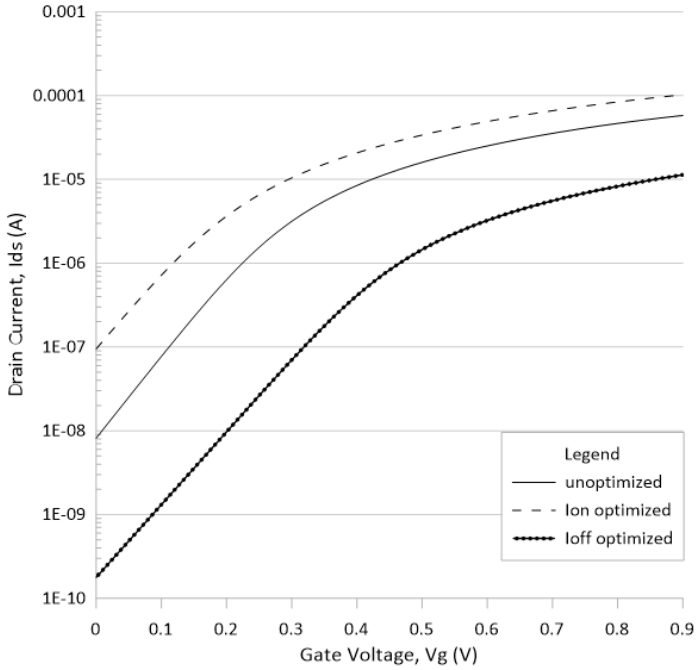

Figure 5. IV characteristics to compare the unoptimized CNTFET and optimized CNTFET

Table 6. Comparison between the unoptimized CNTFET and optimized CNTFET according to each response variable

	Unoptimized CNTFET	**Optimized CNTFET (Ion)**	**Optimized CNTFET (Ioff)**	**Optimized CNTFET (Ion/Ioff)**	**32nm** (Moaiyeri et al., 2017)	**ITRS 2022-High Performance** (IEEE 2020)
Ion (uA)	57.9	110.00			97	912
Ioff (uA)	0.00816		0.000178		0.006	0.01
Ion/Ioff	7100			87982.03	16166.7	91200.0

For off-current performance, the response variable used STB SNR to achieve a lower value when the CNTFET design parameters had been optimized. Fig. 5 shows that the off-current of the optimized CNTFET was enhanced. As a result, the off-current decreased from 0.00816 uA to 0.000178 uA, as shown in Table 6. The Ioff value of the optimized CNTFET is also lower than the previous model (Moaiyeri et al., 2017). An Ioff can produce a better low-power device. A higher ratio value is preferable to produce a faster switching device. This response variable used the same SNR type as on-current, i.e., LTB, to achieve a higher ratio value. Based on the result, the current ratio of the optimized CNTFET increased compared to the unoptimized design parameters. Table 6 shows that the current ratio increases from 7100 to 87982.029. The current ratio, optimized using the Taguchi method, surpassed the previous CNTFET model stated in Table 6. However, the current ratio of the optimized CNTFET was only 3.6% less than the current ratio set by ITRS 2022 (IEEE 2020). Using the Taguchi method as an optimization process, the CNTFET can be designed for better performance.

Application of the CNTFET in High-Performance and Low-Power Applications

For high-performance applications, the CNTFET with optimized Ion was chosen for use in the inverter circuit. Maintaining the highest Ion value at a higher switching rate activity for the CNTFET inverter was essential (Ali Usmani and Hasan, 2010; Rongtian Zhang et al., 2001). By choosing the CNTFET with high Ion, the CNTFET power consumption inverter increases, as shown in Table 7.

Table 7. CNTFET circuit study analysis for high-performance and low-power application

	Delay (ps)		**Average Power (uW)**	
	Unoptimized CNTFET	**Optimized CNTFET**	**Unoptimized CNTFET**	**Optimized CNTFET**
High Performance Application	2.8179	2.4484 (13% delay reduction)	1.1840	1.4961
Low Power Application		6.2416		1.0074 (15% average power reduction)

This is the drawback encountered by the CNTFET inverter for a high-performance application. For the low-power device application, the CNTFET with the optimized Ioff was chosen for the inverter circuit. Since the low-power application is usually used in a portable electronic device, the power consumption must be at the lowest possible. Hence, it is important to keep Ioff small to minimize the power that a circuit consumes when it is in standby mode (Hu, 2009). For this experiment, the power consumption of the optimized CNTFET inverter was reduced from 1.1840 uW to 1.0074 uW. However, reducing the average power consumption increased the delay of the optimized CNTFET inverter, as shown in Table 7.

CONCLUSION

This paper uses the Taguchi method and ANOVA to present an optimized CNTFET design regarding on-current, off-current and current ratio performance. The performance analysis depended on the device geometry design, especially the CNT diameter, by more than 50% based on the ANOVA result for the three response variables. The following Ion parameters were optimal for current trade-offs: 1.4 nm of CNT diameter, 5.0 nm of CNT pitch, and 5 tubes in the CNTFET. Since higher Ion resulted in a shorter delay, applying it to a high-performance device was best. The following are the best parameters to improve Ioff performance: 1.0 nm of CNT diameter, 3.0 nm of CNT pitch and 1 tube in the CNTFET. A lower Ioff transistor was best applied in a low-power device because it consumes less power. The following parameters improved performance for the current trade-offs and ratio: 1.0 nm of CNT diameter, 5.0 nm of CNT pitch and 3 tubes in the CNTFET. In conclusion, the Taguchi method optimization is important in designing the next technology node to achieve continuous transistor scaling development.

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