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Performance Analysis of Charge Plasma Induced Graded Channel Si Nanotube

Ashima *, Vaithiyanathan Dhandapani* and Balwinder Raj**

**Department of Electronics and Communication Engineering, National Institute of Technology Delhi, India*
***Department of Electronics and Communication Engineering, National Institute of Technical Teachers Training and Research, Chandigargh, India.*
Corresponding author: ashima@nitdelhi.ac.in

ABSTRACT

This paper investigates a comparison based on DC and AC analysis of a charge plasma-based graded channel nanotube in two configurations. Nanotube structures offer enhanced gate ctontrol over other devices, they offer higher on-current than nanowires of equivalent silicon film thickness, making them a promising device, however, the core gate of nanotube results in higher gate leakages also. This paper draws a comparison of the two possible configurations of making a graded channel without ion implantation. The results show that a gate of higher work function in S-GC-NTFET is necessary to bring the same subthreshold characteristics as D-GC-NTFET. The D configuration shows slightly enhanced DC characteristics however, the RF analysis shows better results for S configuration.

Keywords: Graded channel; Nanotube; Nanowires; Charge plasma.

INTRODUCTION

Recent years are witnessing increasing researches in the field of nanoscale device engineering (Kuhn, K.J., 2012, Colinge, J.P., Lee, C.W., Afzalian, A., Akhavan, N.D., Yan, R., Ferain, I., Razavi, P., O'neill, B., Blake, A., White, M. and Kelleher, A.M., 2010 & Singh, S. and Raj, B., 2020). The era of smart devices has presented a need for more sophisticated devices in terms of size, speed, and power consumption. On the other hand, scaling trends are facing several issues, predominantly classified as short channel effects (SCEs). Nanotubes and Nanowires as devices are studied extensively because of their efficient gate control, with the former having a core gate that increases the tunnelling width at the channel-drain interface and also the source to channel barrier height resulting in an increased Ion (Sahay, S. and Kumar, M.J., 2017, Sahay, S. and Kumar, M.J., 2017 & Tayal, S. and Nandi, A., 2017). Nanotubes are nanowire like Gate-all-around (GAA) cylindrical structures with an inner core gate that can be present as per different configurations covering source-channel, channel-drain, or symmetric source-drain. Structures with core gate covering channel and drain regions have reported better results in terms of reduced Cgg(overall gate capacitance), ft(cut-off frequency), and intrinsic gain in comparison to its counterparts (Tekleab, D., 2014, Fahad, H.M., Smith, C.E., Rojas, J.P. and Hussain, M.M., 2011, Tan, C.M. and Chen, X., 2014 & Fahad, H.M. and Hussain, M.M., 2012).

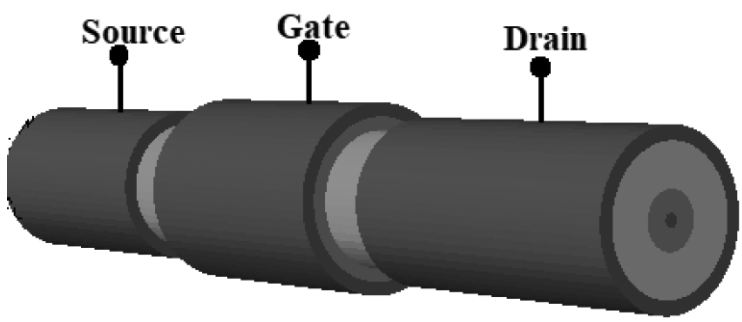
The study of channel engineered nanotubes can exhibit enhanced device performance by suppression of SCEs (Pratap, Y., Gautam, R., Haldar, S., Gupta, R.S. and Gupta, M., 2016, Baral, K., Singh, P.K., Kumar, S., Chander, S. and Jit, S., 2020 & Sahay, S. and Kumar, M.J., 2016). Graded Channel technique is applied to devices in both lateral as well as vertical fashion (14-17 Shan, C., Wang, Y. and Bao, M.T., 2016, Saib, S.S., Yadav, S., Rahul, J., Srivastava, A. and Raj, B., 2015, Chen, Y., Mohamed, M., Jo, M., Ravaioli, U. and Xu, R., 2013 & Pathak, V. and Saini, G., 2018). A gradual change in the doping concentration is seen to increase the on current, consequently enhancing the Ion/Ioff ratio. Despite the evident advantages realizing a graded profile becomes cumbersome with the increasing scalability at 10-20nm technology nodes. The fabrication

procedure for the graded channel involves ion implantation or epitaxial growth which gives rise to an added complexity. To avoid the undue higher thermal budgets owing to the added requirement of ion-implantation, "charge-plasma" concept can be utilized (Sahu, C. and Singh, J., 2014). Charge plasma concept has been applied to BJTs, MOSFETs, Nanowire structures in which instead of using ion implantation to produce the required doping. According to this technique, with a metal of suitable work function, electrons and holes can be artificially induced.

In this work, graded channel technique has been implemented in two different ways- by applying charge plasma concept over channel-drain Graded Channel Nanotube FET (D-GC-NTFET) or over source-channel (S-GC-NTFET). We have compared both the configurations by studying its impact on various performance metrics. In the following sections: Section 2 gives the device design and parameters of simulation. Section 3 discusses the results obtained with the conclusion being finally laid in section 4.

DEVICE DESIGN AND PARAMETERS FOR SIMULATION

Figure 1 shows the 3D and cross-sectional views of the S- and D-GC-NTFET. The inner gate contact is kept in the drain side and is set small to minimize the miller capacitance. The parameters used for both configurations are similar and are discussed in Table 1. To induce n+ region over silicon, the metal's work function over the desired region should be lesser than that of Si, and also the thickness of Si should not exceed the Debye length. To fulfil the criteria's metal and Hafnium is used having a work function of 3.9eV at S/D contact over a silicon body of width 10nm.



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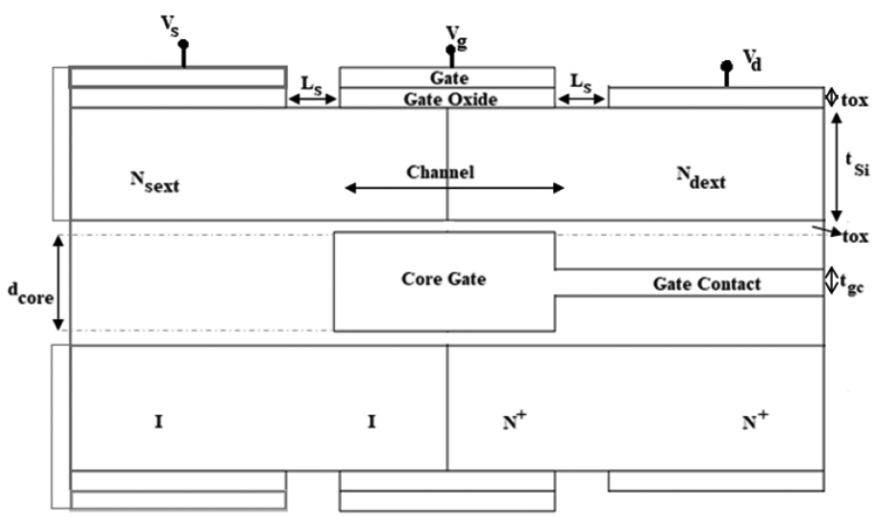

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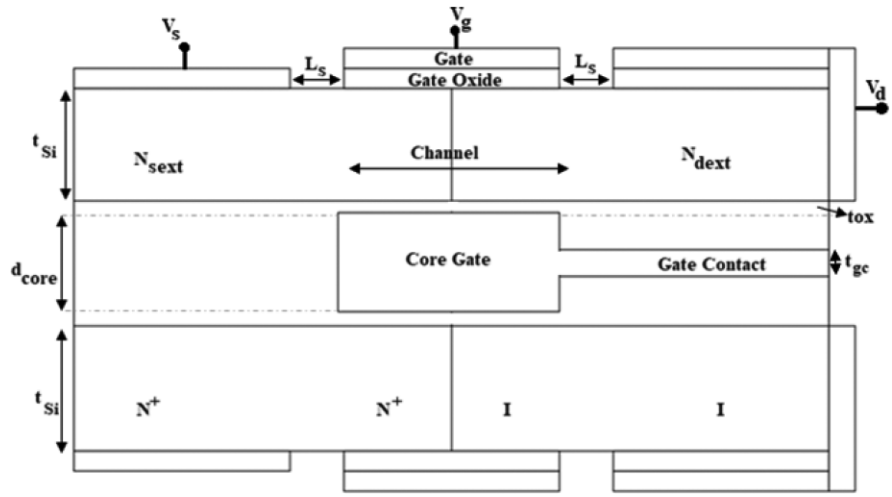


(c)

Fig. 1. (a) 3-D view of GC-NTFET and cross-sectional views of (b) S-GC-NTFET & (c) D-GC-NTFET

Gate work functions of 5.25 and 5eV have been applied in S- and D-GC-NTFET to maintain the threshold voltage for a fair comparison of the characteristics (Sharma, S.K., Jain, A. and Raj, B., 2018, Kumar, S. and Raj, B., 2016 & Jain, A.K., Singh, J. and Kumar, M.J., 2019). Quantum confinement effects were ignored as Si thickness used is greater than 7 nm (Ashima, Vaithiyanathan, D. and Raj, B., 2020).

Silvaco Atlas 3D device simulator TCAD has been used to perform the 3D simulations (ATLAS Device Simulator Software, Silvaco, Santa Clara, CA, USA, 2012). Various models invoked for the simulation set up are nonlocal BTBT to include the L-BTBT incurred at channel-drain junction, Lombardi for the mobility degradations, FLDMOB was included to model any velocity saturation. In addition Shockley-Read-Hall, Auger recombination, Concentration dependent mobility model, Fermi Dirac were also included[17].

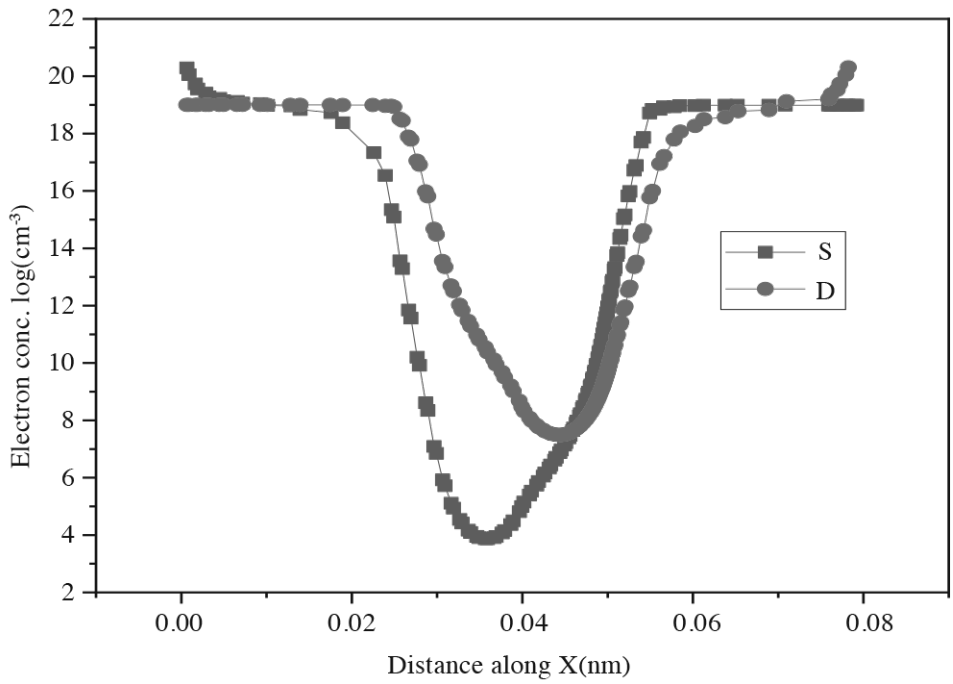
Table 1. Device Parameters

Parameter	S-GC-NTFET	D-GC-NTFET
Diameter of core gate(d_{core})	20 nm	20 nm
Gate contact width (t_{gc})	5nm	5nm
Gate oxide thickness, Sio_2 (t_{ox})	1nm	1nm
Silicon thickness (t_{Si})	10nm	10nm
Gate Workfunction	5.25eV	5eV
Source +1/2 Channel Doping	$1e15cm^{-3}$	$1e19cm^{-3}$
Drain+1/2 Channel Doping	$1e19cm^{-3}$	$1e15cm^{-3}$

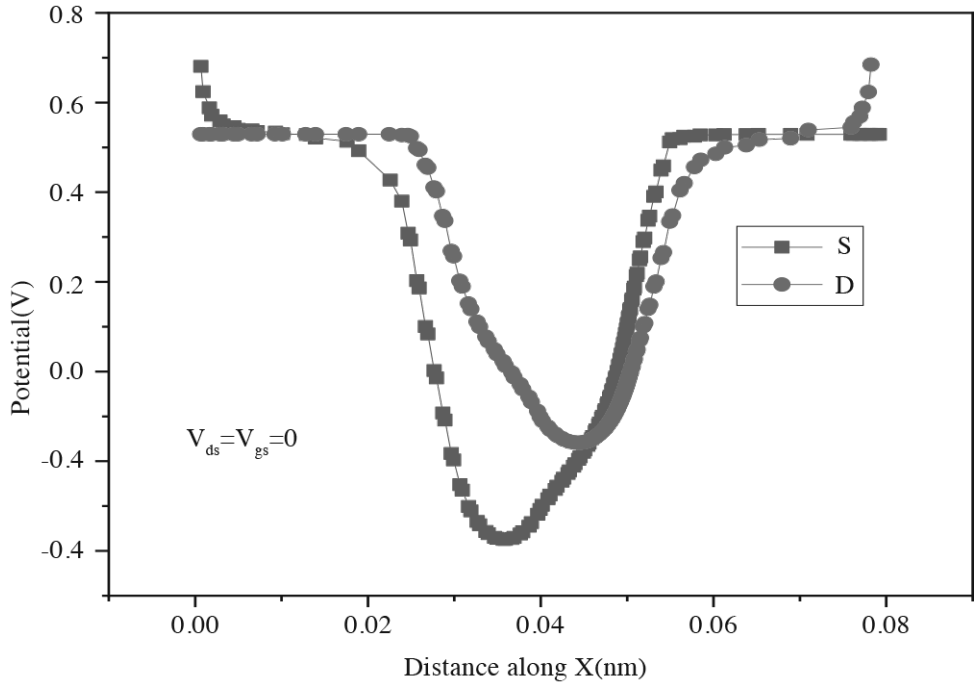
RESULTS AND ANALYSIS

3.1 Electron, Potential and Electric Field Distributions

In this segment, we evaluate the performance of the graded channel in its two configurations. First we compare the device behaviour in an equilibrium state (Vgs=0, Vds=0) for which electron concentration and potential have been extracted along the channel direction with a cutline drawn 1nm below the outer gate oxide and silicon interface. The gate length is kept constant throughout at 20nm extending from 31nm to 51nm. Fig. 2 shows the electron concentration in both the devices. The electron concentration and potential both have an abruptness in both the cases at the center of the channel expanse because of the transition in the doping however the D-GC-NTFET shows higher values of electron conc. throughout the channel region. The region in which the electron concentration is less than the doping signifies the depletion region extension in source/drain of the device. The length of extension region signifies a longer effective channel length (Leff) of the device which helps in combating the SCEs[6].



(a)



(b)

Fig. 2. (a) Electron Concentration and (b) Electrostatic Potential along the direction of the channel for S-, D-GC-NTFET in thermal equilibrium

Electric field distributions have been analyzed along the channel in Fig. 3. Hot carrier degradations (HCDs) are predominant in FET devices because of drain voltage induced high electric fields near the drain region. D-GC-NTFET shows lower electric field distribution near the drain end which helps minimize these HCDs in the on state of the device. Also, we notice small supplementary peaks in the center of the channel expanse because of the graded doping profile that aids the electron velocity in the channel.

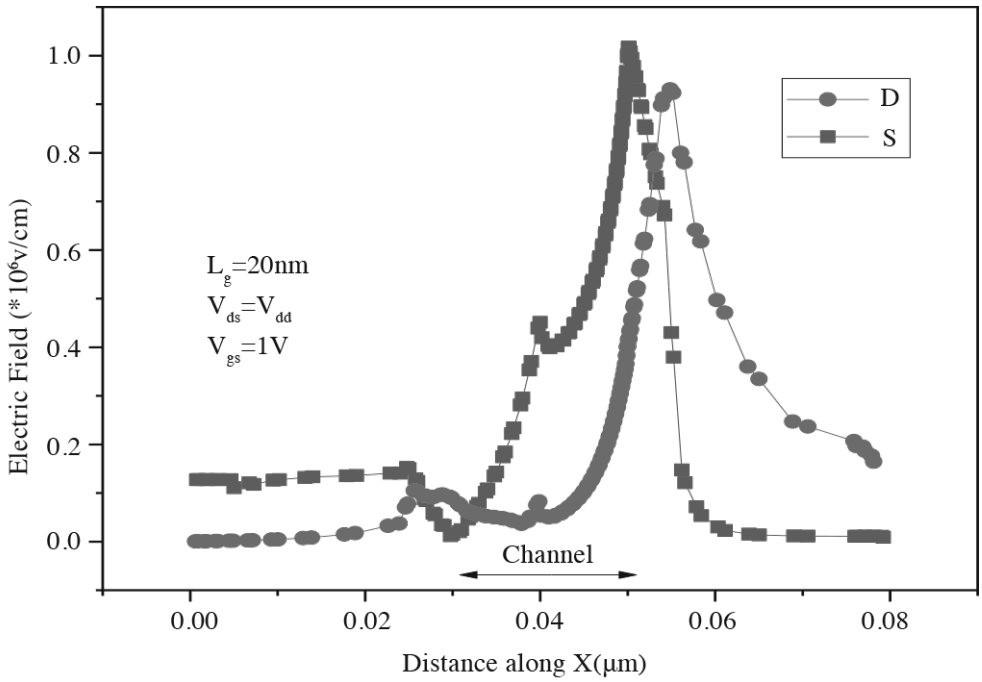


Fig. 3. Electric field distribution along the device length for both configurations in on-state

3.2 DC and Analog Characteristics

Figure 4 illustrates the transfer characteristics of both the configurations at Vds=1V. The Vth of both the configurations has been matched in order to make a valid comparison. The Vth has been calculated using the constant current extraction technique at current value of 10¬-7A. The S-GC-NTFET configuration requires a higher work function of 5.25 eV than D-configuration. The on current of S-GC-NTFET is less because of the presence of an intrinsic region near the channel which acts as a barrier and degrades the on current. The off current in NTFET structures is attributed to L-BTBT because of the channel and drain band overlapping. The Sub-threshold slope for the S and D configurations is 67.4261mV/decade and 66.3504mV/decade respectively.

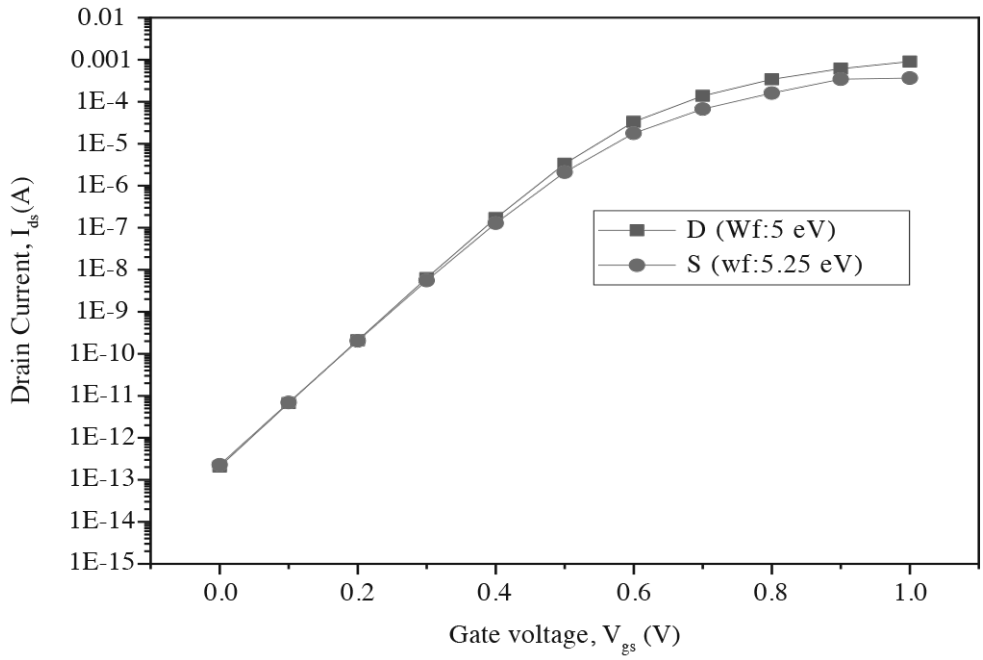


Fig. 4. Transfer Characteristics of D and S configurations at gate work functions 5 and 5.25 eV respectively

RF parameters such as transconductance (gm), transconductance efficiency, total gate capacitance (Cgg), output conductance (GD), Early Voltage (VEA), and cut-off frequency (fT) of both configurations have been explored at a frequency of 1MHz. Transconductance (gm) of a device denotes its sensitivity, it is depicted as change in drain current to change in Vgs. S- and D-GC-NTFET both configurations show increasing values of gm however, the latter has a higher value. As per Fig. 5(a), the course of gm involves its value to first increase and then decrease due to mobility degradation. Transconductance efficiency, as shown in 5(b) denotes the efficacy of the device to convert DC power to AC frequency. The high value in curve denotes weak inversion for lower gate voltages and high inversion for higher gate voltage.

Total gate capacitance is denoted by Cgg and is a combination of Cgs and Cgd as shown in Fig. 6. The S configuration depicts a reduced Cgg .Due to the accumulation effects the device exhibits an increasing Cgg till flat band voltage (Vfb) after which it becomes unvarying. In Fig. 7(a), GD of both the configurations descends after Vds of 0.4V this is due to the graded channel profile. It is ratio of change in Ids and Vds. The D configuration has higher GD because of its higher on current as depicted in Fig. 4. V¬EA Early voltage = Ids/ GD of both configurations has been compared in the Fig. 7(b), the higher values of GD result in lower VEA for D-GC-NTFET. Finally in Fig. 8 cut-off frequency has been compared ft=gm/2πCgg. Cgg of the D configuration is higher by an order as compared to the S-GC-NTFET hence S configurations shows higher ft.

CONCLUSION

In this paper, a new approach to create a graded channel for NTFET is presented and compared based on its two configurations possible. The comparison of charge plasma induced source-, drain based graded channel engineered NTFETs have been investigated through extensive 3D TCAD simulations. D-GC-NTFET shows a higher on current due to low electric field at the drain terminal and also higher gm but it shows a deteriorated value of Cgg and ft. For D configuration Cgd is highly increased due to presence of inner gate and metal deposited for the creation of charge plasma at drain side in D-GC-NTFET. S configuration has a lower Cgg which provides a better gate control over the channel and reduces parasitic oscillations in RF circuits. High frequency parameter ft is crucial

for determining circuit level utility of the device, S-GC-NTFET compensates for lower gm by having a even lower Cgg and hence a higher ft. Hence, S-GC-NTFET is a preferable configuration for high frequency circuits as the cost of slight reduction in the Ion current..

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