مجلة فصلية أكاديمية
محكّمة تعنى بنشر البحوث
والدراسات القانونية والشرعية

مجلة الحقوق

تصدر عن مجلس النشر العلمي - جامعة الكويت

صدر العدد الأول في
يناير ١٩٧٧

الاشتراكات

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المراسلات

توجه جميع المراسلات إلى رئيس التحرير على العنوان الآتي:
مجلة الحقوق - جامعة الكويت ص.ب: ٦٤٩٨٥ الشويخ - ب 70460 الكويت
تلفون: ٢٤٨٣٥٧٨٩ - ٢٤٨٤٧٨١٤ فاكس: ٢٤٨٣١١٤٣
E.mail: jol@ku.edu.kw

عنوان المجلة في شبكة الإنترنت http://www.pubcouncil.kuniv.edu.kw/jol

ISSN 1029 - 6069

Journal of Engg. Research Vol. 2 - (2) June 2014 pp. 63 - 80

تصميم جوامع رقمية معلمة ، سالبة الثنائية وباستقطاب مشفّر ضوئي وذلك بإستعمال مفاتيح مزيلة التضاعف – غير متماثلة وضوئية بالكامل بموجات التراهرتز

عبدالله شري، نبيل خشاب و علي حاجيه

جامعة الكويت ، كلية الهندسة والبترول ، قسم الهندسة الكهربائية

ص.ب 5969 الصفاة 13060 الكويت

خلاصة

هذه المقالة تتقدم بتصميم جديد لجوامع ضوئية بإستخدام نظام تشفير استقطابي . وهذا النظام هو عكس التمثيل العددي للأرقام المعلمة السالبة والتي تعتمد على تشفير شدة الضوء.

وبإستعمال هذه الطريقة المقترحة للتشفير الإستقطابي ينتج عنها دوائر ذات فعالية أكبر من حيث تقليل عدد البوابات المستعملة وتقليل الإعاقة في الدوائر .

في هذه المقالة نقترح ثلاث جوامع ضوئية بالكامل بإستعمال مفرق شعاع إستقطابي ومغير الاستقطاب وموحد الشعاع . والنتائج تظهر بأن الدوائر المقترحة تقلل نسبة عدد البوابات بـ 51.7 % و 45.5 % و 21 % . وتزيد سرعتها بنسبة 44.4 % و 42.9 % و 40 % بالمقارنة مع الدوائر التي تعتمد تشفير شدة الضوء .

All-optical polarization-encoded negabinary signed-digit adder designs using terahertz-optical-asymmetric-demultiplexer switches

A. K. CHERRI*, N. I. KHACHAB AND A. T. HAJJIAH

Kuwait University, College of Engineering & Petroleum, Department of Electrical Engineering, P. O. Box 5969, Safat 13060; Kuwait. Tel: 965 2498 7367, Fax: 965 2481 7451
E-mails: abdallah.cherri@ku.edu.kw ; nabil.khachab@ku.edu.kw; ali.hajjiah@ku.edu.kw.
** Corresponding Author*

ABSTRACT

In contrast to intensity-encoded negabinary modified signed-digit number representation, a polarization-encoding scheme is proposed to design all-optical adders. The utilization of the proposed polarization-encoding produces more efficient circuits in terms of gates numbers and circuit delays. Three all-optical adder circuits are designed using Terahertz-Optical-Asymmetric-Demultiplexer (TOAD) switches, polarization beam splitters, polarization converters, and beam combiners. It will be shown that the proposed circuits utilize 51.7%, 45.5%, and 21% less gates and they are faster by 44.4%, 42.9%, and 40%, respectively, than the corresponding intensity-encoded circuits.

Keywords: All-optical gates; intensity-encoding; negabinary signed-digit; polarization-encoding; terahertz-optical-asymmetric-demultiplexer.

INTRODUCTION

The desire to reach tremendous operation speed in the terahertz range geared researchers towards developing new optical devices. Owing to the benefits that photonics devices offer over its electronics counterparts, ultra response is promising along with huge increase in capacity (Mehra *et al.*, 2012; Li *et al.*, 2007; Stubkjaer, 2000; Schreicek *et al.*, 2002; Vlachos *et al.*, 2003). In the last decade and due to recent development in nonlinear optical materials, works and interests on optical computing have increased (Gosh *et al.*, 2012; Gayen *et al.*, 2011). In this regard, many researchers are exploring all-optical implementations for optical computing to avoid or eliminate the need to convert the optical signals to electronics signals and back to optical signals (Gayen *et al.*, 2011). This is possible based on the nonlinear interaction of light waves with switching capability of more than 100 GHz (Mehra *et al.*, 2012). For instance, various schemes such as ultra-fast nonlinear interferometric and interferometric wavelength converters (Garai & Mukhopadhyay , 2010), semiconductor optical amplifier (SOA)

waveguide based on a Michelson interferometer (Wang *et al.*, 2006), and Mach-Zehnder interferometric (MZI) (Zhang *et al.*, 2003) were reported. Further, optical gates based on terahertz optical asymmetric demultiplexing (TOAD) including SOA as the nonlinear element have attracted many interests due to its practical advantages (Li *et al.*, 2007; Gayan *et al.*, 2011; Dimitiadou & Zoiros, 2012). Attractive features of TOAD switches such as the extremely high operational speed, tremendous potential for integration with a wide variety of active and passive components, low power consumption, and high stability motivates researchers to realize various all-optical logic operations such as XOR, OR, and NOR as well as arithmetic operations (Kim *et al.*, 2006; Gayen & Roy, 2008; Roy & Gayen, 2007).

In optical information processing and computing, intensity encoding scheme is used to represent the optical digits. Another encoding technique is wavelength or frequency encoding. Utilizing the polarization state of light is another alternative to represent the optical information.

On the other hand, an arithmetic optical computing system is more efficient when a non binary number representation is utilized to avoid the long carry/borrow bit propagation paths that exist during the binary arithmetic operations (Cherri, 1998; Chattopadhyay *et al.*, 2009; Al-zayed & Cherri, 2010; Song & Yan, 2012). Examples of some non binary number representation are the multiple-valued number and the redundant signed-digit number, which permit parallel arithmetic operations. In this regard, another competitive number representation system referred to as negabinary uses a negative base to handle bipolar data (Zohar, 1970; Zhang & Karim, 1998). Negabinary number representation was proposed to implement optical linear algebra processors-OLAP (Perlee & Casasent, 1986), optical complex matrix operation (Li *et al.*, 1994), optical one step adder (Zhang & Karim, 1998), and optical modular multiplication (Li *et al.*, 1999). Due to its redundancy, the NMSD has the potential to be used in implementing fast VLSI multipliers and dividers (Lakshmi & Dhar, 2011; Jaberipur & Parhami, 2008).

The negabinary number system, which uses radix $r = (-2)$ as the base allows parallel operations at each digit position and thus, these operations are space-invariant. The original negabinary number system was recently improved to handle signed-digit (Li *et al.*, 1999; Cherri & Kamal, 2004; Cherri, 2011) and is called negabinary modified signed-digit (NMSD). Both optoelectronics as well as all-optical implementations were reported. The all-optical implementation using MZI and the NMSD digits were encoded using intensity states of light. In this paper, TOAD switches along with the parallel NMSD number representation are utilized to design and realize more efficient all-optical arithmetic circuits using polarization-ending schemes for the NMSD digits. Three all-optical adder circuits are designed using TOAD switches, polarization beam splitters, polarization converters, and beam combiners. It will be shown that the three proposed circuits utilize much less gates and they are much faster than the

corresponding intensity-encoded adders. Design details for the proposed circuits are presented, where two-bit polarization-encoding scheme for each trinary NMSD digit is employed in order to fully utilize the switching property of the TOAD. The rest of the paper is organized as follows. Sections 2 and 3 briefly introduce the NMSD number system and the operation of the TOAD switch. Section 4 details the three proposed adder designs. Section 5 summarizes the results.

MODIFIED NEGABINARY SIGNED-DIGIT NUMBER

Originally, an n-bits negabinary number representation of a decimal number $\boldsymbol{B}$ is expressed as $B = \sum_{j=0}^{n-1} b_j (-2)^j$ with b_j is being logic '0' or '1'. The representation uniquely represents the decimal number $\boldsymbol{B}$. When adding/subtracting two negabinary numbers $\boldsymbol{A}$ and $\boldsymbol{B}$, carry bits may propagate from the lower significant bit all the way to the most significant bit position (Perlee & Casasent, 1986; Li *et al.*, 1994). If twin carries to the next higher bits are allowed, then the carry propagation is restricted only to the next bit. Recently, we have introduced signed carries; i. e. negative as well as positive carries (Cherri & Kamal, 2004) to restrict the carry propagation process to only two neighbouring digit positions. Thus, the negabinary number representation was extended and referred to as negabinary modified signed-digit (NMSD) where the decimal number $\boldsymbol{B}$ is expressed as $B = \sum_{j=0}^{n-1} b_j (-2)^j$ and b_j belongs to the set $\{1, 0, \bar{1}\}$ where $\bar{1}$ denotes -1. This forces the NMSD to be a redundant number representation. For instance, $(6)_{10}$ can be represented as $[\bar{1}\,010]_{NMSD}$ or as $[\bar{1}\,010]_{NMSD}$ and $(-6)_{10} = [10\,\bar{1}\,0]_{NMSD}$ or equivalently as $[0\,\bar{1}\,10]_{NMSD}$. Note that a negative NMSD number is the NMSD complement of its positive number. Further, the addition rules of two NMSD numbers $\boldsymbol{A}$ and $\boldsymbol{B}$ are governed by the following three equations which generate three-step rules as shown in Figure 1 and Table 1 (Cherri & Kamal, 2004; Cherri, 2011):

$$\begin{aligned} Step1 \Rightarrow \quad & a_i + b_i = (-2)T_{i+1} + W_i \\ Step2 \Rightarrow \quad & T_i + W_i = (-2)T'_{i+1} + W'_i \\ Step3 \Rightarrow \quad & S_i = T'_i + W'_i \end{aligned}$$

Note that Table 1 includes polarization-encoding for the NMSD digits that will be explained later. The first step generates intermediate transfer (T_{i+1}) and weight (W_i) digits whereas the second step produces second intermediate transfer (T'_{i+1}) and weight (W'_i) digits. Finally, the third step is applied to produce the resulting sum digits. The following example illustrates the addition rules of the NMSD representation:

		1	$\bar{1}$	$\bar{1}$	1	0	(18)10
		$\bar{1}$	$\bar{1}$	0	1	1	(-9)10
	0	1	1	$\bar{1}$	$\bar{1}$	Ø	
	Ø	0	0	1	0	$\bar{1}$	
0	0	0	0	0	0	Ø	
Ø	0	1	1	0	$\bar{1}$	$\bar{1}$	
0	0	1	1	0	$\bar{1}$	$\bar{1}$	(9)10

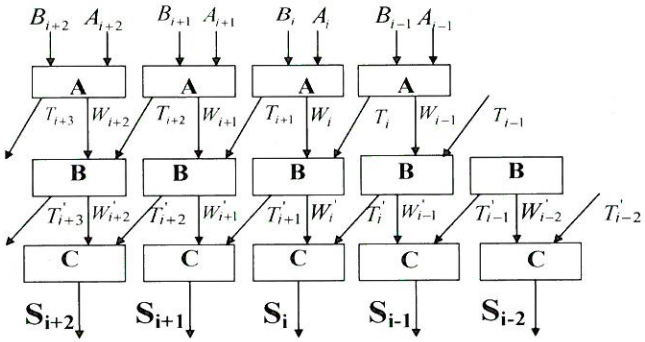

Fig. 1. The NMSD addition: the classical three-step adder.

Table 1. The classical three-step NMSD addition rules: (a) Step1 rules; (b) Step2 rules; and (c) Step3 rules. Two-bit polarization-encoding is also included.

(a)

Input Digits		**Output Digits**	
A_iB_i	Polarization-encoding $a_i^V b_i^V a_i^H b_i^H$	T_{i+1}	W_i
1 1	V V 0 0	$\bar{1}$ [H]	0[0]
1 0	V 0 0 0	$\bar{1}$ [H]	$\bar{1}$ [H]
0 1	0 V 0 0	$\bar{1}$ [H]	$\bar{1}$ [H]
0 0	0 0 0 0	0[0]	0[0]
1 $\bar{1}$	V 0 0 H	0[0]	0[0]
$\bar{1}$ 1	0 V H 0	0[0]	0[0]
$\bar{1}$ 0	0 0 H 0	1[V]	1[V]
0 $\bar{1}$	0 0 0 H	1[V]	1[V]
$\bar{1}$ $\bar{1}$	0 0 H H	1[V]	0[0]

(b)

Input Digits		Output Digits	
$T_i\ W_i$	Polarization-encoding $T_1^V W_i^V T_i^H W_i^H$	$T_{i+1}^{'}$	$W_i^{'}$
1 1	V V 0 0	$\bar{1}$ [H]	0[0]
1 0	V 0 0 0	0[0]	1[V]
0 1	0 V 0 0	0[0]	1[V]
0 0	0 0 0 0	0[0]	0[0]
1 $\bar{1}$	V 0 0 H	0[0]	0[0]
$\bar{1}$ 1	0 V H 0	0[0]	0[0]
$\bar{1}$ 0	0 0 H 0	0[0]	$\bar{1}$ [H]
0 $\bar{1}$	0 0 0 H	0[0]	$\bar{1}$ [H]
$\bar{1}$ $\bar{1}$	0 0 H H	1[V]	0[0]

(c)

Input Digits		Output Digits
$T_i^{'}W_i^{'}$	Polarization-encoding $T_1^{'V} W_i^{'V} T_i^{'H} W_i^{'H}$	S_i
1 0	V 0 0 0	1[V]
0 1	0 V 0 0	1[V]
0 0	0 0 0 0	0[0]
1 $\bar{1}$	V 0 0 H	0[0]
$\bar{1}$ 1	0 V H 0	0[0]
$\bar{1}$ 0	0 0 H 0	$\bar{1}$ [H]
0 $\bar{1}$	0 0 0 H	$\bar{1}$ [H]

It is worth mentioning that the consecutive application of **Step1** and **Step2** computation rules guarantees that 11 or $\bar{1}\bar{1}$ digits do not appear at the same digit position in the third step, and consequently the carry propagation is eliminated. Further, the subtraction operation can be achieved by applying a complementing operation step first and then followed by the three computation steps rules for the addition. Moreover, due to the redundancy of the representation, one may obtain simpler addition rules by taking into consideration the current digits A_iB_i and the lower digits $A_{i-1}B_{i-1}$ to directly produce the intermediate transfer ($T_{i+1}^{'}$) and weight ($W_i^{'}$) digits as shown in Figure 2.

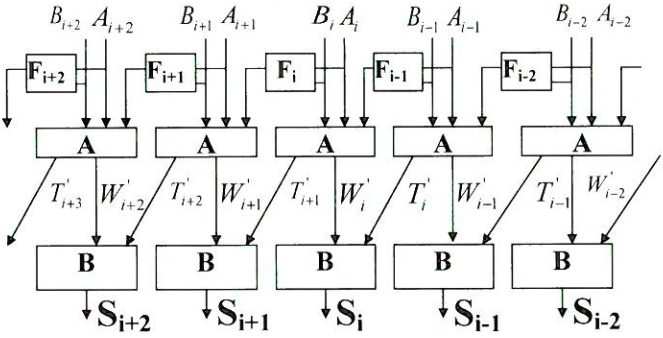

Fig. 2. The NMSD addition: the flagged adder.

Next, T'_{i+1} and W'_i digits are added using **Step3** computation rules (see Table 2). In this regard, a flag bit "F_i" that has a value of 0 or $\bar{1}$ to classify the less significant pair of NMSD digits $A_{i-1}B_{i-1}$ into two groups is employed. In addition, a much simpler addition scheme may be achieved by considering the next lower digits $A_{i-2}B_{i-2}$ altogether with the current digits A_iB_i and the lower digits $A_{i-1}B_{i-1}$. These digits are put into groups to produce the sum digit O_i (see Figure 3 and Table 3).

Table 2. Two-bit polarization-encoding of the flagged NMSD addition: (a) the flag bit rules; (b) the first-step rules; and (c) the second-step rules.

(a)

Input Digits		**Flag Bit**
NMSD A_iB_i	Polarization-encoding $a^V_{i-1}b^V_{i-1}a^H_{i-1}b^H_{i-1}$	F_{i-1}
1 1	V V 0 0	0
1 0	V 0 0 0	0
0 1	0 V 0 0	0
0 0	0 0 0 0	0
1 $\bar{1}$	V 0 0 H	$\bar{1}$ [H]
$\bar{1}$ 1	0 V H 0	$\bar{1}$ [H]
$\bar{1}$ 0	0 0 H 0	$\bar{1}$ [H]
0 $\bar{1}$	0 0 0 H	$\bar{1}$ [H]
$\bar{1}$ $\bar{1}$	0 0 H H	$\bar{1}$ [H]

(b)

Input Digits		Transfer/Weight Digits	
		$F_{i-1}=0$	$F_{i-1}=\mathrm{H}$
NMSD A_iB_i	Polarization-encoding $a_i^V b_i^V a_i^H b_i^H$	$T'_{i+1}W'_i$	$T'_{i+1}W'_i$
1 1	V V 0 0	10 [V0]	10 [V0]
1 0	V 0 0 0	0 $\bar{1}$ [0H]	11 [VV]
0 1	0 V 0 0	0 $\bar{1}$ [0H]	11 [VV]
0 0	0 0 0 0	00 [00]	00 [00]
1 $\bar{1}$	V 0 0 H	00 [00]	00 [00]
$\bar{1}$ 1	0 V H 0	00 [00]	00 [00]
$\bar{1}$ 0	0 0 H 0	$\bar{1}$ $\bar{1}$ [HH]	01 [0V]
0 $\bar{1}$	0 0 0 H	$\bar{1}$ $\bar{1}$ [HH]	01 [0V]
$\bar{1}$ $\bar{1}$	0 0 H H	$\bar{1}$ 0 [H0]	$\bar{1}$ 0 [H0]

(c)

Input Digits		Output Digits
NMSD $T'_iW'_i$	Polarization-encoding $T_i'^V W_i'^V T_i'^H W_i'^H$	S_i
1 0	V 0 0 0	1 [V]
0 1	0 V 0 0	1 [V]
0 0	0 0 0 0	0 [0]
1 $\bar{1}$	V 0 0 H	0 [0]
$\bar{1}$ 1	0 V H 0	0 [0]
$\bar{1}$ 0	0 0 H 0	$\bar{1}$ [H]
0 $\bar{1}$	0 0 0 H	$\bar{1}$ [H]

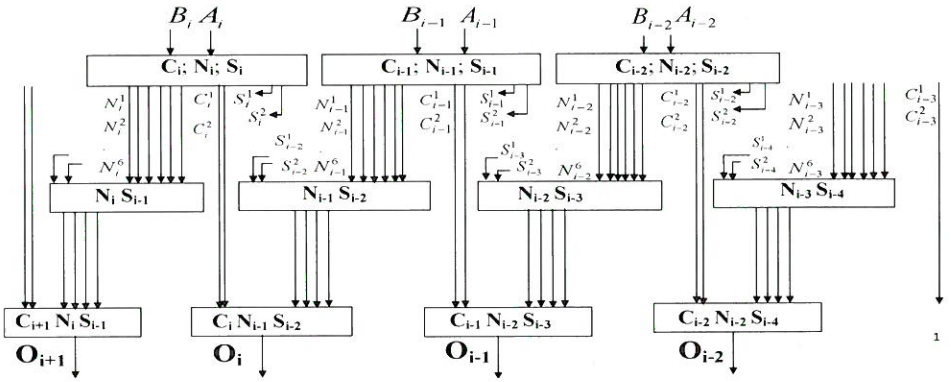

Fig. 3. The NMSD addition: the digit grouping adder.

Table 3. Digits grouping and computation rules NMSD addition; CP: current position; NLOP: next lower position; SLOP: second lower position.

NMSD Digit Groups		
$G_1 = \bar{1}\,\bar{1}$; $G_2 = 0\,\bar{1}, \bar{1}\,0$; $G_3 = 00, 1\,\bar{1}, \bar{1}\,1$; $G_4 = 01, 10$; $G_5 = 11$		
CP Digit Groups	NLOP Digit Groups	SLOP Digit Groups
$a_i\, b_i$	$a_{i-1}\, b_{i-1}$	$a_{i-2}\, b_{i-2}$
$C_1 = G_2 + G_4$;	$N_1 = G_1$; $N_2 = G_2$;	$S_1 = G_1 + G_2 + G_3$
$C_2 = G_1 + G_3 + G_5$;	$N_3 = G_3$; $N_4 = G_4$;	$S_2 = G_4 + G_5$
$N_5 = G_5$;		
NMSD Computation Rules		
$C_1N_1 \rightarrow 1$	$C_1N_5 \rightarrow \bar{1}$	$C_1N_3 \rightarrow 0$
$C_1N_2S_2 \rightarrow 1$	$C_1N_4S_1 \rightarrow \bar{1}$	$C_1N_2S_1 \rightarrow 0$
$C_2N_4S_2 \rightarrow 1$	$C_2N_3 \rightarrow \bar{1}$	$C_1N_4S_2 \rightarrow 0$
	$C_2N_2S_1 \rightarrow \bar{1}$	$C_2N_4S_1 \rightarrow 0$
		$C_2N_2S_2 \rightarrow 0$
		$C_2N_1 \rightarrow 0$
		$C_2N_5 \rightarrow 0$

OPERATION OF TOAD-BASED OPTICAL SWITCH

TOAD switch was demonstrated by Sokoloff *et al.* (1993) as a promising competitor to other similar all-optical switches, which can be used in optical time–division multiplexed (OTDM) communication systems. Further, many researchers pointed out that this ultrafast switch can operate with low energy control signals and consequently it has the potential to be integrated on a chip (Glesk *et al.*, 2001; Houbavlis & Zoiros, 2004; Stubkjaer, 2000, Gayen *et al.*, 2011).

A TOAD consists of a loop mirror with an intra loop 2x2 coupler and a nonlinear element (NLE) which is offset from the loop's midpoint by a distance Δx as shown in Figure 4a. Sokoloff *et al.* (1993) explained the detailed operation of the switch, where a strong optical signal (control pulse – CP) is used to control another optical signal (incoming pulse – IP) through nonlinear interaction in a material based on interferometer setup. Recently, the reflected signal in the switch is used in addition to the transmitted one (Gayen & Roy, 2008). Briefly, the TOAD works as follows. When there is no CP signal, the IP signal enters the loop shown in Figure 4a and splits into two counterpropagating ones. These two signals now recombine and interfere at the input coupler and emerge as a single light at the lower port. However, if a strong CP light is injected into the loop, then it saturates the SOA and its index of refraction is changed. Consequently, the two IP counterpropagating signals will face differential phase shift, such that they will interfere and re-emerge or transmitted from the output port. At the two output ports (reflected and transmitted), a polarization or wavelength filter is used to block the optical CP signal and only pass the optical IP signal. Note that the optical CP (very short pulse) has sufficient energy to modify the optical property of the SOA element, whereas the two counter propagating IP signals do not. Further, in the absence of the CP signal, the input light exits from the lower port in the figure (no light is present in the upper port). However, when both CP and IP signals are present simultaneously, all light is directed towards the upper port in the figure (no light is present in the lower port). When there is no IP signal, both channels receive no light as the filter blocks the CP signal. A schematic block diagram for the TOAD switch is shown in Figure 4b.

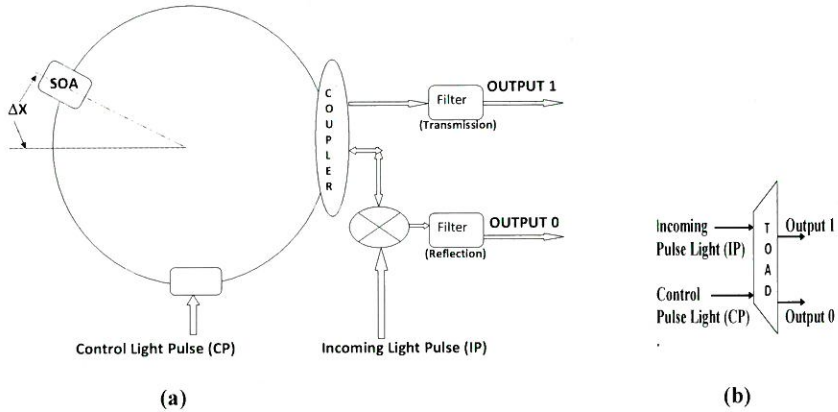

Fig. 4. (a) TOAD-based optical switch; (b) schematic diagram of the switch.

POLARIZATION ENCODED TOAD-BASED NMSD ADDER CIRCUITS

In a previous work (Cherri, 2011), the trinary NMSD digits were encoded using intensity of light, where two-valued (two-bit) logic encoding was used and referred to as "sign" and "value" encoding <*s,v*>. In this encoding scheme, the NMSD digits $\{\overline{1}, 0, 1\}$ are represented by {(1,1), (0,0), (0,1)}, respectively. In this section, we will show the implementation of the adder using polarization-encoding scheme where the digit set $\{\overline{1}, 0, 1\}$ are encoded using polarization states of light as horizontal, no light, and vertical, which are denoted as {*H, 0, V*}, respectively.

In a similar way to the <*s,v*> encoding, one may generate a two-bit encoding scheme using polarized beam splitters as shown in Figure 5. This encoding scheme is denoted as the <*H,V*> polarization encoding scheme. Therefore, the digits $A_i = \{\overline{1}, 0, 1\}$ are represented by two bits $a_i^V a_i^H$ = {(0H), (00), (V0)}, respectively. Thus, to add two polarization-encoded NMSD digits aibi, one needs to incorporate four control signals representing the binary bits (polarized lights) $a_i^V b_i^V a_i^H b_i^H$. Next, the polarized-encoded bits will be used in two channels as input and control signals in the TOAD switches structure to design various parallel adders.

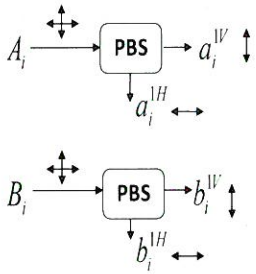

Fig. 5. Two-bit Polarization-encoding for the NMSD digits.

Circuit design 1: Classical three-step NMSD adder

Table 1 lists the <*H,V*> polarization encoding of the classical three-step NMSD adder. In this table, one can identify that some of the output digits are generated from entries (inputs) that have vertical polarization bits, while others are coming from horizontally polarized bits. Note that in the first three entries (the last three entries) $a_i^H b_i^H = 00$ ($a_i^V b_i^V = 00$). Thus, these entries distinguish between the two channels in step1 as shown in Table 1. Similar observations are applied for $T_i^H W_i^H$ and $T_i^V W_i^V$ for step2. In step3, the first two entries and the last two entries separate the two channels. By combining these entries in two different circuits, we will obtain the design shown in Figure 6 for the classical three-step adder where 14 gates are needed as well as 5 gate delays. In this figure, the symbol $\oplus$ is used to denote a beam combiner. In addition, a polarization converter is used in front of some inputs to the TOAD switches since the two inputs lights to a TOAD must have different intensities or opposite light polarization states. Further, the entries in Table 1 are shown at the output ports of the TOAD switches.

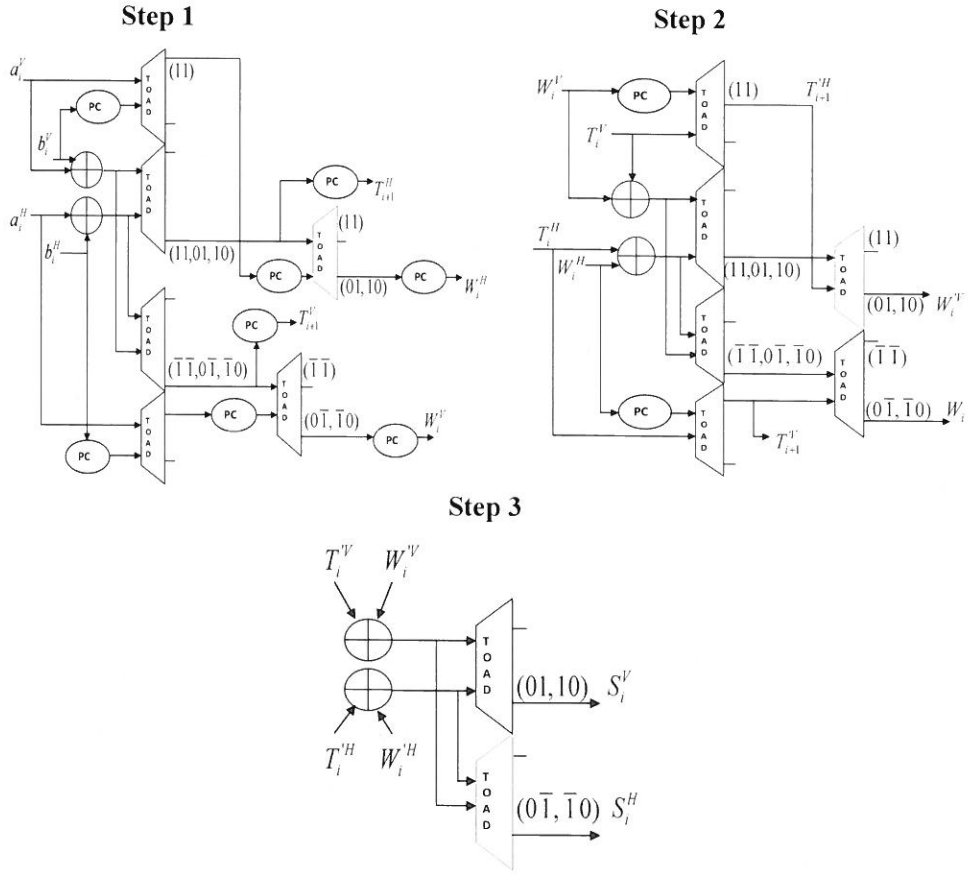

Fig. 6. DESIGN 1: the classical three-step circuit. The symbol $\oplus$ represents a beam combiner; ***PC*** denotes a polarization converter.

Circuit design 2: Flagged three-step NMSD adder

Table 2(a) identifies the minterms that generate the flagged bit F_{i-1}. Since F_{i-1} is binary, there is no need to use the two-bit <H,V> polarization encoding for it. Here logic 1 is represented as horizontally polarized light. Notice that the flag bit F_{i-1} is simply obtained by combining the a_{i-1}^{H} and b_{i-1}^{H} bits. In Table 2b, the transfer and weight digits are listed according to the value of the flag bit F_{i-1} being 0 or H. In a similar manner to the previous design, the minterms are generated by combining $a_i^H b_i^H$ =(00) and $a_i^V b_i^V$ = (00). These minterms are directed as input and control signals to the first two TOAD switches shown in Figure 7. As seen in Table 2b, this flagged bit F_{i-1} needs to be ANDed with the minterms $a_i^V b_i^V a_i^H b_i^H$ that produce the transfer $T_{i+1}^{'V} W_i^{'V}$ and weight $T_{i+1}^{'H} W_i^{'H}$ bits. Once these bits are generated, the final NMSD addition will be obtained according to the rules of Table 2c. Note that in this design, step 3 circuit of Design1 is the same as step 2 for this design. This design requires 10 gates and takes only four gate delay units for the addition. Figure 8 shows an alternative TOAD-based set up to realize the minterms needed in the addition of Table 2b.

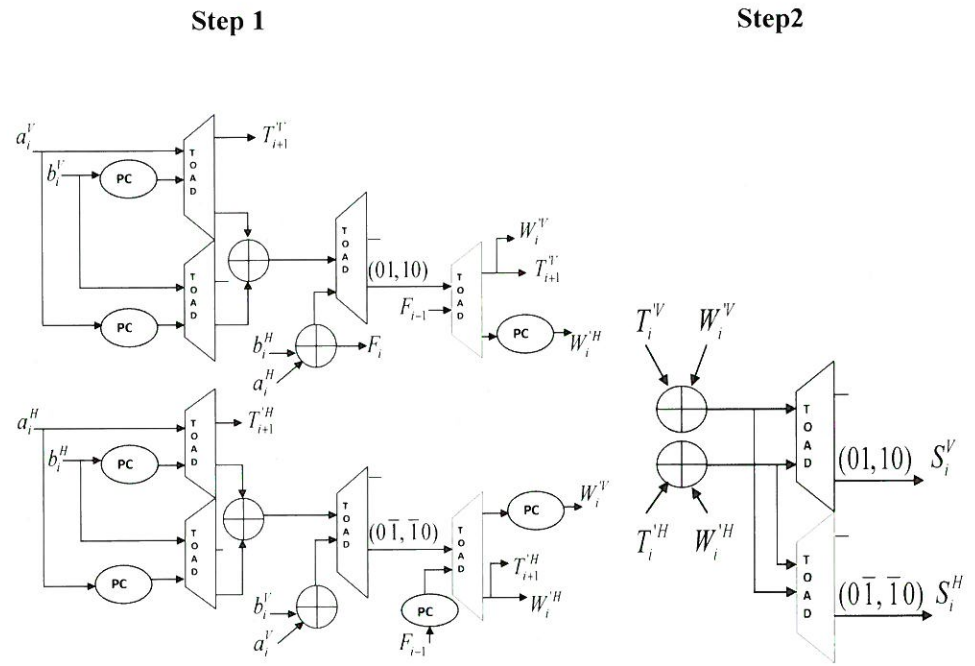

Fig. 7. DESIGN 2: the flagged NMSD circuits.

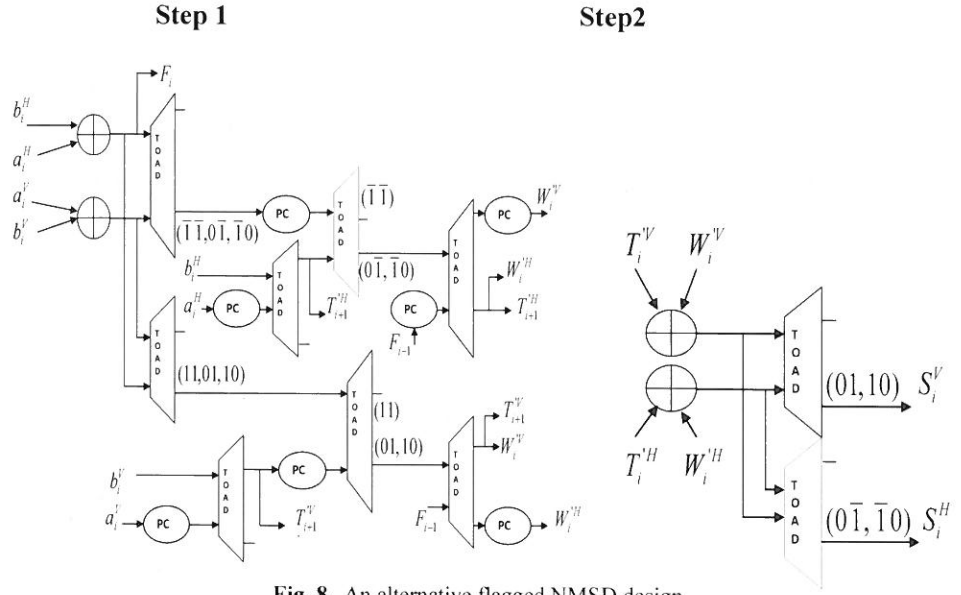

Fig. 8. An alternative flagged NMSD design.

Circuit design 3: Digits grouping NMSD adder

According to Cherri (2011), grouping of NMSD digits $a_i b_i$, $a_{i-1}b_{i-1}$, and $a_{i-2}b_{i-2}$ was demonstrated to produce a faster and more compact intensity-encoded NMSD adder. The digits $a_i b_i$, $a_{i-1}b_{i-1}$, $a_{i-2}b_{i-2}$ are all available in parallel, and consequently, they can be logically combined and routed to produce the output digits as shown in Figure 3. Table 3 lists the digit combinations (groups) that were considered to produce a fully parallel adder. Also, the table lists the computation rules to produce the sum O_i of the addition. As can be seen from Table 3, once we generate the $N_i^1, N_i^2, N_i^3, N_i^4, N_i^5$ terms, then the other two groups C_i and S_i can be realized. In Table 3, the current digits $a_i b_i$ are divided into two groups $C_i^1 = \{N_i^2 + N_i^4\}$ and $C_i^2 = \{N_i^1 + N_i^3 + N_i^5\}$; and the digits $a_{i-2}b_{i-2}$ are grouped into two groups $S_{i-2}^1 = [N_{i-2}^1 + N_{i-2}^2 + N_{i-2}^5\}$ and $S_{i-2}^2 = \{N_{i-2}^4 + N_{i-2}^5\}$. Then, these groups digits are routed to be combined (***OR**ed*) and then cascaded (***AND**ed*) together to produce the computation rules:

$$O_i^V = C_i^1[N_{i-1}^1 + N_{i-1}^2 S_{i-2}^2] + C_i^2 N_{i-1}^4 S_{i-2}^2$$
$$O_i^H = C_i^1[N_{i-1}^5 + N_{i-1}^4 S_{i-2}^1] + C_i^2[N_{i-1}^3 + N_{i-1}^2 S_{i-2}^1]$$

Figure 9a shows how the $N_{i-1}^1, N_{i-1}^2, N_{i-1}^3, N_{i-1}^4, N_{i-1}^5$ terms are generated while Figure 9b shows how to obtain the output sum digit O_i. This design requires 15 gates and 3 gate delay units.

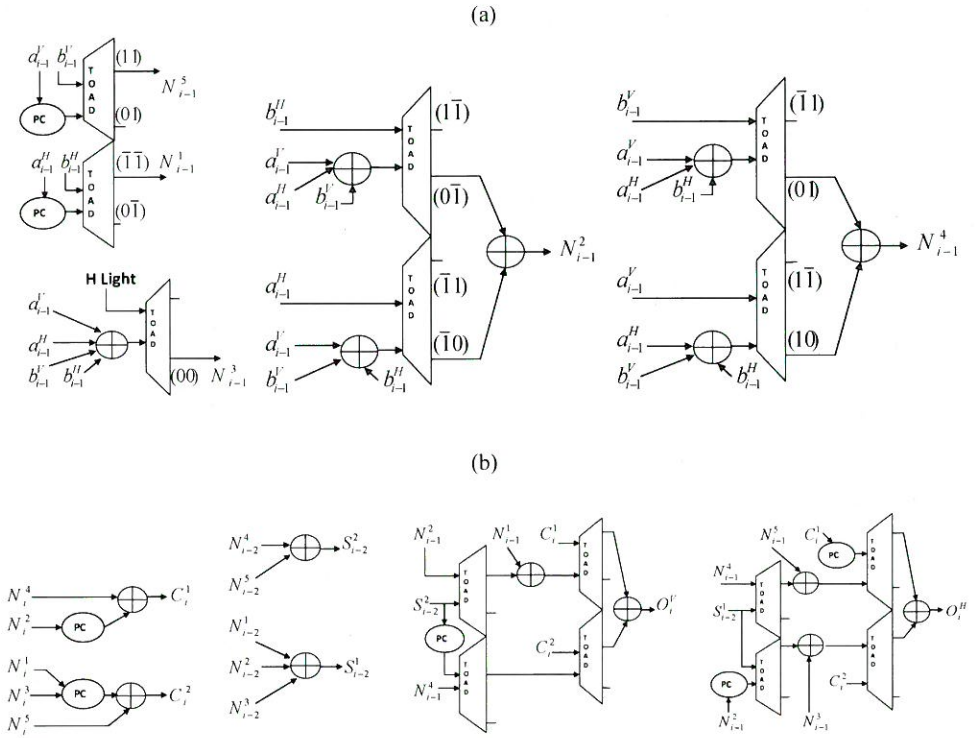

Fig. 9. DESIGN 3: the digit grouping NMSD adder. (a) generating the five Ni-1 digits groups and (b) generating the Ci, Si-2, and Oi digits.

CONCLUSIONS

Three all-optical circuits using polarization-encoded NMSD number representation have been proposed. It is clear from Table 4 that the polarization-encoded NMSD adders are more efficient than the intensity-encoded ones. From Table 4, one can draw the following conclusions. In contrast to the intensity-encoded adders, the proposed adders employ much fewer gates and they are much faster. The proposed classical three-step adder uses 51.7% less gate and it is 44.5% faster; while the flagged adder uses about 45.5% less gates and 42.9% faster. On the other hand, the digits grouping design provides 21% less gates and it is 40% faster. Note that in the previous discussions, many practical designs issues need to be solved. For instance, the issue of cascadability (a switch driving another switch) is a key requirement for building combinatorial networks (Scaffardi, *et al.*, 2007; Gayen, *et al.*, 2012; Chattopadhyay, 2012). Further, design issues regarding the SOA carrier lifetime, synchronization of the inserted lights to the switches, light intensities losses due to splitters/couplers, polarizations, pulse duration, etc need to be considered. Promising experimental

results regarding some of these issues have been reported (Hamilton & Robinson, 2002; Wang **et al.**, 2002; Zoiros *et al.*, 2010)

Table 4. Comparison between the polarization-encoded NMSD adders and the intensity–encoded ones (numbers between parentheses after Cherri, 2011)

NMSD Adder	Gates	Unit delay	Beam Combiners	Polarization Converters
DESIGN1: Classical Three-step	14 (29)	5 (9)	6 (13)	10
DESIGN2: Flagged Three-step	10 (22)	4 (7)	4 (10)	7
DESIGN3: Digits Grouping	15 (19)	3 (5)	16 (13)	7

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Submitted: 10/09/2013
Revised: 02/12/2013
Accepted: 30/12/2013

Journal of Engg. Research Vol. 2 - (2) June 2014 pp. 81 - 99

تطوير أنظمة التعرف على الكلام للصم في اللغات المحلية

*سي. جيالاكشمي، **في. كريشنامورتهي، ***أ. ريفاتهي

*قسم هندسة الكمبيوتر – كلية ترتشي- ترتشي- تاميلنادو- الهند

**قسم هندسة الكمبيوتر – كلية الهندسة – جامعة آنا- جيناي- الهند

***قسم هندسة الكمبيوتر- كلية ساراناثان الهندسية- ترتشي- تاميلنادو- الهند

الخلاصة

هذه الورقة تقدم أداء نظام التعرف على الكلام بالنسبة للأطفال الطبيعيين والأطفال الصم. مع أن التجويف الأنفي والسمعي للصم يبدو طبيعيا إلا أنهم لا يستطيعون النطق بسبب عدم قدرتهم على السماع، وذلك لأن فهم اللغة والنطق بها مرتبط بعمليات في الدماغ لذلك فإن الشخص المصاب بضرر في السمع أو بنشاط الدماغ بسبب في الولادة أو سبب طارئ يجد صعوبة في التحدث، هؤلاء يصنفون على أنهم صم أو ضعيفي السمع بناء على القدرة على السماع.

إن التشخيص المبكر للصم يساعد الشخص المعنى على إصدار أصوات بواسطة العلاج بالتحدث، إذا تم تشخيص الصمم في مرحلة متأخرة فإنه من الصعب جعل حديث المصاب مفهوما لدى الآخرين، لذلك أصبح من المهم إيجاد طريقة لجعل لغة هؤلاء المصابين مفهومة وخاصة باللهجات المحلية.

في هذه الورقة تم تطوير نظام للغة التاميل باستخدام خاصية MFCC في الإستخلاص في المقدمة وأداة HTK المتكاملة في نهاية النظام حيث تم تقييم هذا النظام بالمقارنة بين محادثة أشخاص طبيعيين وأشخاص صم وكانت نسبة التعرف على الكلمات 92.4 % بالنسبة للأشخاص الصم و98.4 % بالنسبة للأشخاص الطبيعيين، مع أنه من الصعب للمستمعين غير المعتادين على سماع حديث الأشخاص الصم إلا أن النظام يمكن استخدامه للتعرف على المحادثة بين الأشخاص الصم فيما بينهم.